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# DC Power Circuit Evaluation for the Development of the Barrel Calorimeter Processor V2

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The development of the CMS Barrel Calorimeter Processor (BCP) for the high-luminosity LHC poses a challenge due to strict power requirements. To minimize the risk of performance degradations or component damage, a project-specific and inexpensive evaluation board has been designed with multiple DC power circuits to safely test and evaluate them outside of the expensive BCP. The planned tests will verify several operating parameters of the power circuits, including output voltage, ripple voltage, and transient load. We will report on the results of these tests along with any roadblocks, their solutions, and lessons learned from this investigation.

## Summary (500 words)

For the high-luminosity LHC (HL-LHC), a new back-end electronic board, the Barrel Calorimeter Processor (BCP), is being developed to support the CMS barrel calorimeters. The BCP is an ATCA-based board with very challenging power requirements, including a FPGA core voltage of 0.85V with a strict valid range of +/- 25mV while supporting up to 160A of current, and voltages for the FPGA multi-gigabit transceivers (MGT) of 0.9V, 1.2V and 1.8V with a maximum allowable noise of 10 mVpp. Additionally, the multiple optical transceivers, or FireFly, require 1.8V, 3.3V and 3.75V with maximum low noise requirements of either 30 mVpp or 50 mVpp depending on the model. Failure to meet these power requirements threatens performance degradations and could even damage expensive components such as the FPGA and FireFly which would be a costly outcome in both time and money.

To minimize the risk, we propose creating a project-specific evaluation board that includes the chosen DC power circuits and uses layout techniques required by the BCP design. This evaluation board will include multiple circuits to also evaluate any possible negative interactions such as thermal or input voltage noise that negatively impact performance. This approach is more accurate than using a manufacturer's evaluation board because those are often designed and optimized for trade-offs that benefit the manufacturer and may not be suitable for our application.

Several tests are planned for the circuits on the custom evaluation board, including verifying the output voltage range under typical and maximum loads and verifying that the ripple voltage remains under 75% of the maximum specification. A transient load test will be performed to verify that the output voltage remains within the specified ranges during transients. A voltage ramp test will confirm that the FPGA voltages all rise to 95% of the nominal voltage within 0.2 to 40 ms. An integration test will load all circuits to verify that the circuits remain under thermal limits and that there are no negative impacts between circuits that may increase ripple voltage on the common input voltage.

Based on the results of the tests, circuit modifications may be performed if there are failing circuits, and then the modified circuits will be retested. In the case of multiple circuits for a single supply, the circuit that best meets specifications will be selected. The presentation will describe the power circuits and discuss the test results, comparing them against the specifications. Any problems encountered, along with circuit modifications and other solutions, will also be examined. This approach will ensure that the BCP meets the challenging power requirements for the HL-LHC and avoids any performance degradations or expensive loss of time or money.

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