The End-of-Substructure (EoS) card for the ATLAS Strip Tracker Upgrade: From Design to Production.

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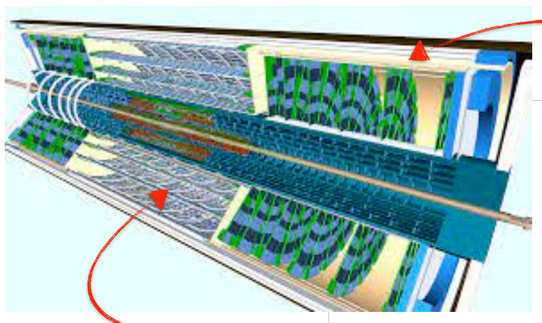
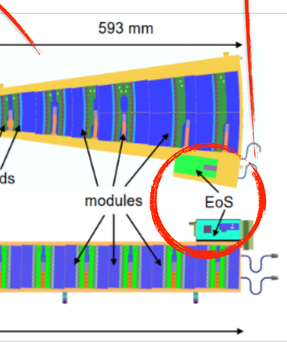
TWEPP23 Poster Session

The ATLAS ITk

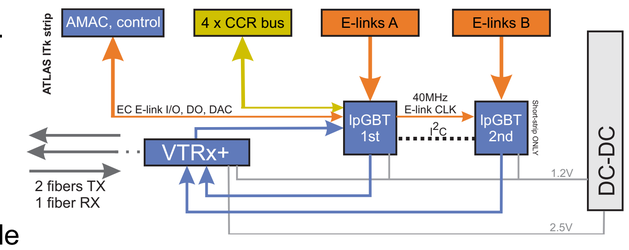
- The Large Hadron Collider will upgrade to **High-Luminosity (HL-LHC).**
- The ATLAS Inner Detector will be replaced by an all-silicon system, the **Inner Tracker (ITk)**:
  - Pixel detector close to the interaction point.
  - Strip tracker consisting of a barrel (built from "**staves**") and two end-caps (built from "**petals**").
- At the end of each stave or petal, **a pair of main-secondary EoS card** is placed.

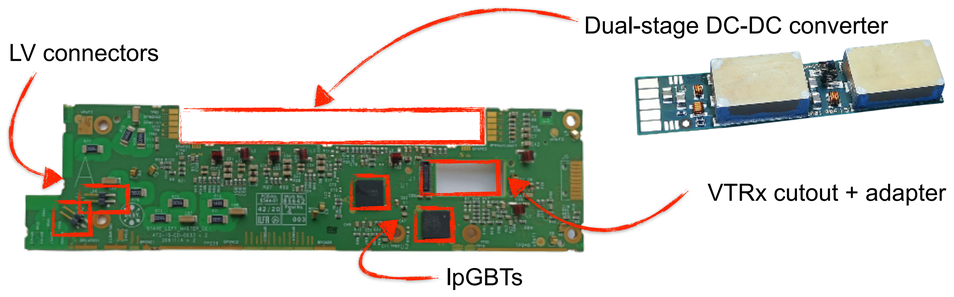




The End-of-Substructure Card (EoS)

- The EoS cards are the **gateway** between on- and off-detector systems.
  - Supplies LV & HV power
  - Timing, Trigger and Control
  - Detector Control System
  - Send the data off the module



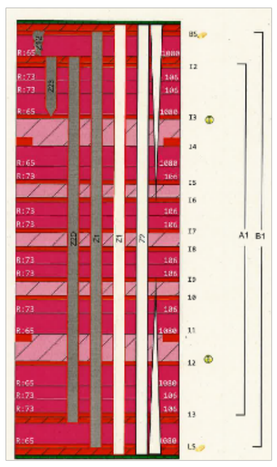


- Due to the detector geometry, **14 different EoS flavours** are needed.
  - Different physical layout designs and flex lead geometries.
  - Variants with either one of two lpGBTs.

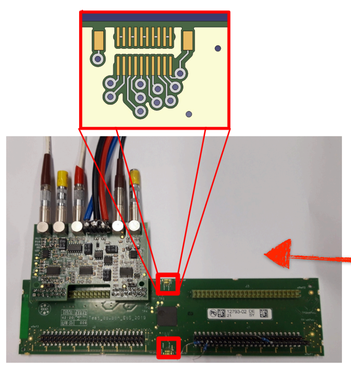
→ **Difficulties in the design and testing** of the EoS cards.

START

PCB Design



- Hierarchical design based on configurable and modular blocks.
  → **Blocks reused in the 10 different flavours**.
- PCB with **14 layers**.
- Re-assignment of gates and pins.
  → **Optimisation of the physical layout**.
- Strict requirements: radiation hardening, geometry…
  → **Vendor-specific design**.



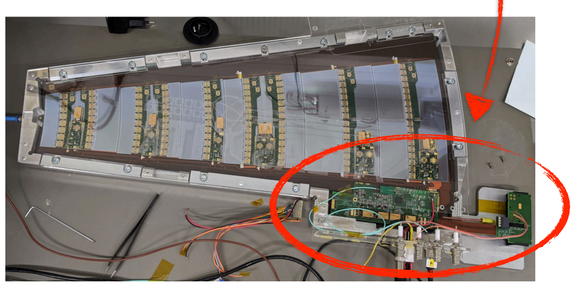
Unpopulated PCB Reception

- Manufacturer tests
  - Connectivity (E-test against netlist).
  - Resistivity/impedance.
  - Visual inspection, images of vias and traces.
- Customer Test Coupons:
  - Resistivity/impedance.
  - Bond pads testing.
  - Thermo cycling test.

Arrival to Assembly Sides

FINISH

- **EoS cards in system tests**.

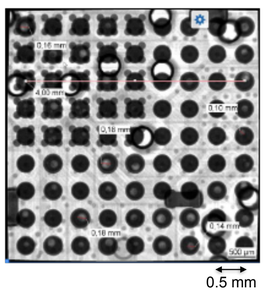


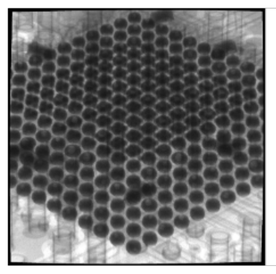
Conclusions and Lessons Learned

- Extensive **prototyping and testing** are crucial.
- Moving into the **production stage**.
  → **~2000 EoS cards** will be tested.
- High degree of **automatisation** needed.
- Compressible interpretation of test results: **pass/fail**
  → Upload results to the **production database**.
- Get the most from the **project reviews**.

Populated PCB Reception

- **3D x-ray** of the solder joints of the BGA.
  → Important for ensuring long-term operation.



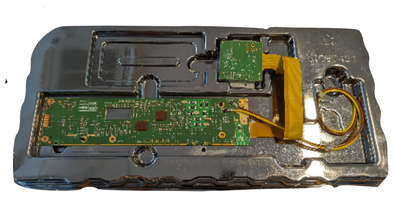


70 µm trace structures

- Check all devices on the board are correctly connected (**Flying Prober Tester**).

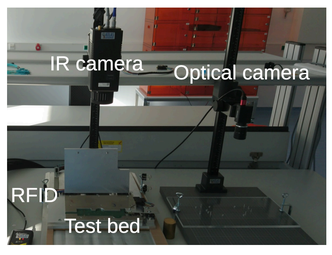
Packing and Shipping

- **ESD-proof sealed bag** (nitrogen atmosphere).
- **Label + QR code** .



Quality Control: 4 Test Benches

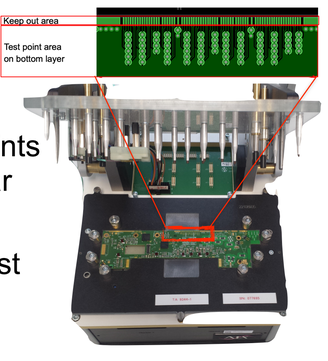
#1
- **Optical & IR inspections**, dimensions, flatness.
- **Check optical links** (up/down).
- **Power consumption**.
- **PLL** synchronisation.
- **ADC calibration**.



#2
- **Thermal stress test**: from -35°C to +40°C. Power on/off for each cycle.
  → Test of basic function (optical links, short BERT test, readout ADC values)

#3
- **HV Test**: Each single HV line to 1.1 kV and monitor the leakage current for 1 minute.

#4



- **Functionality** tests.
- **Needle prober**: test points on a grid of 0.7 mm near the bonding pads.
- Bit-error rate (**BERT**) test of all 640 Mb/s fast signals.
- **Eye-diagrams** of up-links.

References:

- ATLAS collaboration, Technical Design Report For the ATLAS Inner Tracker Strip Detector, CERNLHCC-2017-005, ATLAS-TDR-025 (2017).
- P. Goettlicher et al., Current status of the end-of-substructure (EoS) card project for the ATLAS strip tracker upgrade using final ASICs (TWEPP 2022).