Digital duty cycle correction system for clock paths in radiation-tolerant high-speed wireline transmitters

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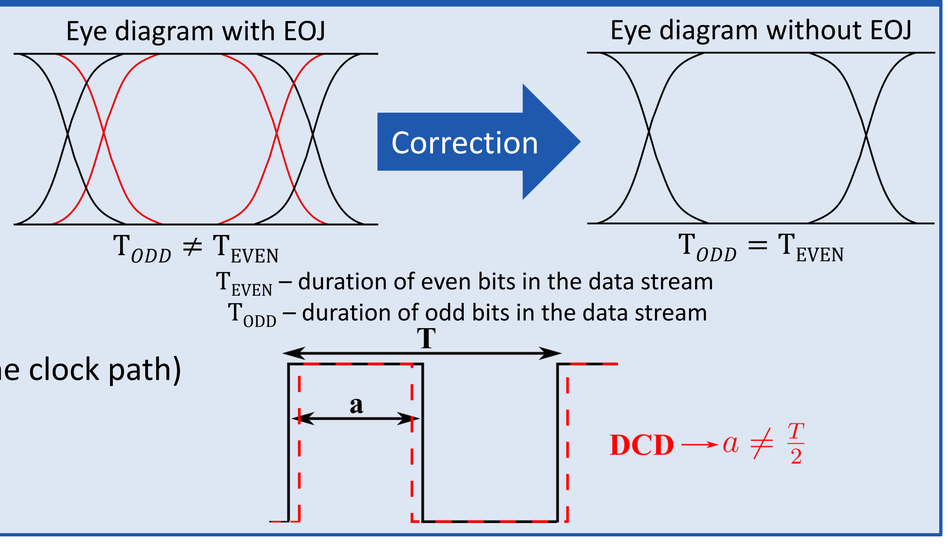
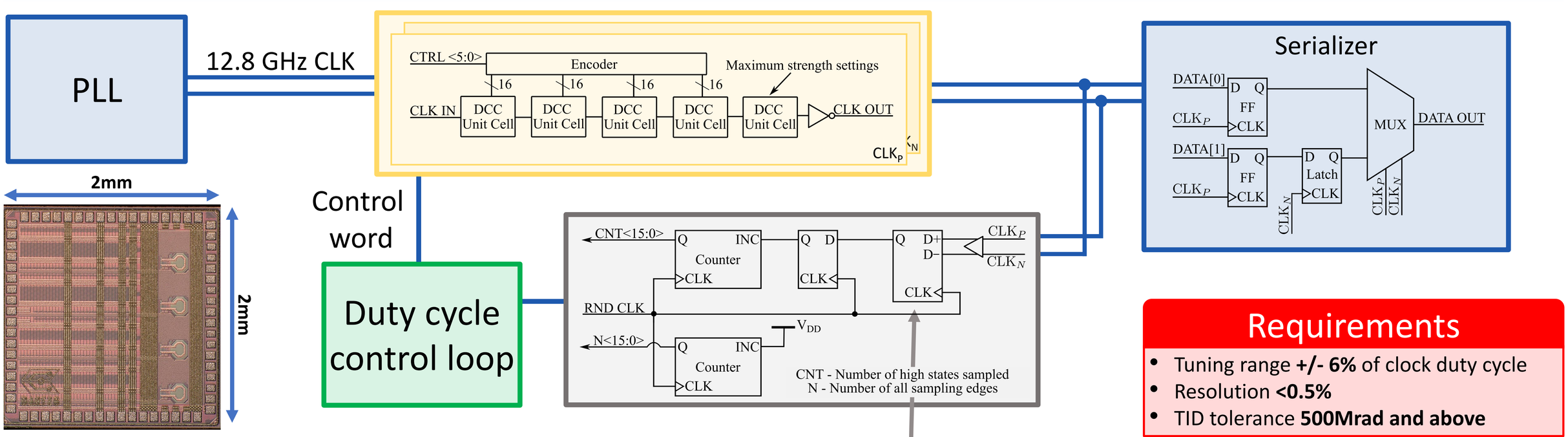
Introduction

- The design of the **DART28** chip which is a radiation-hard high-speed wireline transmitter faces stringent data quality requirements imposed by the commercial communication standards
- The specified even-odd jitter (**EOJ**) parameter needs to be suppressed to below **1.4ps**
- Any amount of the clock duty cycle distortion (**DCD**) for the DART28 serializer (half-rate topology final stage) is translated into EOJ in the output data stream
- The DCD of the clock is the deviation of its duty cycle from the desired target value of (50%)
- The DCD arises as a result of the rise/fall times imbalance of the gates and buffers on the clock path due to the:
  - Design constraints (e.g. Imbalanced PMOS and NMOS strength ratio of the buffers/inverters on the clock path)
  - Process, voltage, and temperature (**PVT**) variation
  - Total ionizing dose (**TID**) degradation (unequal degradation of PMOS and NMOS devices)
- Minimization of the EOJ could be performed by precise control of the clock duty cycle





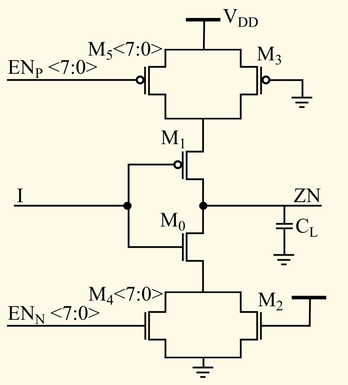
Requirements

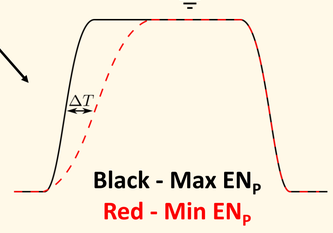
- Tuning range **+/- 6%** of clock duty cycle
- Resolution **<0.5%**
- TID tolerance **500Mrad and above**

Duty cycle correction chain (DCC)

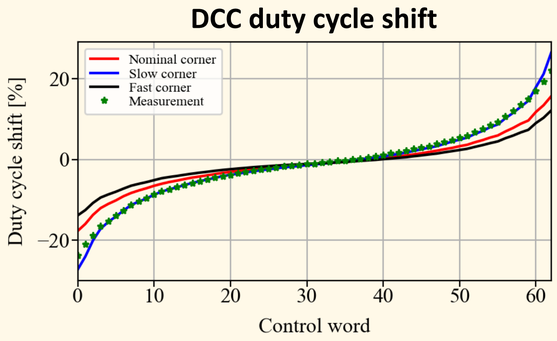
- Chain of 4 controlled unit cells (**UC**) used to achieve target tunability through all PVT variations
  - Each UC is a digitally controlled current-starved inverter
  - PMOS and NMOS branches are controlled independently by two separated 8-bit words
- The fifth UC is used to ensure equal loading for all variable cells
- The duty cycle is changed by each UC by controlling the rise/fall time which results in a delay time difference
- Thermometric encoding is used to ensure a monotonic tuning The DCC chain partially replaces the clock distribution that would be placed in the transmitter anyway
- The additional jitter increase attributed to the degradation in rise/fall times across the DCC chain does not degrade the jitter of the clock distribution chain

DCC Unit Cell (UC)

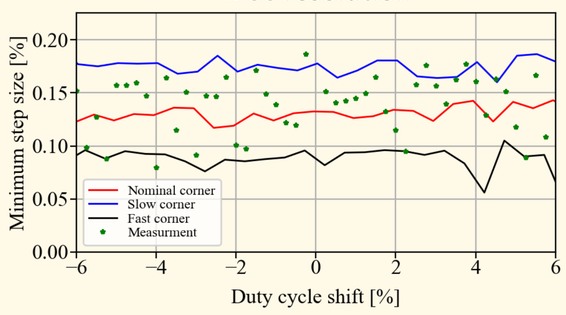




DCC duty cycle shift



DCC resolution



$$T_{rise} \propto \frac{1}{EN_P}$$

$$T_{fall} \propto \frac{1}{EN_N}$$

Duty cycle measurement (DCM)

- Random sampling technique [2] is adopted in order to obtain the high-accuracy measurement
- The number of samples is inversely proportional to the square of the intended resolution

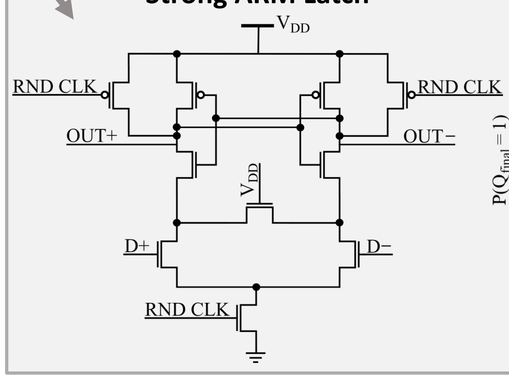
$$N \propto \left(\frac{1}{Resolution}\right)^2$$

- The duty cycle measurement result is obtained as follows

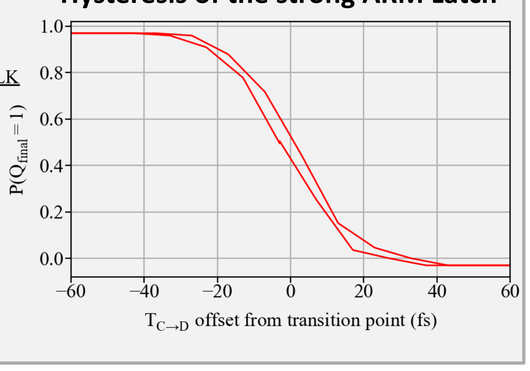
$$Duty\ \text{Cycle} = \frac{CNT}{N}$$

- A sampling clock (RND CLK) frequency unrelated to the measured clock
- A StrongARM latch is used as a sampling circuit. It offers high gain and very small hysteresis

Strong ARM Latch



Hysteresis of the strong ARM Latch



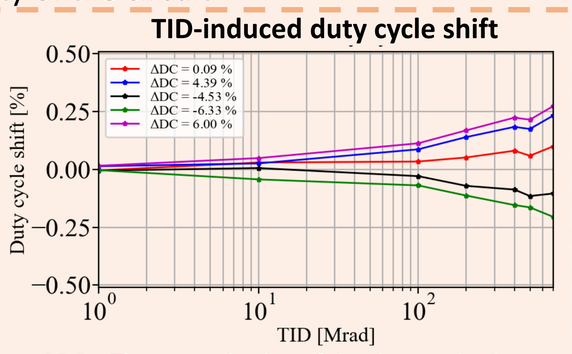
Radiation hardening aspects

- Triple modular redundancy (**TMR**) of the DCC, as well as DCM, was used to increase the immunity of the design to the errors caused by the single event transients (**SET**)
- Wider transistors are used to limit TID-induced g_m degradation in PMOS devices [3]
- Spacing DCC chains by at least 10 µm further increases the SET immunity of the circuit

Radiation validation

- Extending the model from [1] by TID-induced mobility degradation based on ULVT transistor radiation characterization results
- Simulation performed with that model showed radiation immunity of the DCC chain → once set DCC ensures proper duty cycle value even at ultra-high dose rates
- TID-induced degradation results in a **0.25%** duty cycle shift compared with the pre-rad value

TID-induced duty cycle shift



ΔDC – The pre-rad value of the duty cycle change

Duty cycle control loop

- Digital logic regulates the duty cycle by altering the DCC control word based on the DCM results
- Implemented algorithm decrements or increments the control word depending on the sign of the required tune until the minimum error point is reached
  - The number of iterations needed to tune the duty cycle is constrained to **5** by the usage of the binary search
- Control loop implemented off-chip in the first DART28 prototype
- Maximum duty cycle error < **0.5%**

References

[1] KLEKOTKO, Adam, et al. Radiation hard true single-phase-clock logic for high-speed circuits in 28 nm CMOS. *Journal of Instrumentation*, 2023, 18.02: C02068.
[2] BHATTI, Rashed Zafar; DENNEAU, Monty; DRAPER, Jeff. Duty cycle measurement and correction using a random sampling technique. In: 48th Midwest Symposium on Circuits and Systems, 2005. IEEE, 2005. p. 1043-1046.
[3] ZHANG, Chun-Min, et al. Characterization of gigarad total ionizing dose and annealing effects on 28-nm bulk MOSFETs. IEEE Transactions on Nuclear Science, 2017, 64.10: 2639-2647.

Contact

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