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Digital duty cycle correction system for clock paths in radiation-tolerant high-speed wireline transmitters

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Ongoing developments in the field of radiation-tolerant high-speed transmitters (HST) aim to increase data rates above 25 Gb/s while increasing total ionizing dose (TID) tolerance above 1 Grad. The use of half-rate architecture imposes tight constraints on clock signal quality, in particular its duty cycle. Radiation degradation of transistors in the clock path causes duty cycle distortion (DCD), affecting the output signal quality of the HST. In this contribution, a digitally controlled duty cycle correction system suitable for HST is presented, which compensates for process, voltage, and temperature variation as well as radiation-induced duty cycle distortion of the clock.

Summary (500 words)

Radiation-tolerant transmitters targeting data rates above 25 Gb/s have to cope with stringent requirements of clock quality. The parameters of the clocks for such systems are constrained by the output data quality defined in modern communication standards limiting values of the signal distortion or different types of jitter. One of those parameters is Even Odd Jitter (EOJ), which primarily originates from duty cycle distortion in the high-speed clock. In high-energy physics experiments, those transmitters are used in a radiation environment so these circuits should exhibit robustness against high levels of total ionization dose (TID). Prior research has shown that radiation-induced unequal degradation of PMOS and NMOS devices leads to changes in the duty cycle of critical clock signals.

The Demonstrator ASIC for Radiation-Tolerant Transmitter in 28 nm (DART28) developed in the context of the Experimental Physics R&D programme on technologies for future experiments at CERN aims to achieve a data rate of 25.6Gb/s per link and radiation robustness up to 1 Grad. The serializer of that transmitter implements half-rate topology which constrains the highest-speed clock to 12.8 GHz. The half-rate topology also implies that any duty cycle distortion of the high-speed clock will result in additional EOJ at the output. The commercially used communications standards require an EOJ below 0.035 Unit interval peak-peak (UIpp) which in this application is 1.36ps. Without active duty cycle correction, meeting this specification over PVT and radiation-induced degradation is a very challenging problem in advanced CMOS nodes. To meet this specification over an extended range of TID, the duty cycle correction system of the clock was designed to meet the stringent specification and ensure proper transmitter operation over a wide TID range.

The designed digitally controlled duty cycle correction system consists of two main parts:

• A duty cycle adjustment (DCA) circuit comprises a chain of current-starved inverters with digitally controlled driving strength. In each inverter, the rise and fall times can be controlled independently to counteract radiation-induced changes in the duty cycle.

The implemented DCA circuit provides tunability of ±6% (±4.8 ps) across PVT corners with a step size better than 400fs.

A random sampling duty cycle measurement (RS-DCM) circuit, based around a sampling flip flop with ultra-low hysteresis (<10fs) guarantees high precision in distinguishing between low and high states. The flip flop samples the high-speed clock with an uncorrelated low-speed clock. If the clock signal is truly sampled uncorrelated to the sampling rate, the number of acquired relative ones represents the clock's duty cycle if a

sufficient amount of samples was taken.
In this paper, the architecture, performance, tunability curves and influence of the duty cycle distortion on the high-speed clock on the output of the HST will be presented. Also, TID-induced degradation will be compared to an uncompensated clock path. TID degradation simulations were performed using device models including TID-related degradation of NMOS and PMOS transistors, accounting for differences in their respective TID sensitivity.

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