

- 2700 readout channels w/ fully custom readout chain (from SiPM to DAQ)
- 10 electronics crates/disk (280 boards total)
- SiPM cooling to -10 °C

• 2700 Read-Out Units

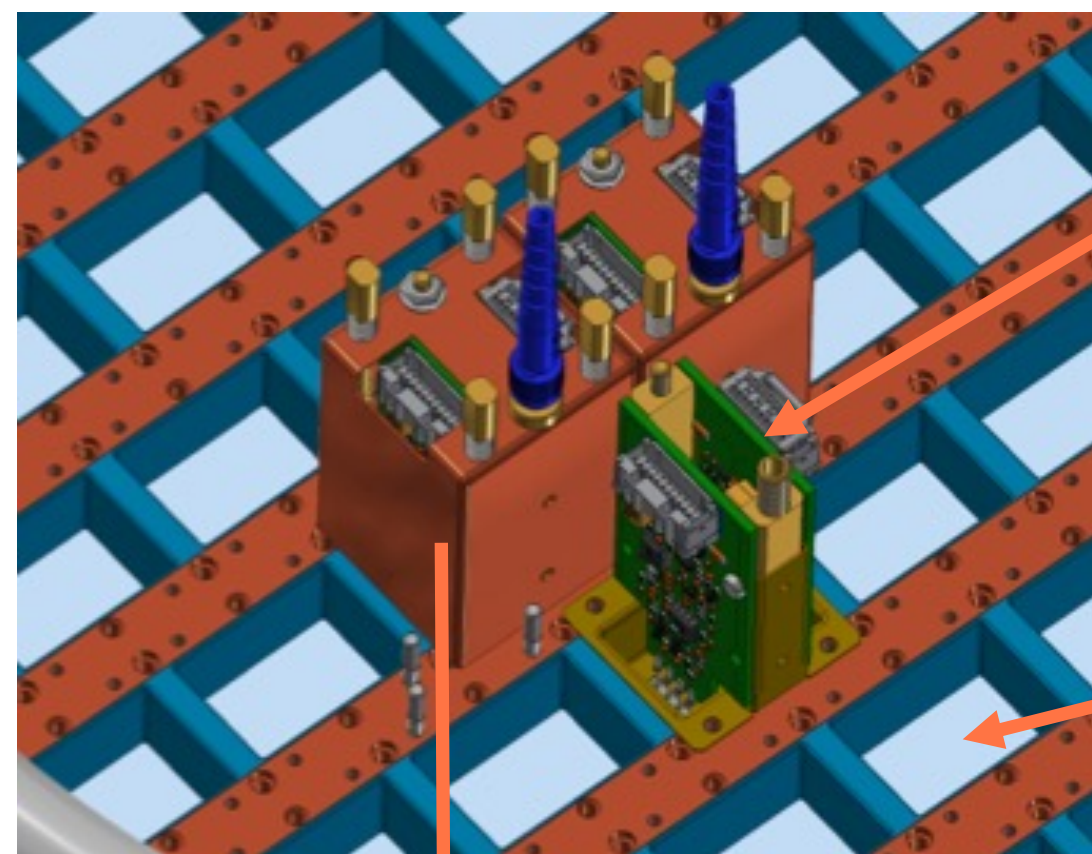
- Two fully independent readout channels per cry
- 2 large-area UV-extended SiPM
- **2 Front-End Electronics (FEE) boards**
 - SiPM amplification and shaping
 - Digitally controlled SiPM monitoring and biasing

• 140 Mezzanine Boards (MB)

- Slow-control distribution
- FEE power distribution
- ARM-microprocessor based

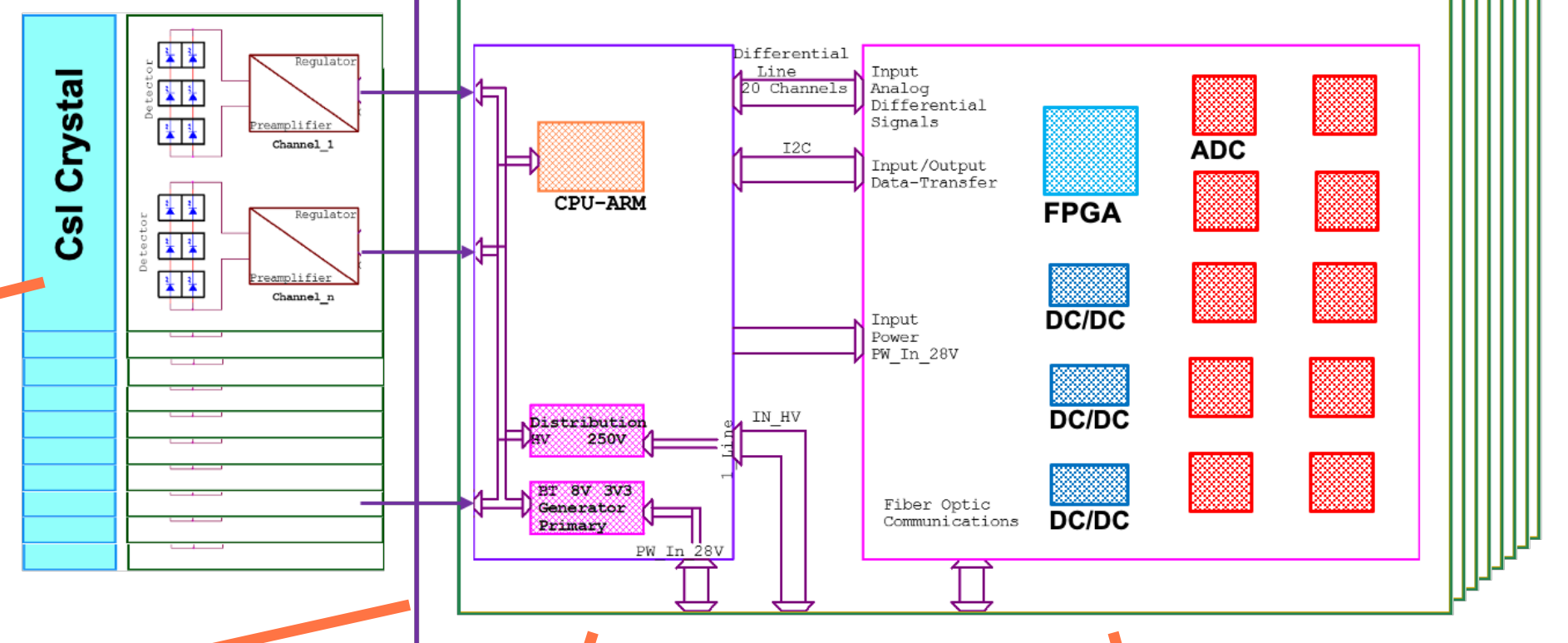
• 140 custom digitiser boards (DIRAC)

- Signal digitisation @ 200 Msps w/ 12-bit flash ADC
- Digitisation to allow good signal reconstruction despite the high expected pileup
- *PolarFire* rad-hard FPGA
- VTRX 10 Gbps optical link to Detector Control System
- DIRAC v3 prototype ready



Disks x 2

**10 crystals/board
(20 FEE/board)**



Crate x10

(Mezzanine board + DIRAC) x8

