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Demonstration of the digital readout chain in the NvDEx experiment

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NvDEx is a proposed experiment to hunt for the neutrinoless double beta decay of 82Se, with a high pressure SeF6 gaseous TPC. The readout and DAQ system are important parts of the experiment. The readout plane placed in one endcap of the TPC consists of around 15,000 sensors for charge measurement. It is crucial to read out data from all of these sensors efficiently. This paper will introduce the design of the demonstrator system for the digital readout chain, including the front-end digital sensor array, the data aggregation module and the DAQ system in the back-end.

Summary (500 words)

Double beta decay has been observed with a few nuclides. However, the neutrinoless double beta decay (0νββ) is still unobserved though the lower limit of half-life period has been pushed to magnitude of 1026 years for some nuclides. 82Se is a nuclide candidate for 0νββ experiment, with the decay energy of about 3 MeV. NvDEx is an experiment for 0νββ detection with a high pressure TPC. For the first step, the NvDEx-100 TPC will be filled with around 100 kg SeF6 under 10 atm pressure. The uniqueness of NvDEx is that the charge drifted to the endcap is measured without avalanche amplification. Around 15,000 charge sensors will be placed on the readout plane, on which each sensor will have 6 neighbors with the pitch of 8 mm. Each sensor can measure the charge collected by the electrode on it, then the decay energy and the track of the drifted ions can be calculated. The final version of sensor is expected to include the electrode for charge collection, the Charge-Sensitive-Amplifier for charge measurement, the ADC for pulse digitization and the digital I/O module for data exchange between sensors. Currently the CSA is still under testing, and improvement on the design is needed to achieve 45 e- ENC. The first version of digital I/O ASIC has been taped-out and tested. In this paper we will introduce the design of the DAQ system especially the hardware and firmware, the data aggregation module and the integration with a small digital sensor array for full chain bidirectional digital data transmission.
The DAQ system in the back-end is based on the PCIe infrastructure. A 16-lane PCIe card supporting 24 fiber optical links has been designed. The throughput from the card to the server is around 180 Gbps. The card supports 28 Gbps optical transmission, but slower QSFP modules could be used in the NvDEx experiment. With the digital I/O, data of the 15,000 sensors will be transferred to the plane edge. In total, there are about 300 digital I/O with speed of about 50 Mbps. A few data aggregation module (DAM) will be placed on the edge of the plane to reduce the quantity of cable connections, which helps to reduce the radioactive background. On one side, high-speed transceiver chips on these modules connect these bidirectional digital I/O. On the other side, the transceivers communicate with the DAQ system via 20 optical links of 1 Gbps. Full digital chain of both directions has been evaluated. For the downlink, commands from the server are encoded in the PCIe card firmware and sent to the DAM. The DAM forwards the 8B10B decoded commands to the digital I/O ASIC, which does the further decoding based on a custom protocol. For the uplink, the encoded data is transferred through the digital I/O chain. The transceiver carries out the 8B10B encoding for data from 16 digital I/O and sends data to the DAQ system. The data is finally sent to the server after decoding in the DAQ firmware.

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