Digital Processing Prototype for the SPS BLM System at CERN

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Abstract

The Beam Loss Monitoring system plays a crucial role in the CERN's Super Proton Synchrotron beam monitoring and machine protection. With the upcoming renovation of the system, the acquisition electronics can be based on an innovative ASIC designed by CERN. This paper presents the development of the control and digital processing electronics for this BLMASIC, reviews the architecture and design choices, discusses implementation details, including the controls and redundancy schemes, and highlights some preliminary results. The conclusion outlines the future development steps, and emphasises the interest of this simple and robust architecture using LpGBT and VTRx for critical systems.

SPS BLM System Foreseen Architecture
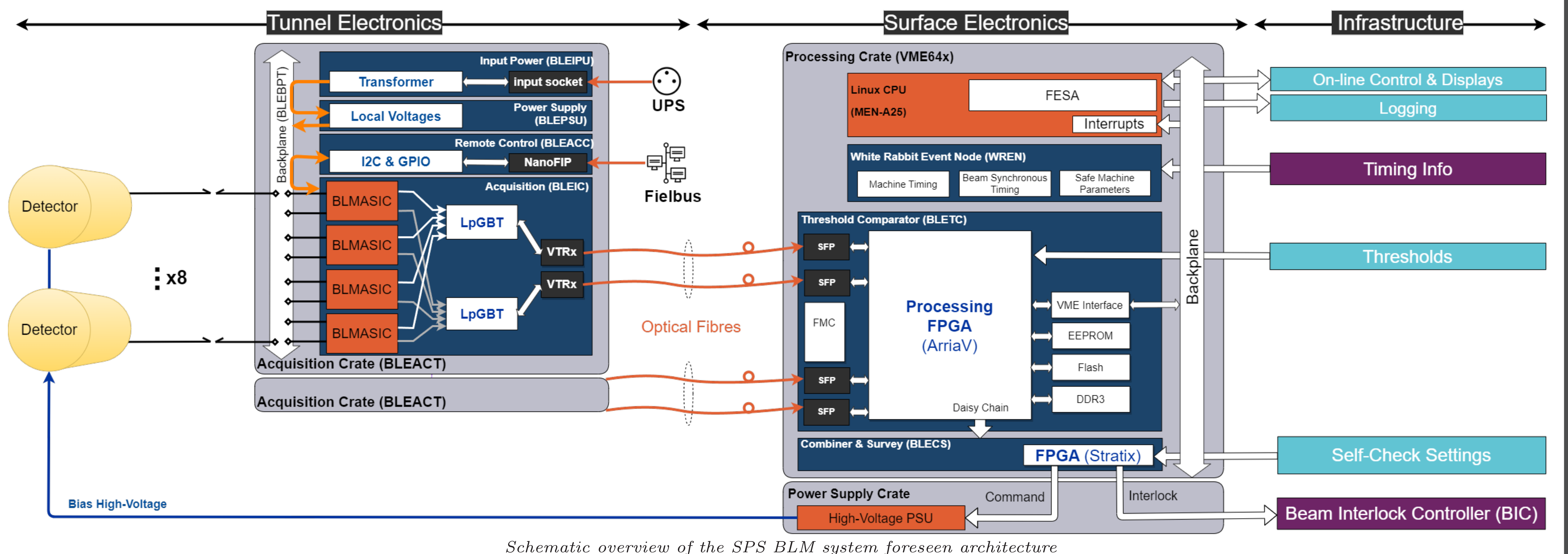
Schematic overview of the SPS BLM system foreseen architecture
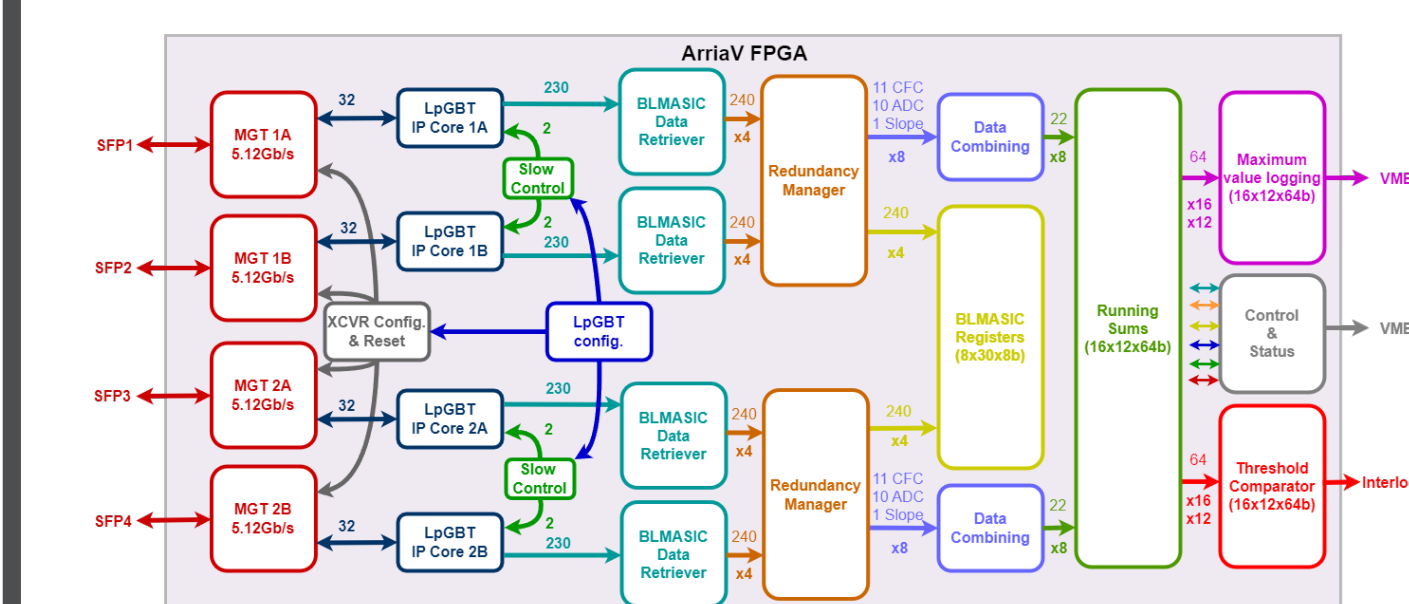
Acquisition Board
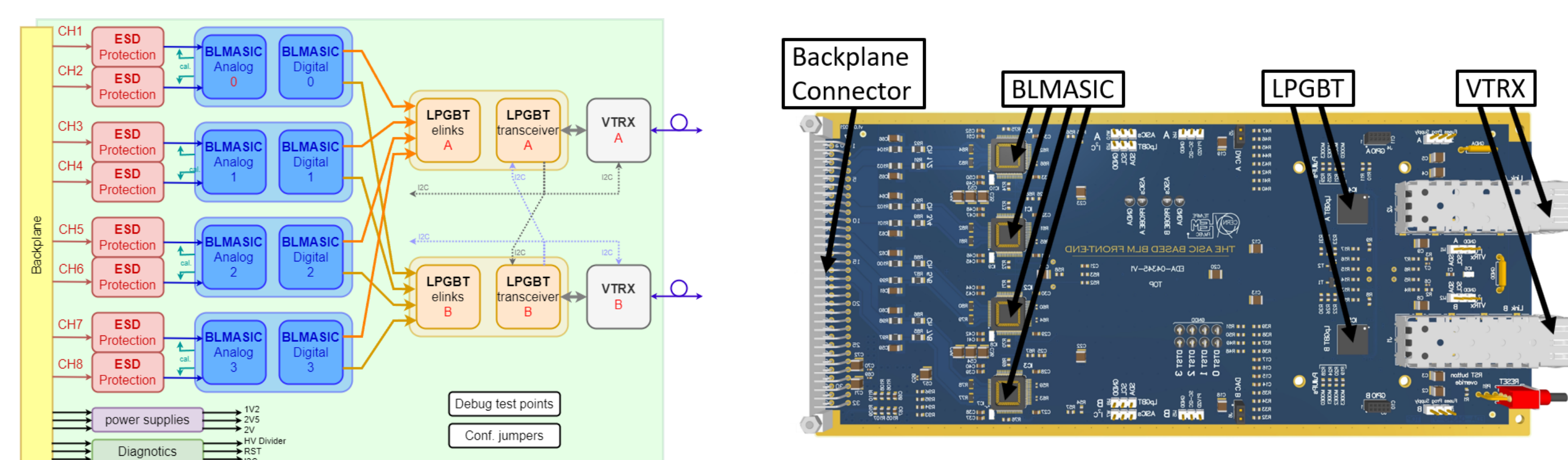
BLEIC Architecture and Layout Top View

The BLM SPS Acquisition electronics (BLEIC) is fully based on radiation-hard components designed at CERN by EP-ESE:

Component	Description	Tested TID
BLMASIC	current to frequency conversion	3 kGy
LpGBT	high-speed serial & and I2C control	3M Gy
VTRx	optical transceiver	10 kGy

Processing Architecture

VFC-HD Backend Processing Architecture

	Data reception	Processing	Total ArriaV
ALM	17822	11653	26.2%
Mk10	22	229	17.7%
DSP	0	16	1.7%
XCVR	4	0	22.2%

VFC-HD Occupancy rate

A flexible and robust data reception module was developed on VFC-HD to reliably receive the BLMASIC data through two redundant pairs of optical links. An embedded FSM automatically connects, configures the remote electronics and continuously checks the link quality to select the best one.
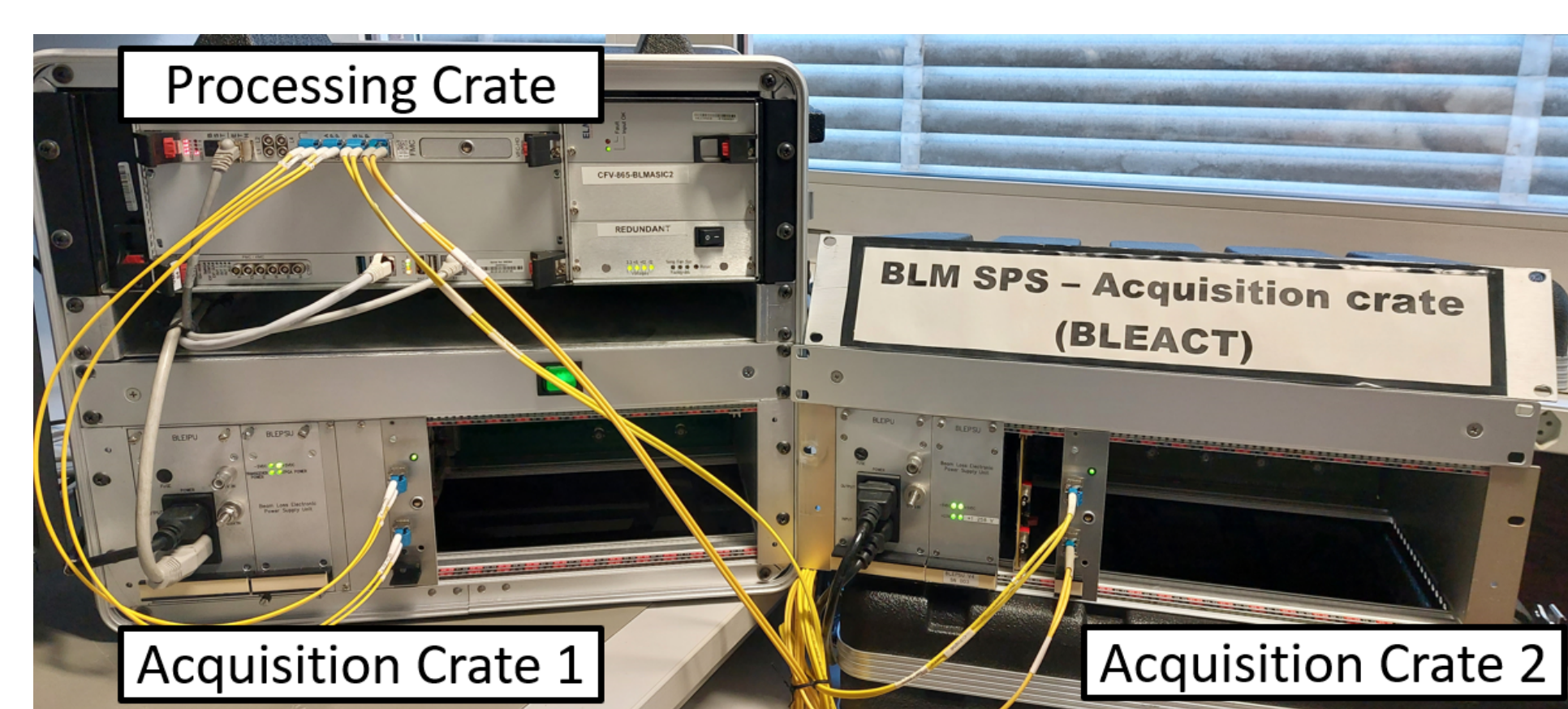
For this prototype, around 26% of the FPGA is used. The data reception block for 4 optical links utilizes 15% of the logic, with potential for optimization of diagnostics. Meanwhile, the measurement processing module accounts for approximately 10%, with plans to better meet the operator's requirements and add new features.

Prototype Setup & BLMASIC

A standard VME crate, the BLEACT acquisition crate and a NUC for storing raw data, have been integrated into a movable box to ease installation and change of location. A second crate was added in the lab to test the acquisition of 16 channels (4 optical links in parallel). This prototype will be installed in the SPS in 2024 to get data with beam and real monitor and cabling and real beam data.

The EDGE GUI is a new BI tool, used first the first time on this project. Although not a real-time tool, this interface uses the full power of Python and enables rapid debugging by simply deploying the new EDGE reader on the desired FEC, and provides graphics, logging and read/write register polling.
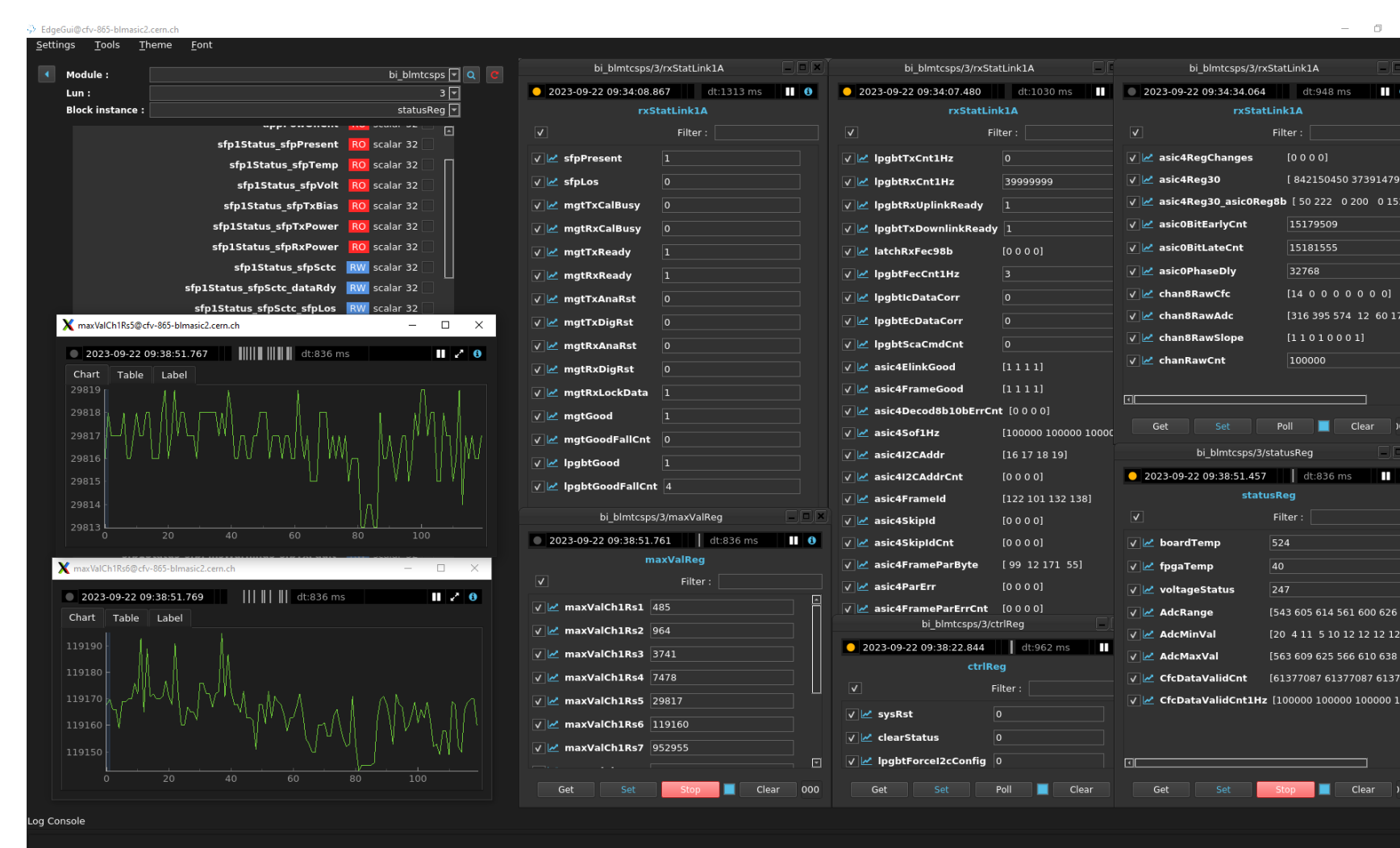
The BLMASIC, developed at CERN by EP-ESE, was fully characterized and tested up to 3 kGy. It uses a current-to-frequency converter combined with an ADC, to provide a 10 µs readout and loss measurements down to 1 pA with an error below 1% in the range [35 µA;1 mA].

Prototype setup in the lab

EDGE GUI example
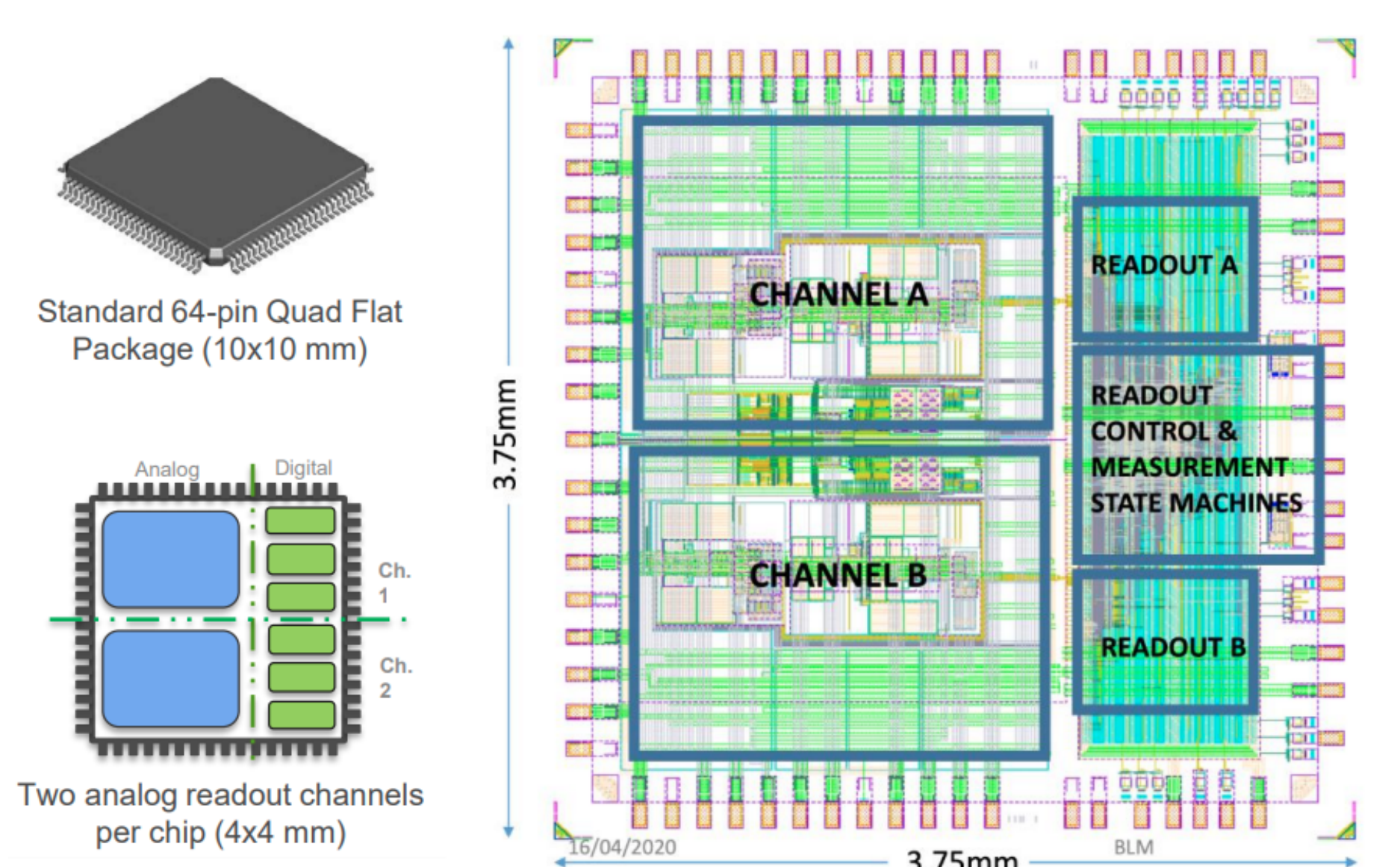
Overview of the BLMASIC chip architecture