TWEPP 2023 Topical Workshop on Electronics for Particle Physics

Design of the ASIC readout scheme for the JUNO-TAO experiment

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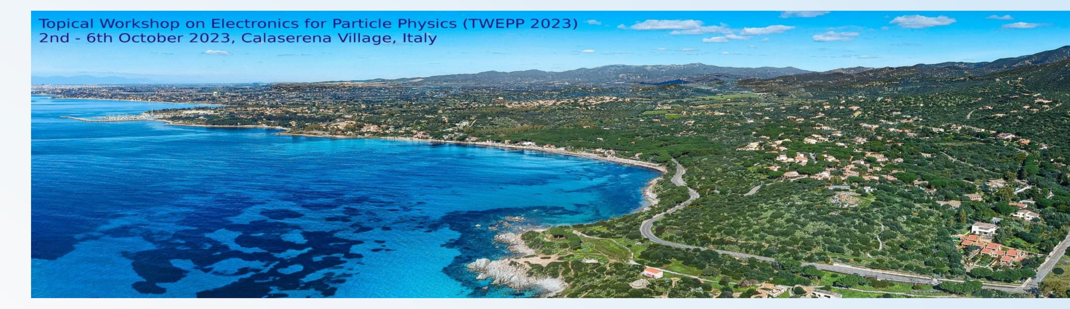


Introduction to JUNO-TAO (Taishan Antineutrino Observatory)

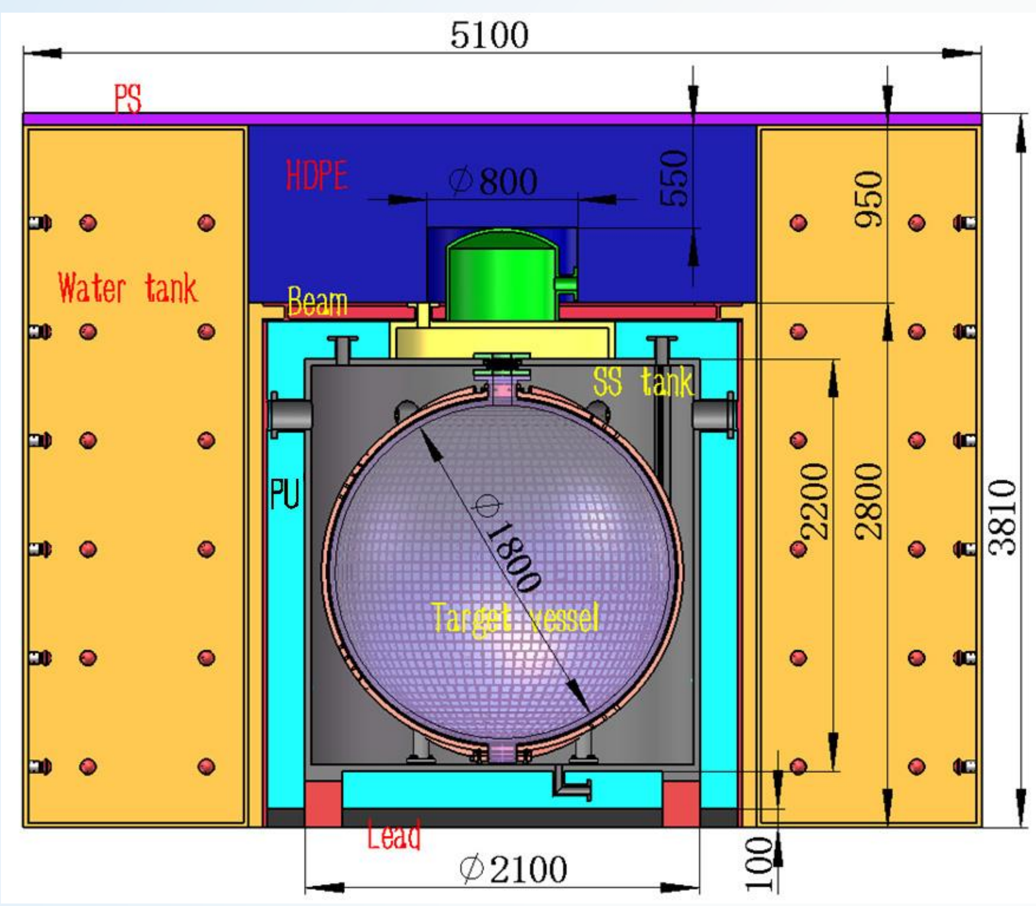


Fig. Conceptual design of the TAO detector. The unit of the dimension is in milimeter.

- TAO is a satellite experiment of the Jiangmen Underground Neutrino Observatory (JUNO)
  - precisely measure the reactor antineutrino spectrum with a record energy resolution of < 2% at 1 MeV.
- TAO will be operated at -50◦C to reduce the influences on the energy resolution from the SiPM dark noise.
- Approximately 10 m^2 SiPMs will be installed on the inner surface of a copper shell
  - The SiPMs are packaged in 4024 SiPM tiles
  - The coverage of the SiPM tiles is approximately 95%
  - The photon detection efficiency of the SiPMs must reach 50%， which yields a photon detection of ~ 4500 photoelectron (p.e.) per MeV.
  - Each tile with dimensions of about 50 mm × 50 mm consists of 8 × 8 SiPMs (6 × 6 mm^2 for each SiPM).
- The backup readout scheme for JUNO-TAO

Introduction to Klaus6

	KLauS6
Target	SiPM calorimetry
Designer	Heidelberg
Input channels	36
Dynamic range	4.5 fC ~ 450 pC 0.03 p.e.~ 2800 p.e.
ADC	40MHz 10/12 bit SAR ADC
Dead time	0.6 us
Time resolution	200 ps
Power consumption per channel	26.6 uW(Power Pulsing) 3.6 mW(full operation)

Tab. Key Parameters of Klaus6

- Input stage → Buffer & distribute signal current, SiPM bias voltage tuning
- 2 integration branches → Different charge range
- 2 comparators → Timestamp & ADC start, self-selected gain
  - Leading edge current discrimination
- Developed by University Heidelberg
  - 36-channel SiPM readout
  - UMC 180nm CMOS technology
- Application
  - Calorimetry for future linear collider experiments

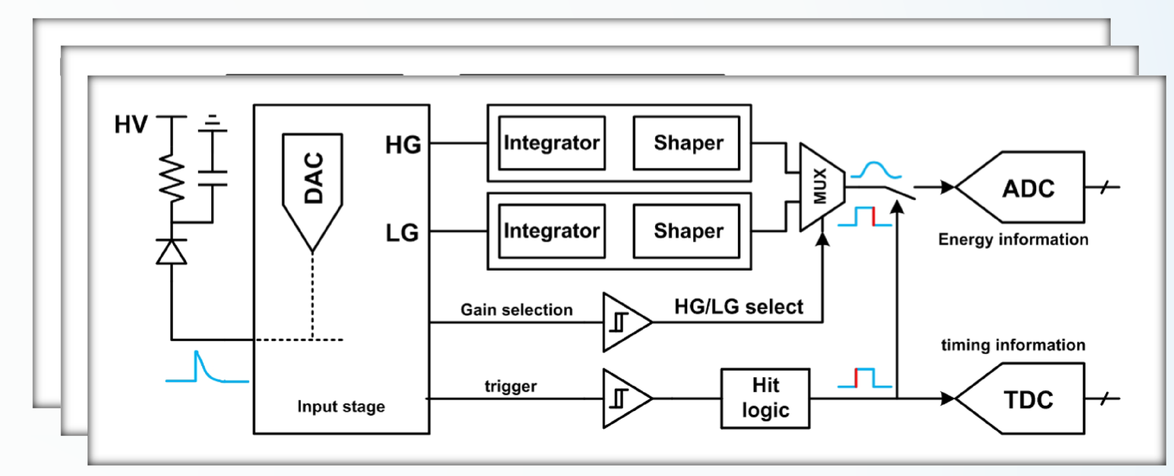
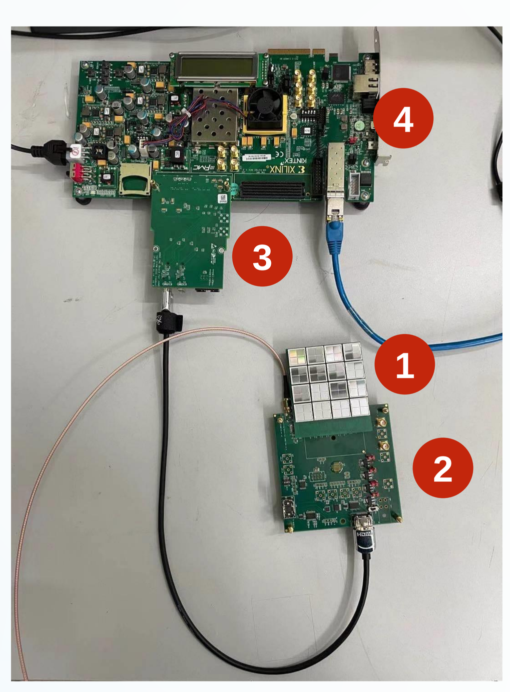
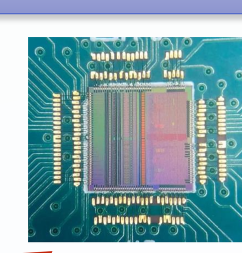


Fig. Structure Diagram

Introduction to ASIC Readout Prototype for the JUNO-TAO

- SiPM tile board
  - 8 x 8 array from Hamamatsu
- TAO_WIRE_BONDING_TEST board
  - KLauS6 bare die via wire-bonding
  - Debug and testing point
- HDMI_FMC board
  - A FMC expansion board to connect multiple test board with HDMI cables
  - Voltage and current monitoring
- Xilinx Evaluation Kit KC705 board
  - The same FPGA (Kintex 7) with the FEC board
  - Control and readout through the FMC HPC/LPC.
  - The hardware based network processors (SiTCP) are employed for data transmission via GbE.
- A SiPM evaluation kit for the KLauS6 bare die via wire-bonding
- Cascade connection through HDMI cables





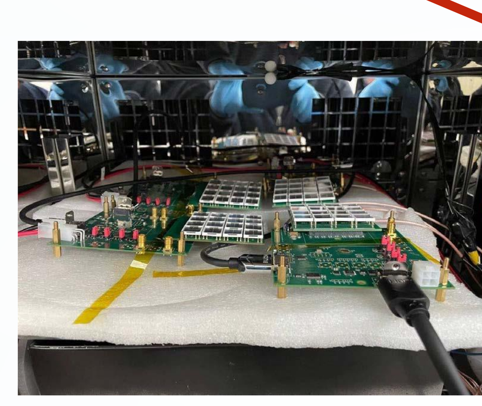
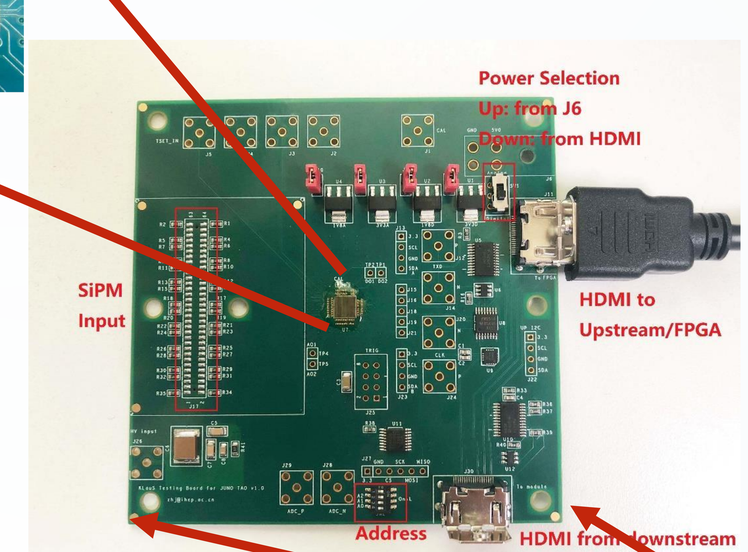


Fig. 4 chips are cascaded



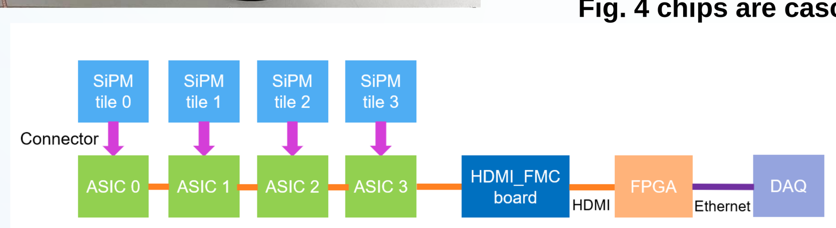


Fig. Prototype Readout System

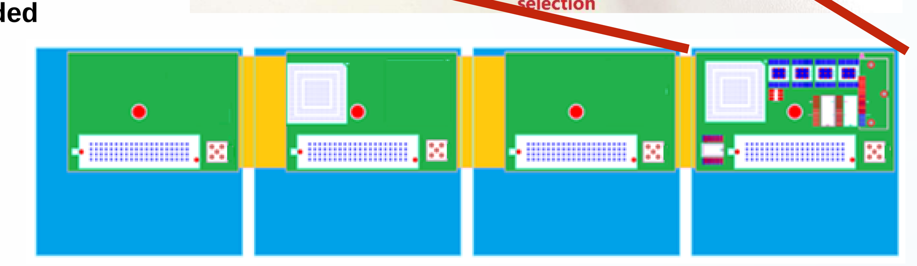
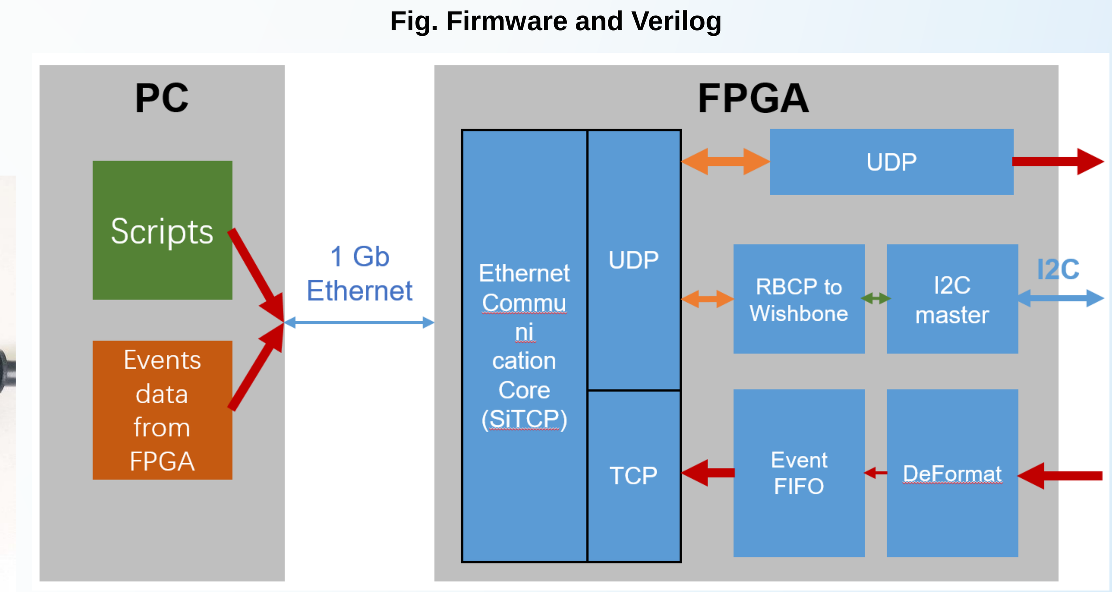


Fig. TAO_WIRE_BONDING_TEST board and Klaus6

Fig. Firmware and Verilog



Firmware/Verilog

- UDP for control
- TCP for readout
- 160Mbps LVDS interface
  - 8b10b encode
  - CRC (Cyclic Redundancy Check)

Performance Measurement With Charge injection

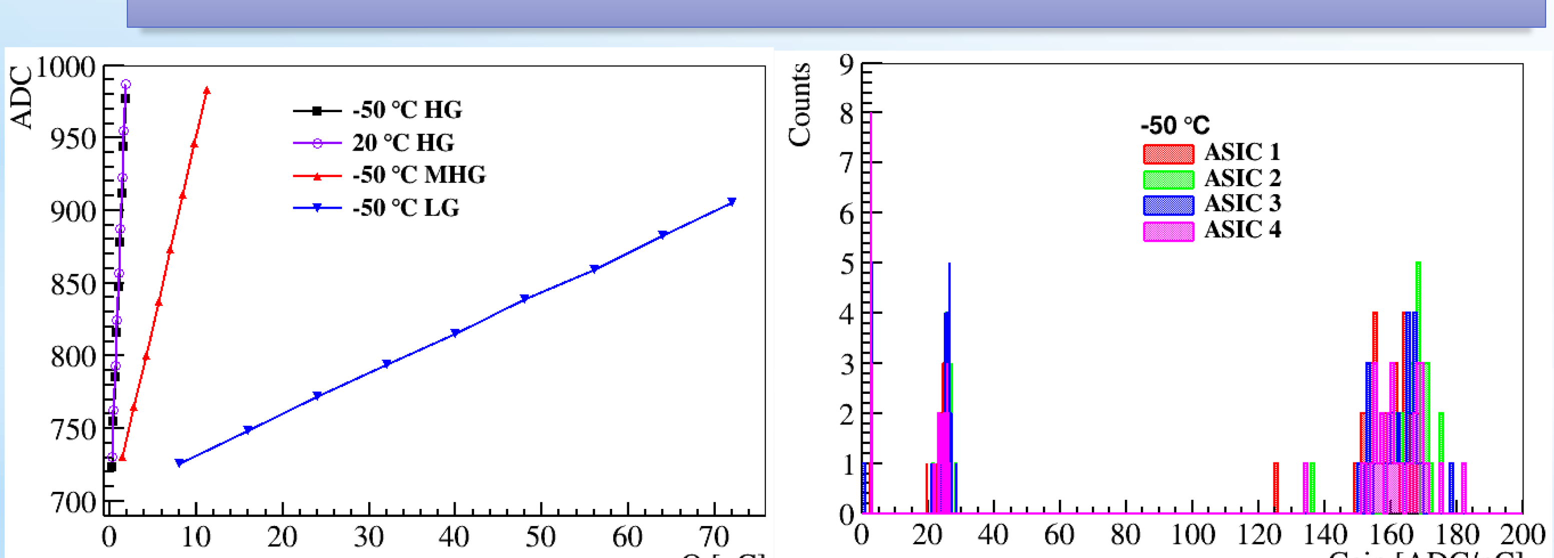


Fig. Gain measurement

- Gains in 3 branches (HG 1:1, MHG 1:7 and LG 1:40) have been characterized for 4 chips at low temperatures, which shows good linearity.
- The input capacitance variations (5%) contribute to the non-uniformity between channels.

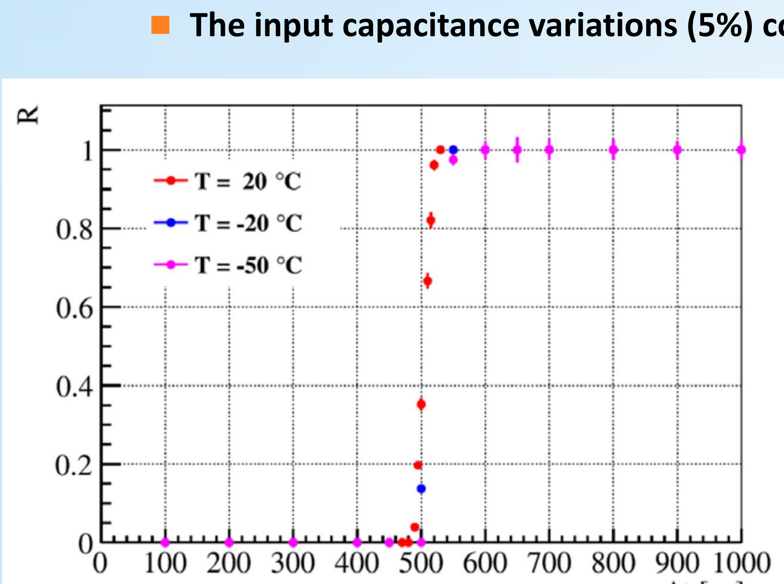


Fig. Deadtime Measurement with Charge injection

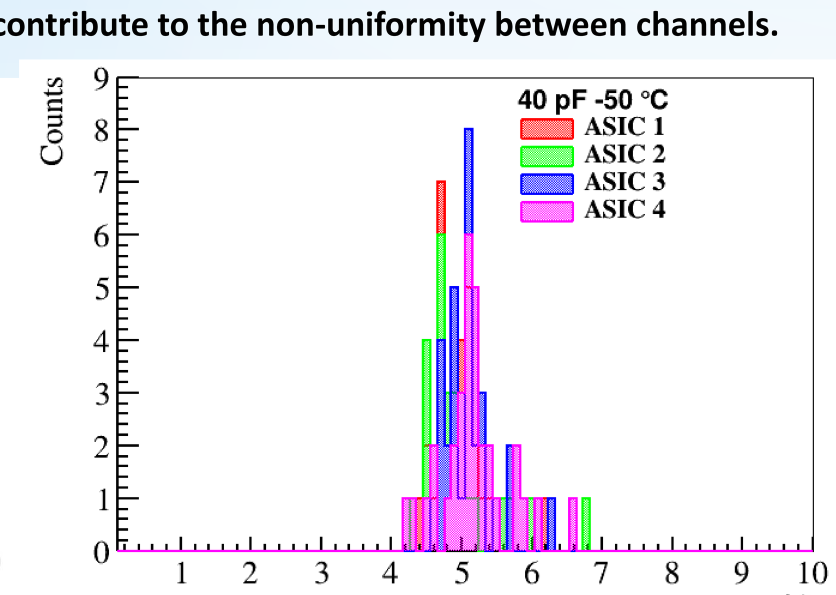


Fig. ENC Measurement with 4 ASICs

- The dead time of the KLauS chip is less than 600 ns, which meets the requirement of 1 μs for IBD detection.
- Small Equivalent Noise Charge ENC = 4.5fC， which Meets the requirement that ENC must be less than 0.1 p.e.

Performance Measurement With SiPMs

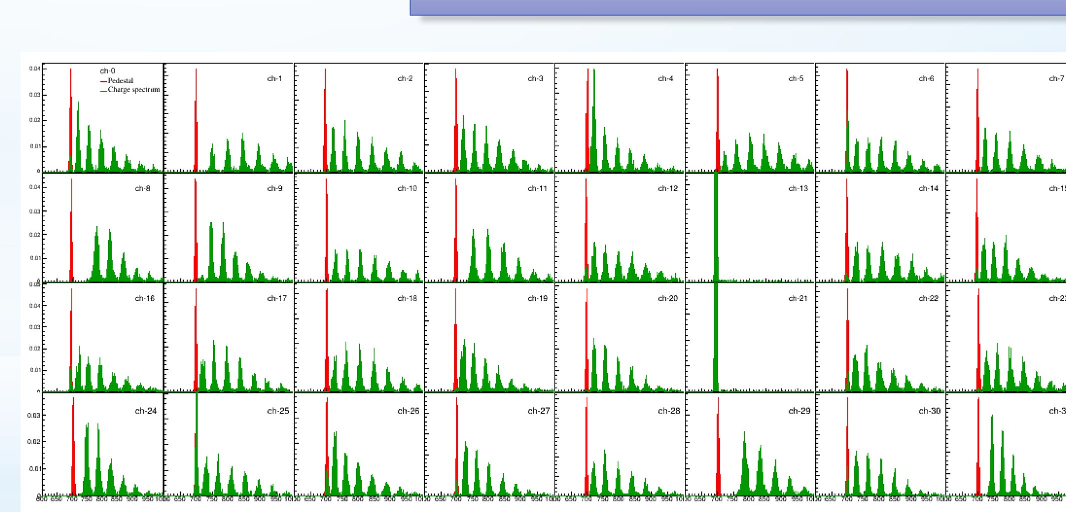


Fig. HG charge spectra at -50 ℃, OV ~2.5V, HG (1:1), Channel 0 - 31

- 8 x 8 SiPM elements, 6 mm x 6 mm for each
- 2 SiPMs are connected in parallel in one readout channel
- Illuminated with a pulsed LED light source on top of the tile
- The same bias voltage is used for all channels
- Charge spectra were measured (HG) both at -50 ℃ and -60℃
- Only results at -50 ℃ are shown, since the differences between -50℃ and -60 ℃ are not significant.
- Clear SPE signals can be observed for all three tested SiPMs from different vendors.

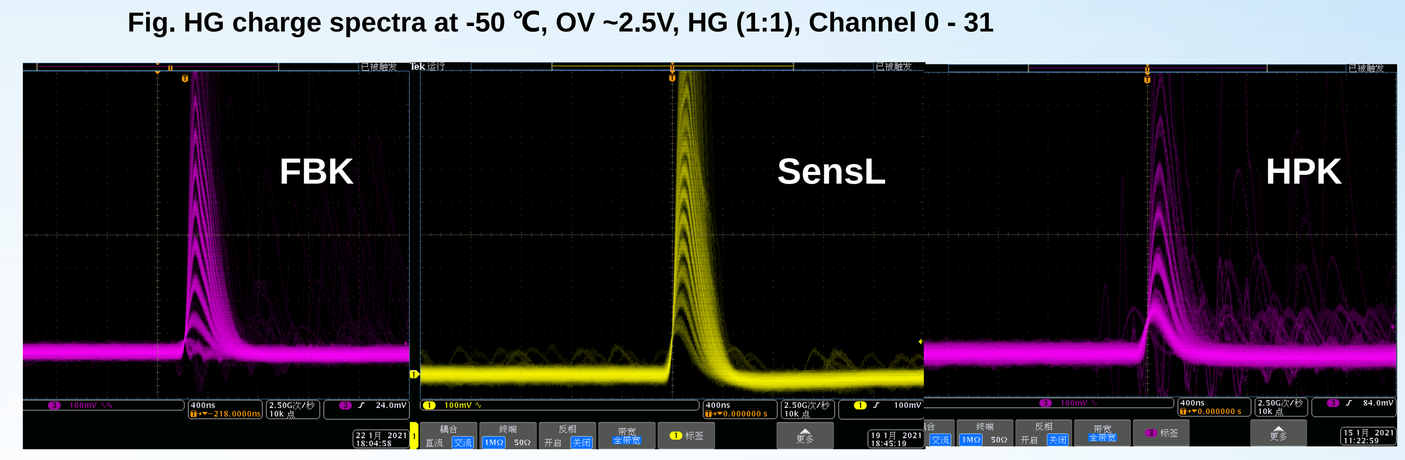


Fig. HG charge spectra at -50℃ with Hamamatsu, SensL and FBK

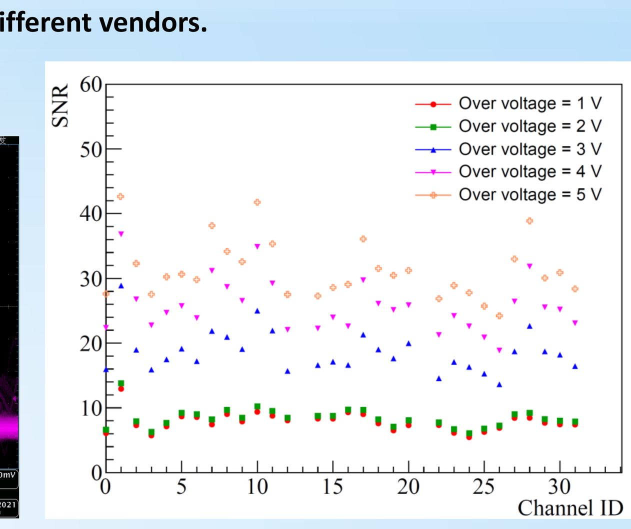


Fig. SNR Measurement with a SiPM Tile

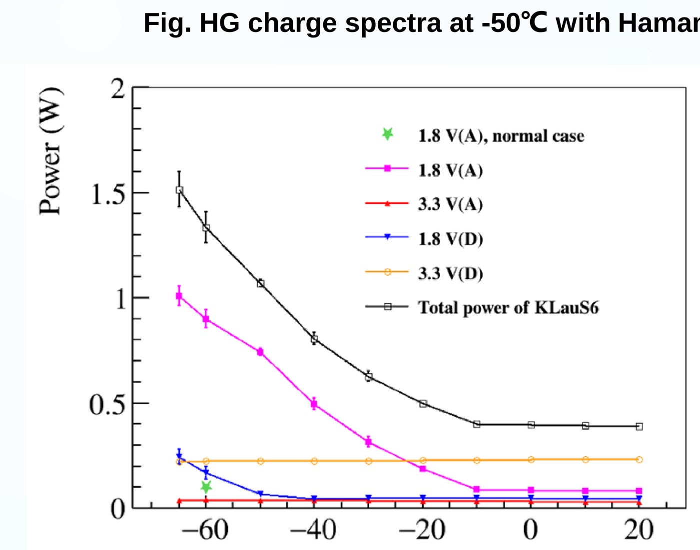


Fig. Power Dissipation

- The testing results of the ASIC readout prototype look quite promising at low temperatures.
- It has been proved that the design of the ASIC readout scheme is solid and robust.
- The performance of the KLauS6 chip can meet TAO's requirements.
- The power dissipation is increased at low temperatures, which induced a potential risk on long term reliability. But it has no effect on the performance of Klaus6.