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# Design of the ASIC readout scheme for the JUNO-TAO experiment

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One of the main objectives of the Taishan Antineutrino Observatory (TAO) is to accurately measure the reactor neutrino energy spectrum to provide precise input to the Jiangmen Underground Neutrino Observatory (JUNO). In this study, we designed a full potential readout system for TAO based on the Klaus6 chip.We also developed a mockup prototype based on the design, which includes 4 chips (up to 128 channels). The performance of the prototype has been carefully evaluated both at room temperature and at -50 ℃. Good performance is obtained on gain uniformity, charge linearity, equivalent charge noise, dynamic range, and recovery time.

## Summary (500 words)

The TAO detector requires 4024 SiPMs to be installed, so a large number of readout channels are needed in the electronics section. Compared with usual discrete readout systems, using ASICs as SiPM readout systems has the advantages of high integration and good performance, which can simplify the design of the whole electronics readout system.

In order to meet the requirements of the TAO experiments on electronic charge noise, time resolution, dynamic range, power consumption. We investigated many current ASIC chips that might be used as SiPM readout. In this paper, we show the comparison of these chips in terms of these parameters and introduce the performance of the Klaus6 chip finally selected in detail.

This paper designs a complete ASIC readout system for the TAO detector, mainly divided into two parts: Front-End Board (FEB) and Front-End Controller (FEC). FEB is used as front-end interface board for SiPM, which has a Klaus6 chip and a high voltage connector to provide bias voltage to the SiPM. Every four FEBs are cascaded together (up to 128 channels). On the last FEB, the HDMI connector, power distribution network, configuration bus and readout driver are designed. FEC is used for control and readout, which consists of the Front-End Electronic (FEE) board and the Rear Transfer Module (RTM) board, which are connected through the backplane connector and placed in the Micro-TCA (Telecom Computing Architectrue) chassis.

In addition, this paper designs an ASIC readout prototype system and introduces it from both the hardware and software aspects. The performance of the prototype has been carefully tested both at room temperature and at -50 ℃. The results show that KLauS6 has good performance at the tested temperatures with no significant degradation of the charge noise, charge linearity, gain uniformity and recovery time, all of which meet the requirements of TAO.

Therefore, this ASIC readout system has very good application prospects and can serve as an important references for many similar experiments.

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