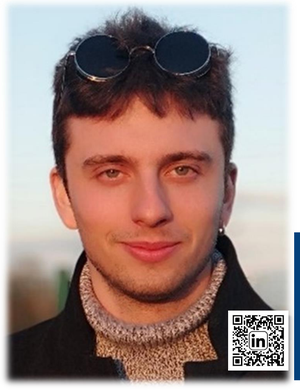
CMS HGCAL Vertical Integration System Tests



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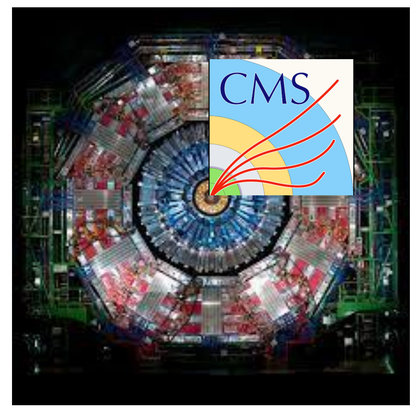
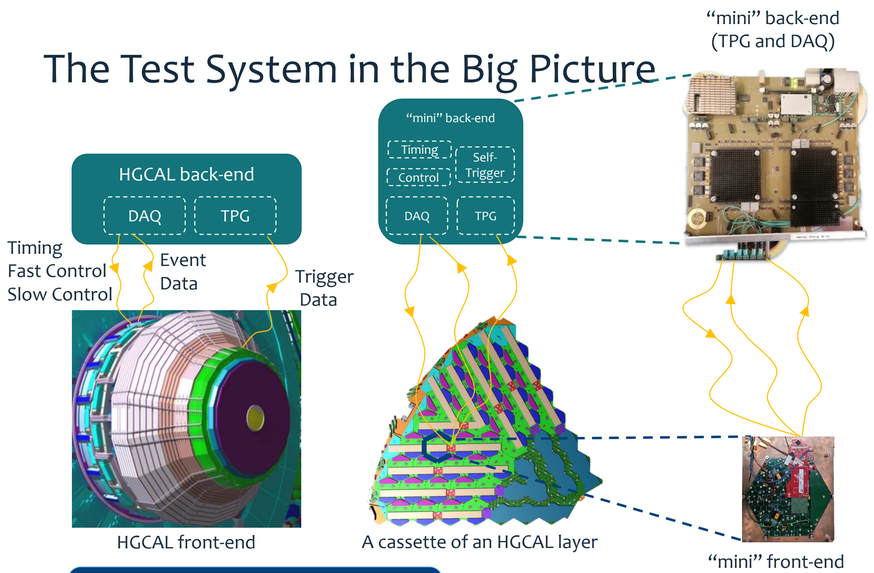
On behalf of the CMS Collaboration

TWEPP 2023

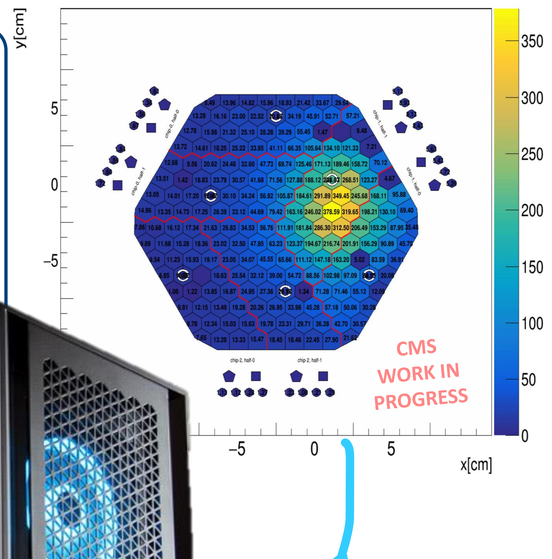


The Test System in the Big Picture



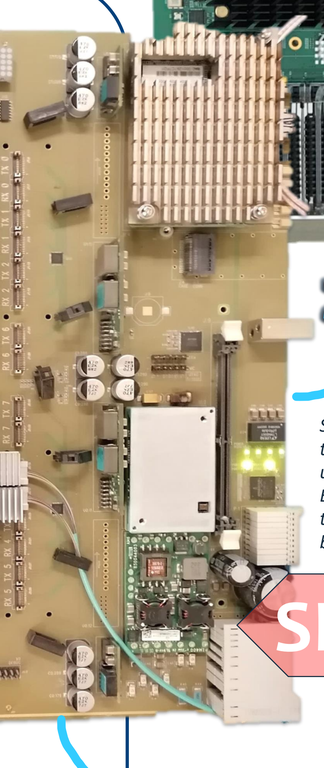
Abstract

In preparation for the High-Luminosity era of the LHC, CMS will replace the existing calorimeter endcaps with a novel device - the High Granularity Calorimeter (HGCAL), which will have around **six million readout channels**. Given the scale and complexity of the endcap upgrade project, **the electronics testing must be carefully planned.** The strategy has been **to split the efforts between vertical (start-to-end) and horizontal (parallelisation) test systems** wherever possible. An important milestone is the development and operation of test systems to **prototype one vertical slice** of the future endcap electronics system**. For the first time** (and just a few days ago) we returned from a beam test where we used **the full vertical electronics chain** to acquire **real data!**



Motivation

The test system at CERN consists of front-end hardware with **real ASICs and back-end boards** running custom firmware and software. In addition, it is split into its respective **TPG (Trigger Primitive Generator) and DAQ** paths in both cases. The main goals are to test various kinds of data exchange between the front-end and the back-end, specifically the **timing distribution, slow and fast control, and acquisition of trigger and event data**, across all the relevant interfaces. Success in these activities allows the project to move towards horizontal system scaling.



System Operation

Timing Distribution

- The Serenity DAQ back-end reliably distributes the 40 MHz clock embedded in the fibre-optical link to the front-end.
- Measurements show that **the jitter** in the system **meets the specification requirements, i.e. TIE ~ 8.5 ps < 15 ps.**

Slow Control

- The Serenity DAQ back-end performs slow control (i.e. configuration and monitoring) of the front-end ASICs .
- **Able to reliably read from and write to any ASIC register in the front-end.**

Fast Control

- The Serenity DAQ back-end generates and distributes various fast commands (i.e. Level-1 Accept, Idle, etc.) to the front-end chips.
- **Able to reliably send a variety of fast commands to the front-end and confirm their proper reception by receiving ASIC responses as per design.**

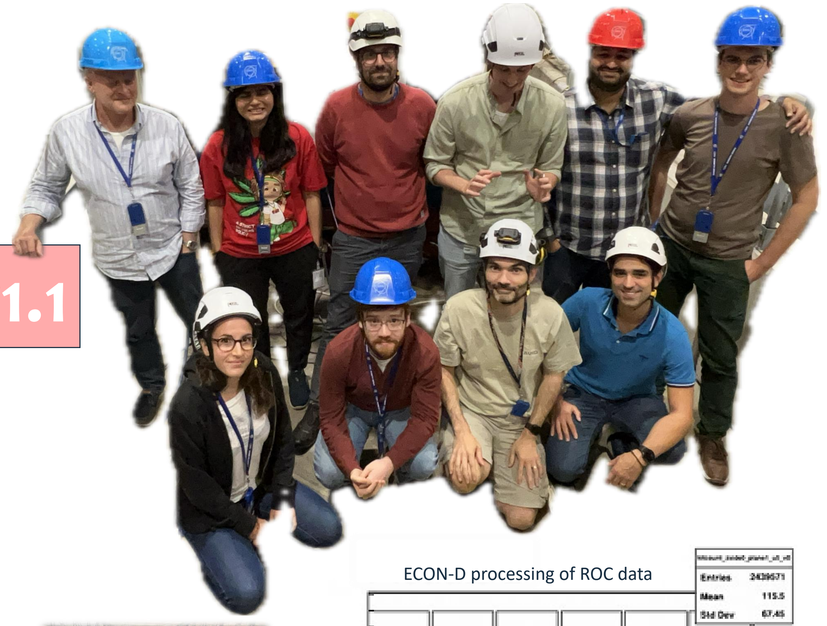
Data Acquisition

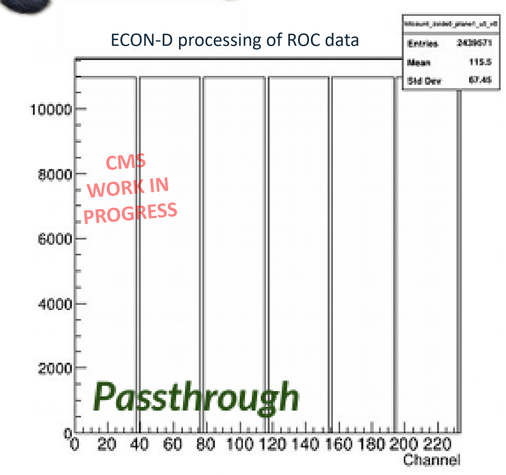
- **Able to transmit trigger and event data through** the **entire sequence of front-end chips** that filter, format, and error-protect them.
- **Able to bring both trigger and event data through the back-end processing chain:**
  1. **SERENITY (TPG and DAQ) back-end**
  2. **DTH400**
  3. **DAQ PC for permanent storage**

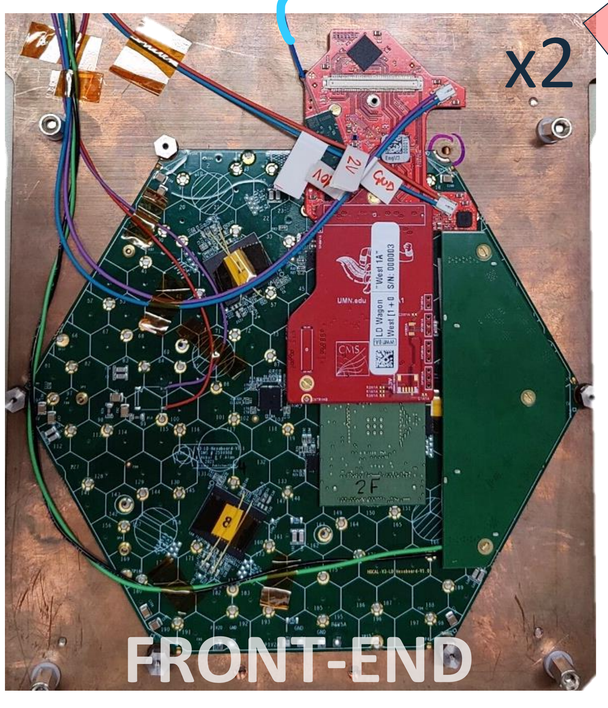
where they are **captured, unpacked and combined, precisely meeting** the **expectations** w.r.t. the FE chip configuration.

- Depending on the particle beam type (i.e. particle type and particle energy) and system configuration (i.e. algorithm choices in ECON ASICs) **the rates of events** during particle spills would be as high as **O(100 kHz)**, generating up to **O(1 Gbit/s)** worth of **data rates**.
- The system was able to reliably acquire up to **O(100M)** events in long (overnight) **runs** without expert supervision.

See R.Shukla's talk about unpacking the ECON-T data in the Serenity back-end







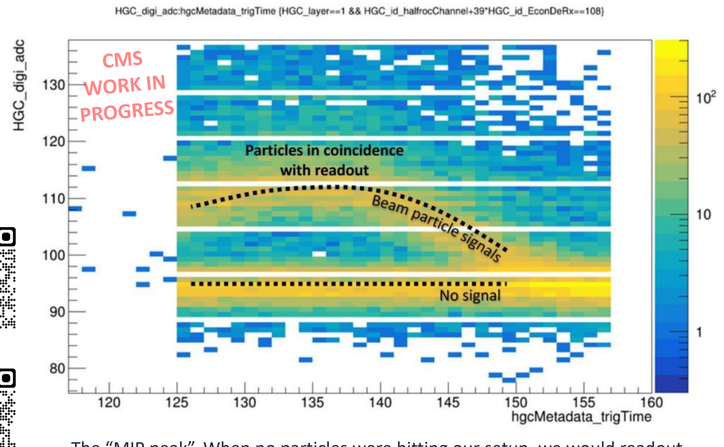
2x Si Train

- **Engine V3 and Wagon PCB**
  - **1x VTRX+ ASIC**
  - **3x lpGBT V1 ASIC**
  - **1x LDO**
- **ECON Mezzanine PCB**
  - **1x ECON-T- P1 ASIC**
  - **1x ECON-D-P1 ASIC**
- **Hexaboard PCB:**
  - **3x HGCROC V3 ASIC**
  - **1x Rafael ASIC**
  - **Si Modules biased with -270 V**
    - **1x 300 µm**
    - **1x 200 µm**
- **DC-DC Converter**

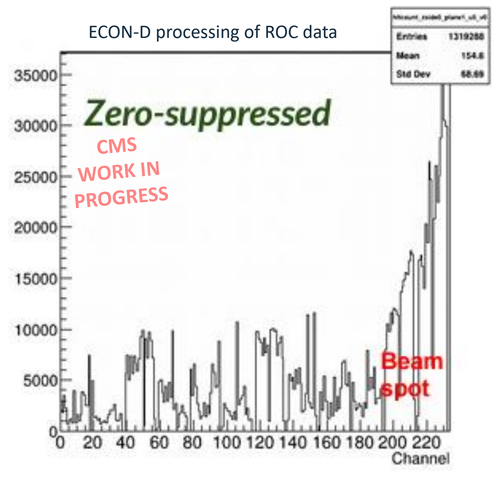
See C. Mantilla's talk for details on standalone ECON testing

See F. Khan's talk on timing performance of Si modules

See J. David's talk on H2GCROC3s



The "MIP peak". When no particles were hitting our setup, we would readout a base ADC count level from the silicon sensors. That corresponds to the horizontal yellowish line in the ADC versus time plot below. However, when shooting a beam of pion particles into our detector, another shape is expected to emerge – the so-called "MIP peak", as high as about ~20 ADC counts above the noise level. Why? The detector is synchronous to a 40 MHz clock and the beam particles can arrive at any random time with respect to that. Hence, the particle signal is maximum at the right phase and smaller whenever the particles are not in coincidence with the sampling clock.



The above two plots nicely summarise how the zero suppression is working using the ECON-D ASIC. These plots show how many times the signal recorded in hexaboard channels were passing the threshold. When we are in pass-through mode, we see signals coming from all the channels (top plot). When in zero suppression mode (bottom plot; pass only if signal > certain threshold) signals only from some channel do pass through.

Conclusion and Future Work

The components (i.e. PCBs and ASICs) of this system are usually products that **came from completely different parts of the world** and have **only** been **tested** in their home institutes **standalone**. Moreover, the **experience of** assembling one such setup and **getting all these devices to work together was very limited.** Nevertheless, over the past couple of years, **most** of the **interfaces** have been **tested** and the **full chain of Timing, Slow Control, Fast Control and data acquisition was shown to work** in a realistic environment (i.e. beam test)**.**

The future goals are to expand to **service several copies of the front-end** test systems **in parallel, prepare the system for production cassette testing.**