

System-level Tests of Large-scale Multi-module Prototype Structures of the ATLAS ITk Pixel Detector

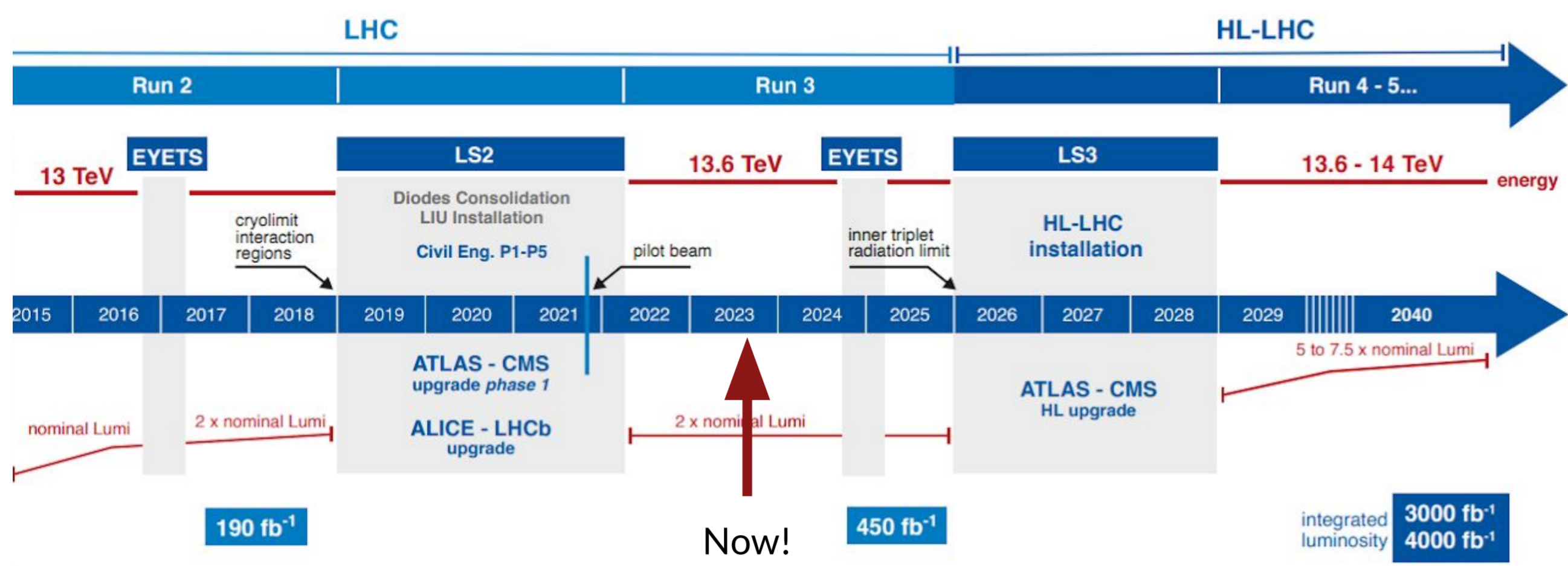


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On behalf of the ATLAS ITk Collaboration

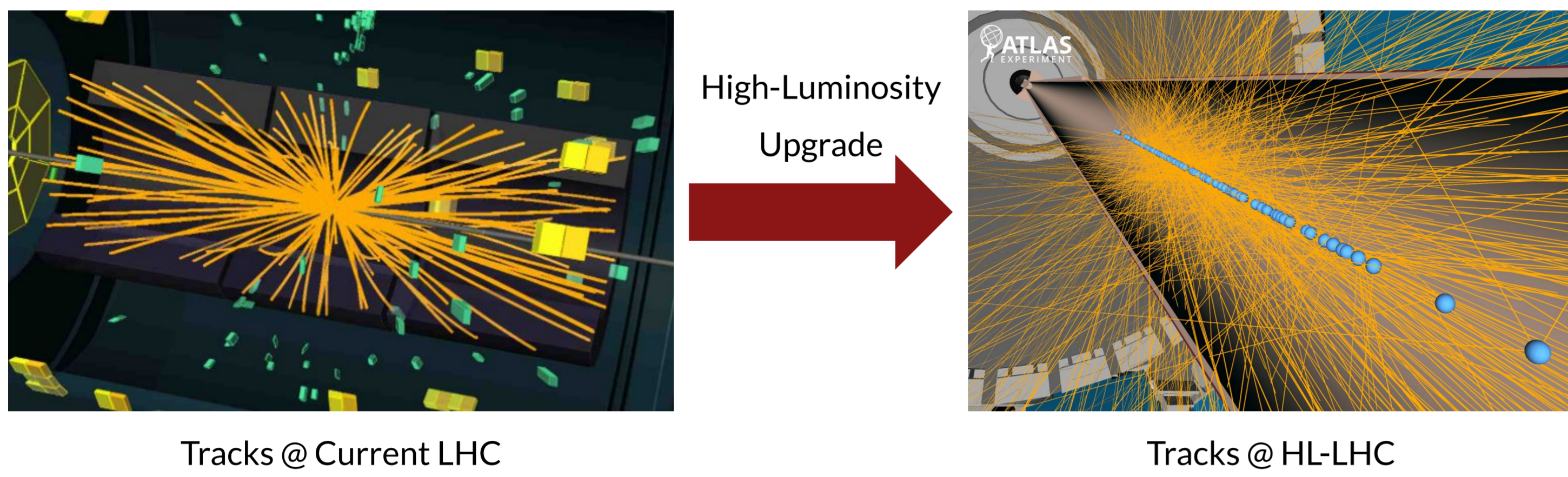


ATLAS Inner Tracker in High-Luminosity Era



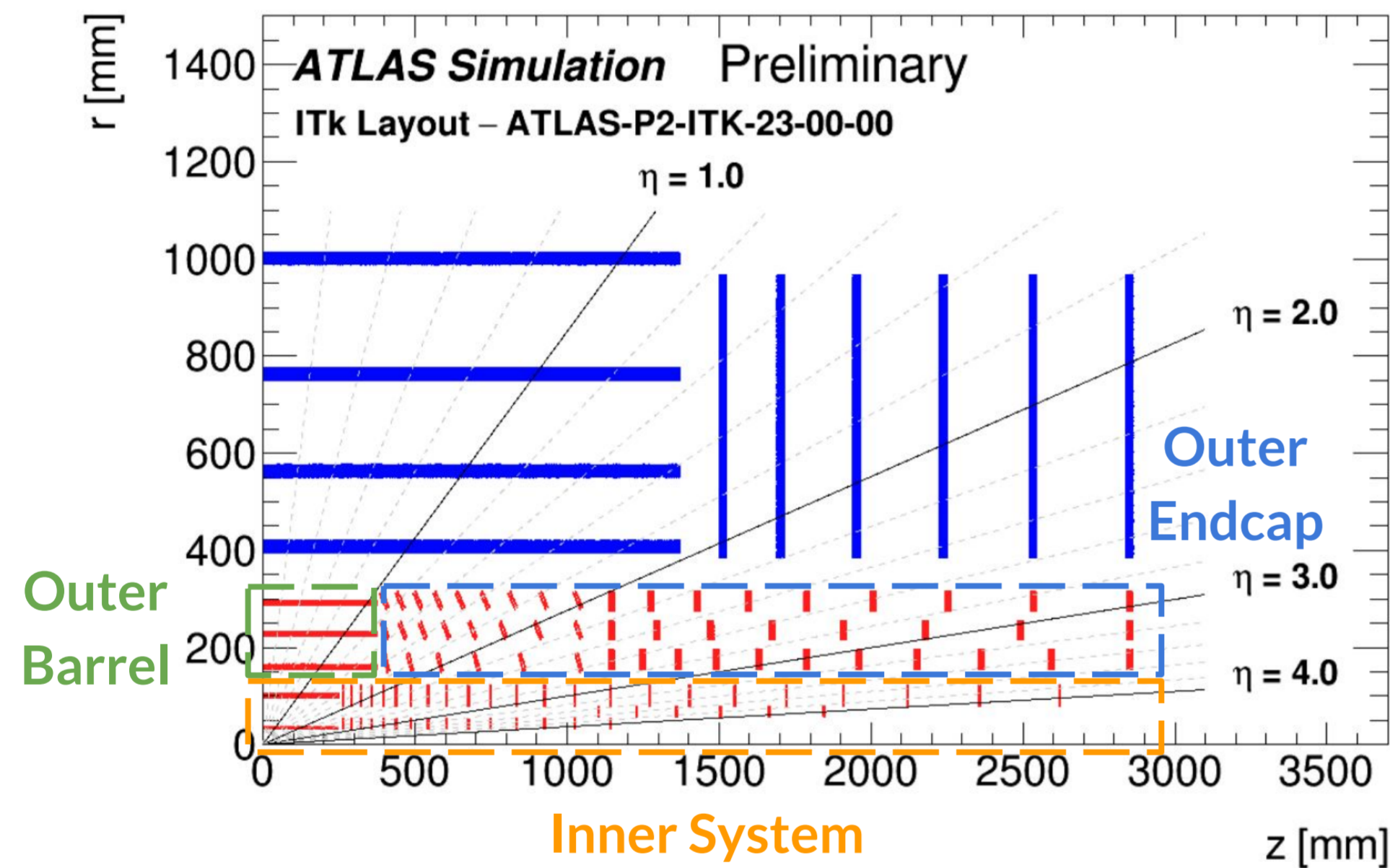
High-Luminosity LHC (HL-LHC)

- HL-LHC will produce beams with luminosity over 3x higher than current LHC
 - Instantaneous: $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \Rightarrow 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
 - Integrated: up to 4000 fb^{-1}
 - Interactions / event: $\langle \mu \rangle \sim 50 \Rightarrow \langle \mu \rangle \sim 200$
- Physics run in 2029, scheduled out to 2040
- More pp collisions, more physics opportunities!



New ATLAS Inner Tracker (ITk)

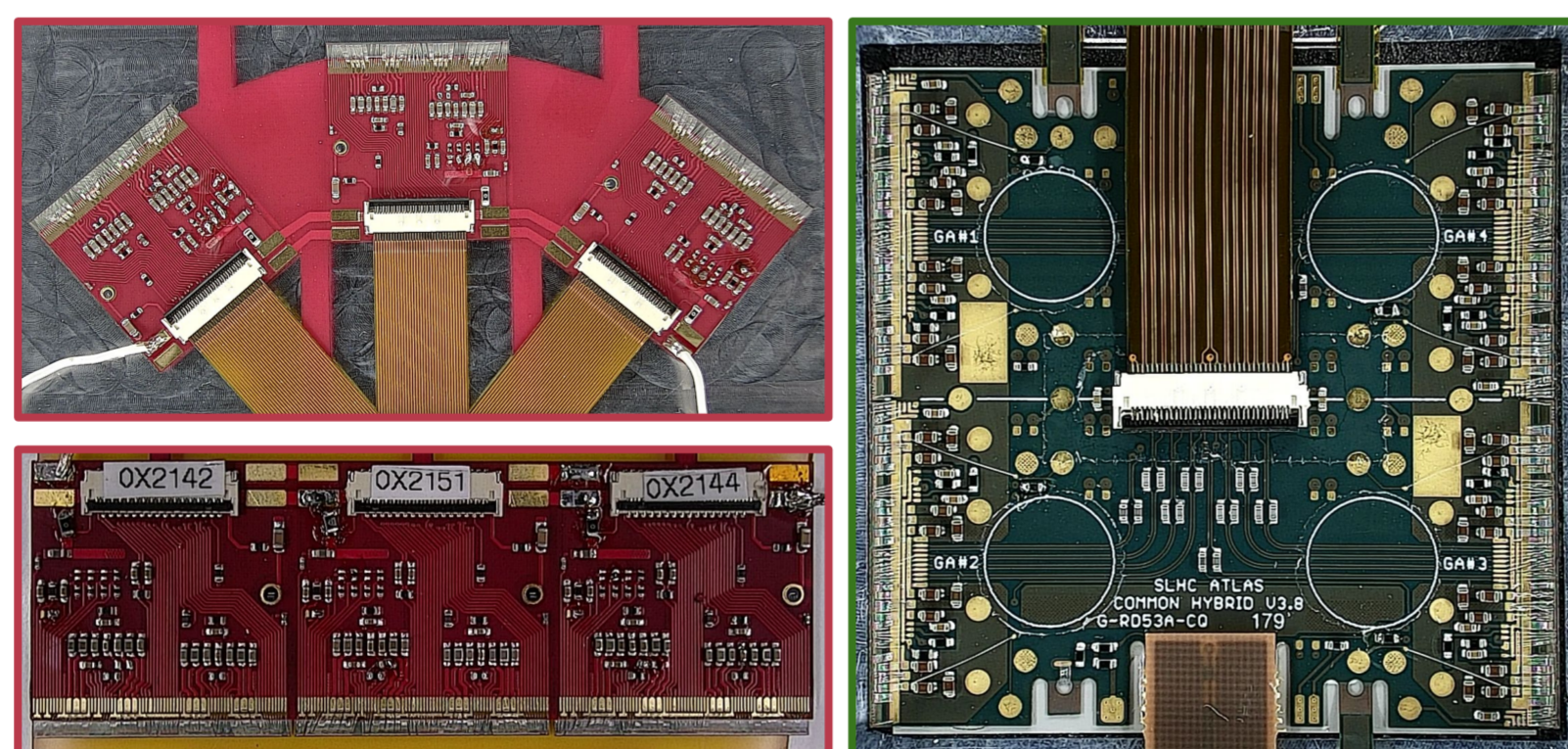
- Resolve and reconstruct more particles per event
 - More layers and higher granularity than current ATLAS Inner Detector
 - Pixels:** 13 m^2 total area, 5 layers (in barrel)
 - Strips:** 165 m^2 total area, 4 layers (in barrel)
- Radiation hard up to $2 \times 10^{16} \text{ n}_{\text{eq}} / \text{cm}^2$ fluence
- Inner System will be replaced after 2000 fb^{-1}



ITk Pixel Prototypes—Inner System

Prototypes built with RD53A pixel modules

- Module = sensor + front-end (FE) chip
- Two flavors:
 - Triples:** 3 sensors & 3 FE's
 - Quads:** 1 large sensor & 2×2 FE's
- 400px x 192px with 3 different FE designs
- Data transmission up to 1.28Gbps per FE
- Serial-powered from constant current source (Shunt-LDO regulator)

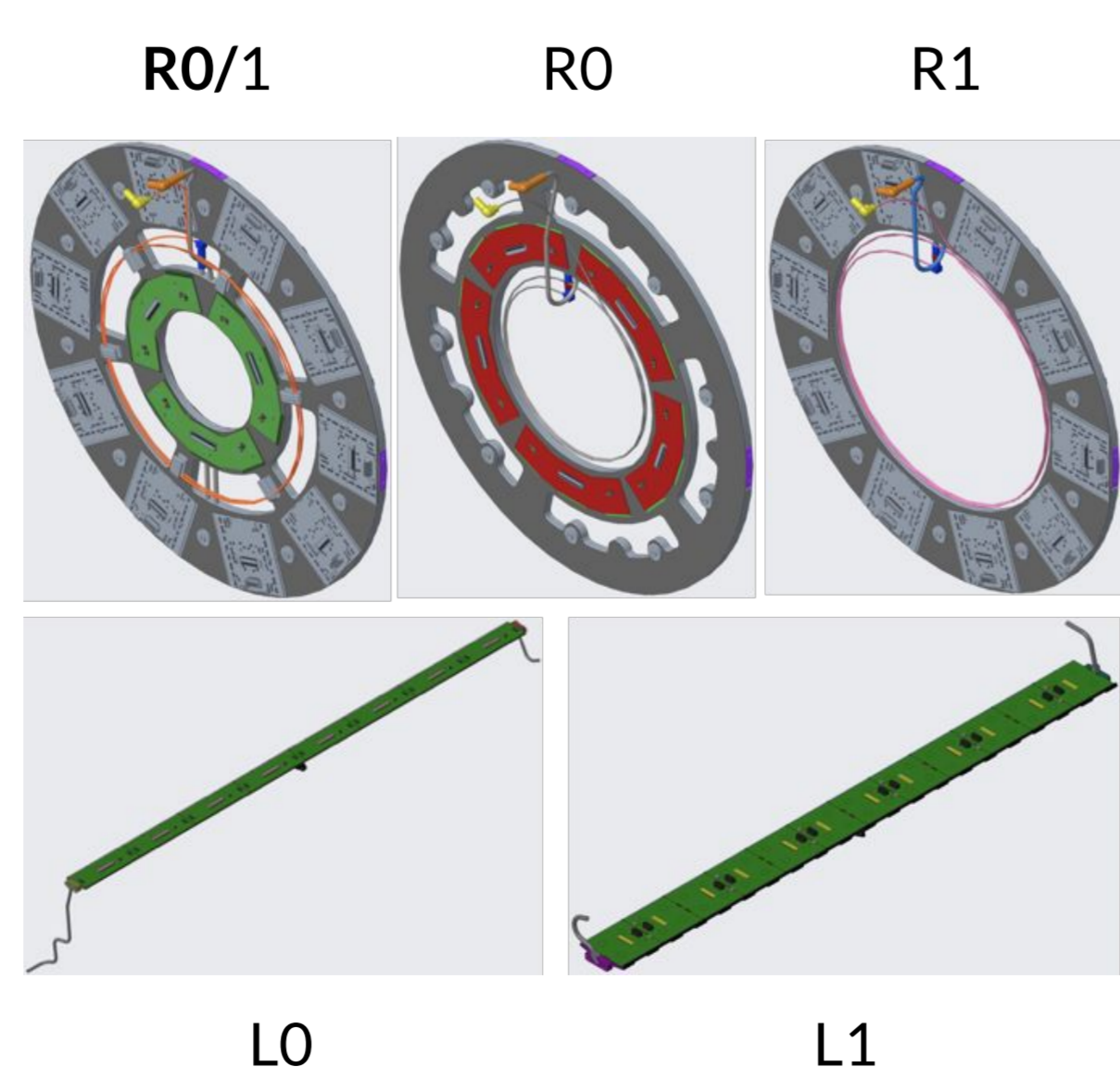


Building the ITk Pixel System

- Load modules onto local supports
 - Carbon fiber structures
 - Staves for barrel region, rings for endcap region
- Connect various flexes and electrical services

Testing the ITk Pixel System

- Test module performance at each step
 - Production → Reception
 - Loading → With proper services
 - **Connectivity, digital scans, disconnected bump-bonds (discBB), etc.**
- Verify thermal performance
- Verify serial power chain

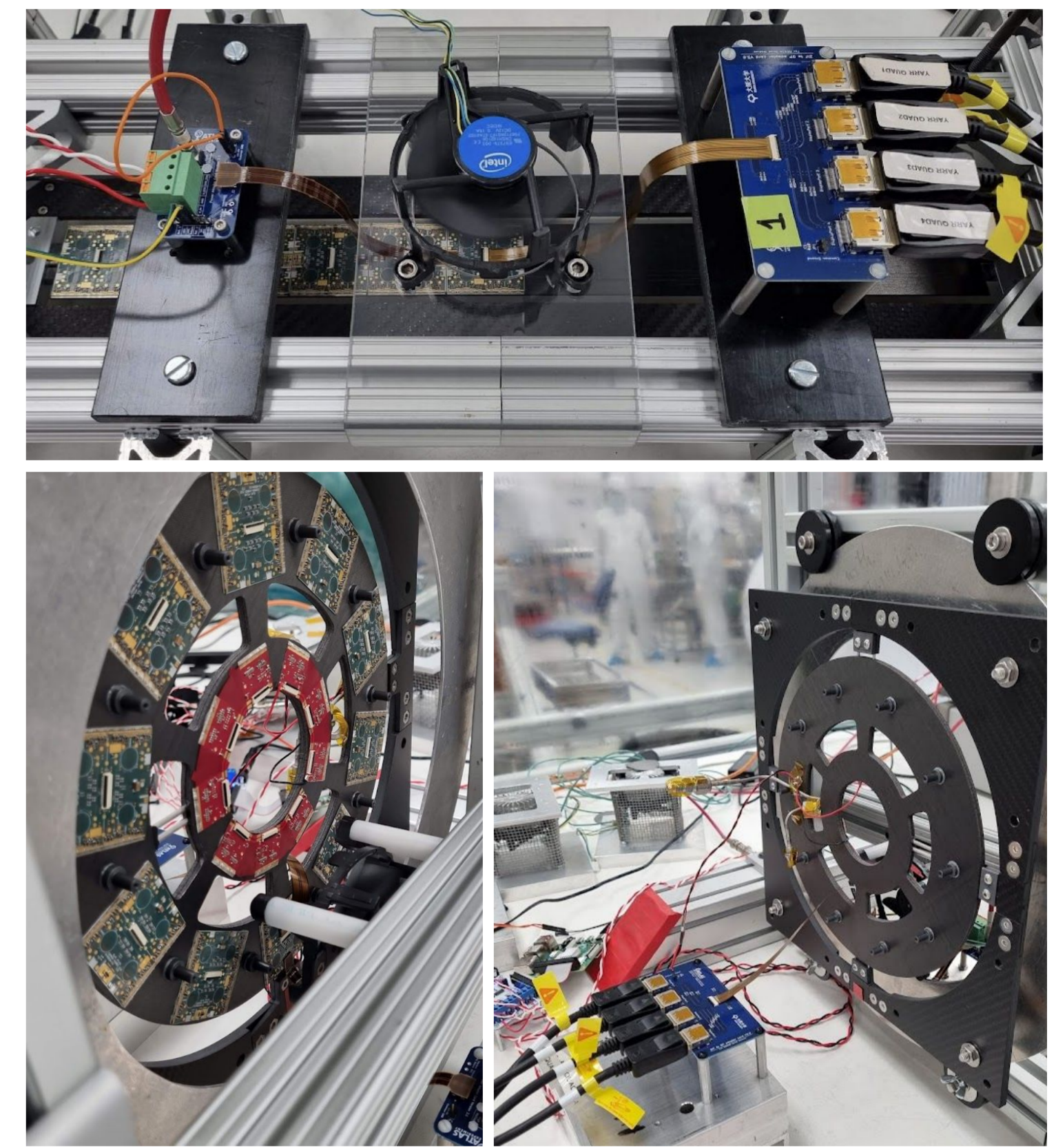
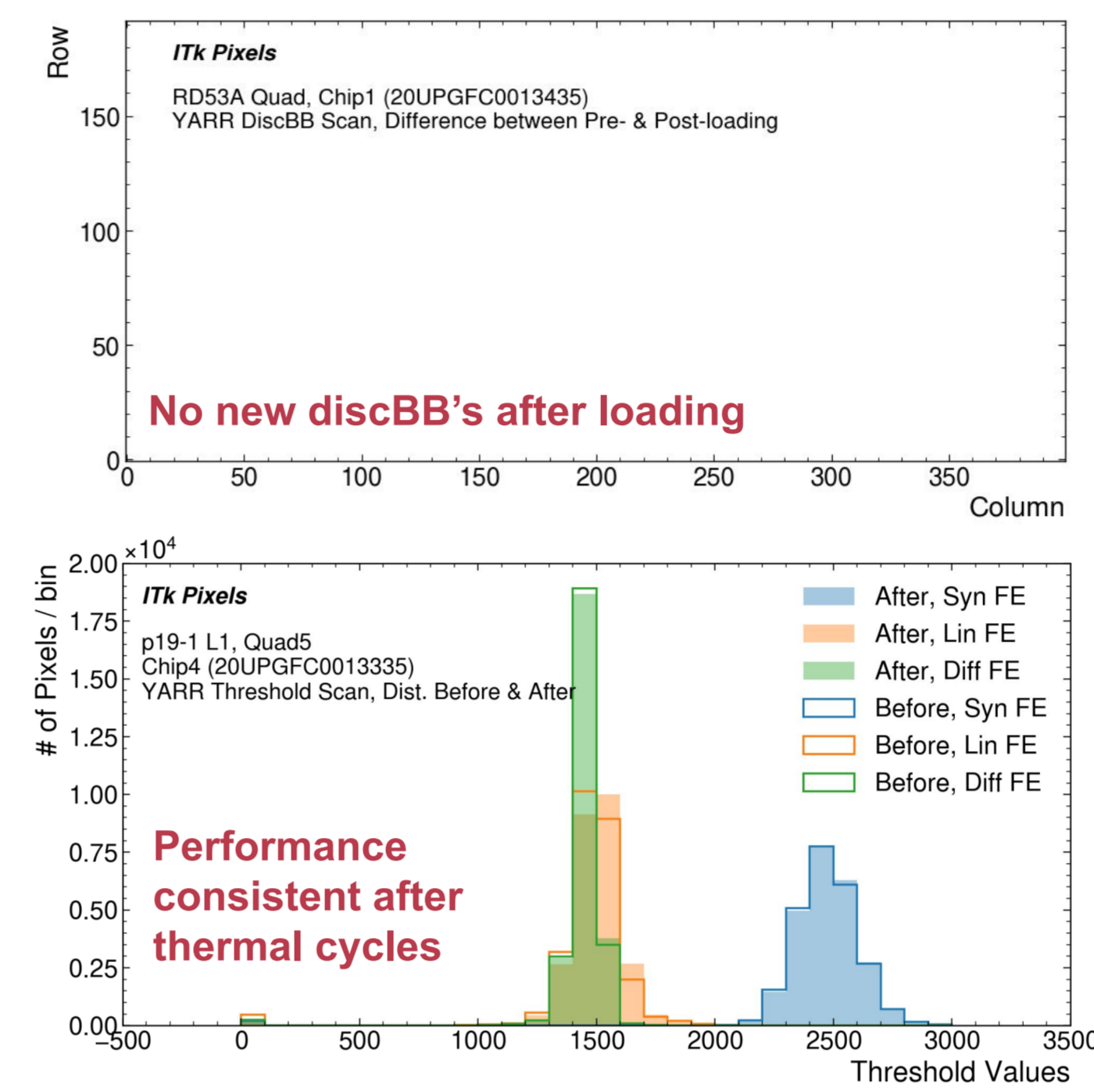


5 Flavors of Inner System Structures

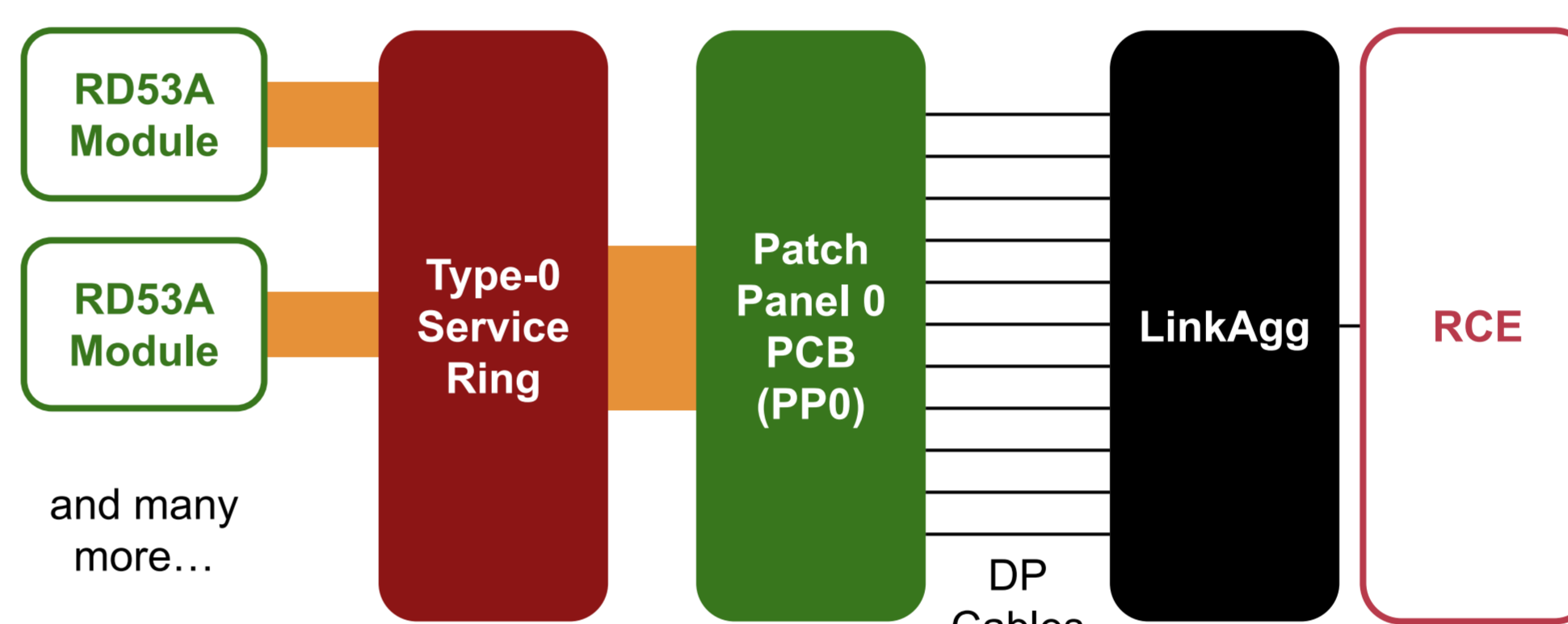
Testing Loaded Local Supports

Testing after Loading

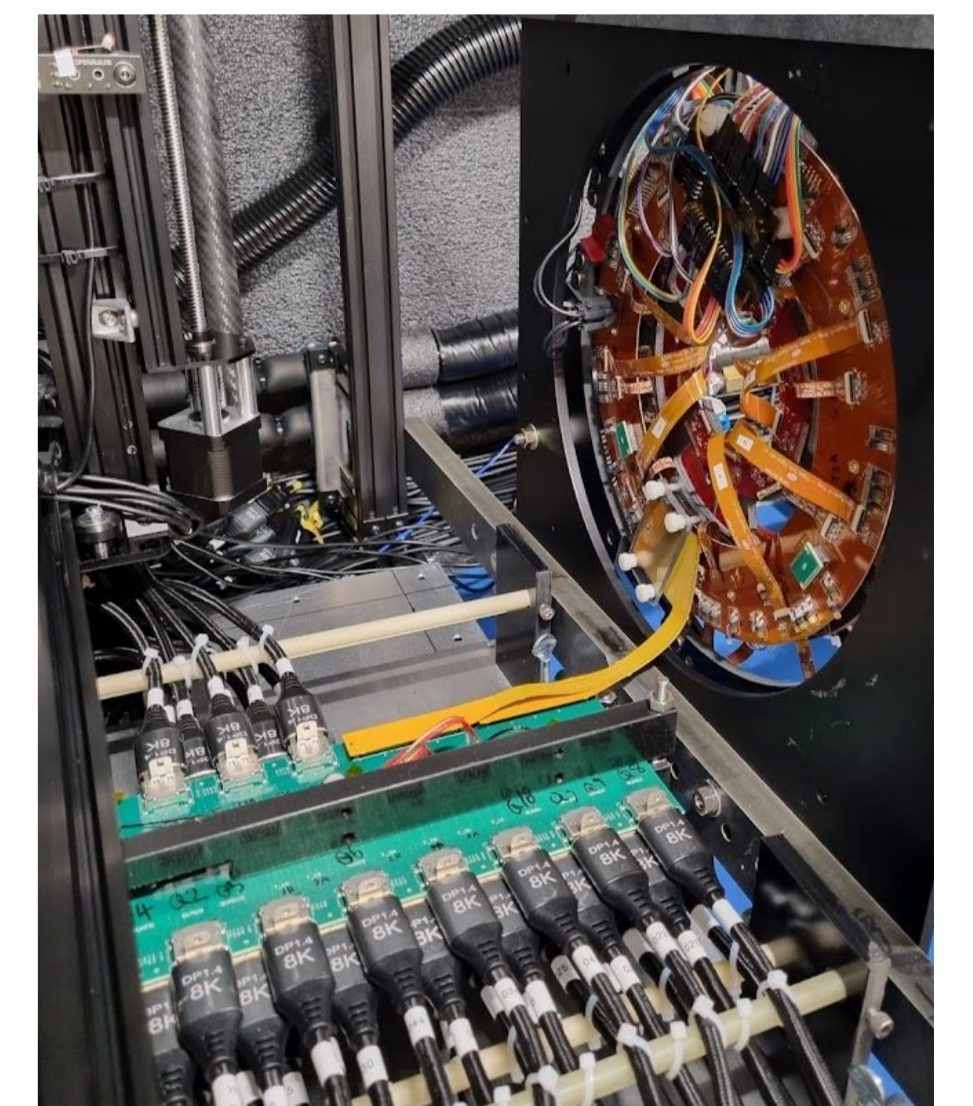
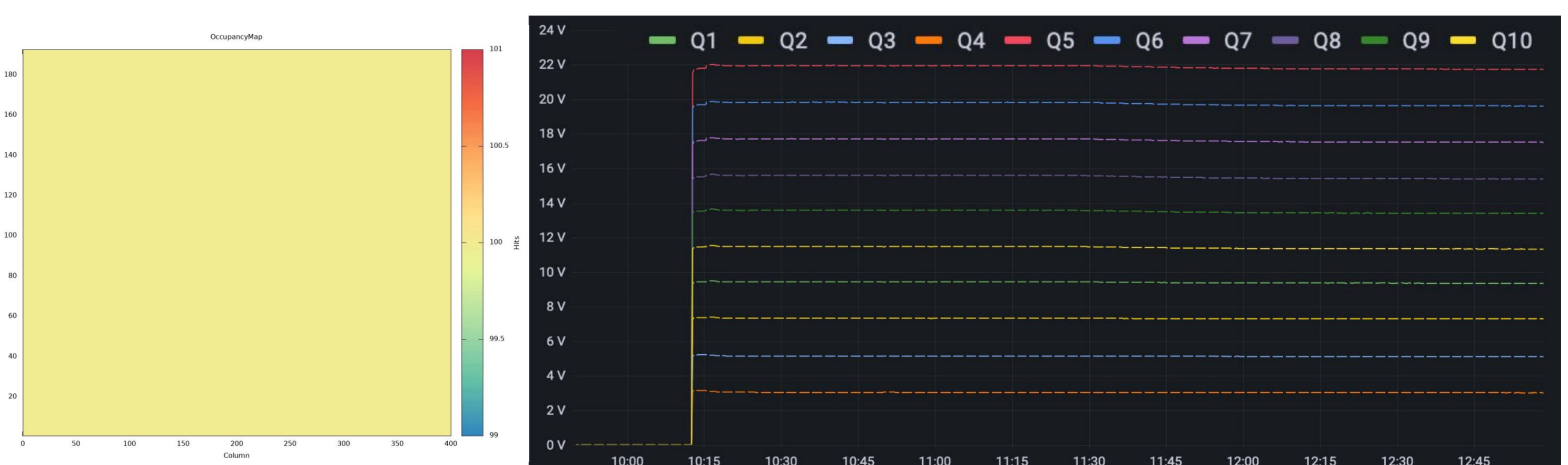
- Loaded modules are individually tested to assess any damages during loading
 - No performance degradation, no new discBB's found
 - Loading procedure is well-established and safe!
- L1 stave has been tested through thermal cycles
 - Total of 100 cycles from -55°C to 20°C at LBL
 - Tested after 1, 34, 67, and 100 cycles
 - No performance degradation, no new discBB's



Testing with Prototype Electrical Services



- R0/1 ring connected to prototype type-0 and PP0
- Testing one chip at a time
 - Read-out with YARR, customized for full-speed (1.28Gbps)
 - Results look consistent with previous tests
- Verifying serial powering scheme
 - Constant current supply @ 4.6A \Rightarrow $\sim 2\text{V}$ / quad module
 - Demonstration of properly regulated SP chain



Future Work

- We are now in pre-production!
- Test L0 & L1 staves with their appropriate services
- Infrastructure upgrades
 - Improving CO₂ cooling tower
 - Implement more realistic DCS/interlock system
- Multi-module read-out scheme in development
 - Multi-module control software ready, but need firmware modifications
- Integrating multiple local supports into quarter-shell system
 - Active mock-up's in progress
 - Planning integration strategy & providing design feedback
- Multi-sub-system "slice" test @ CERN, planned for 2024

