New Electronics for the HADES MDC Drift Chambers

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for the HADES collaboration
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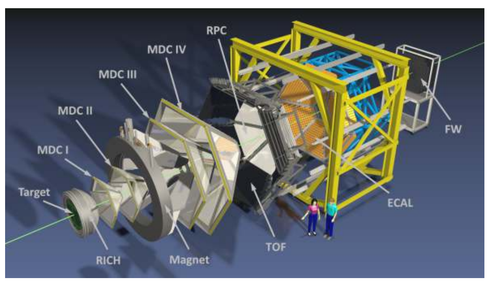
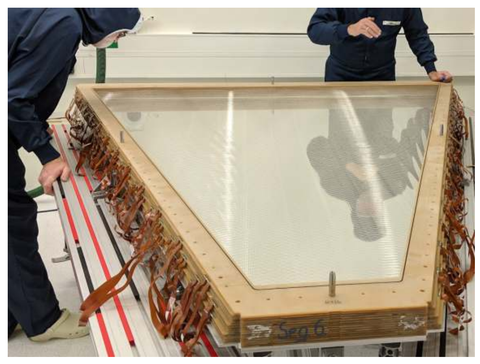
The HADES detector



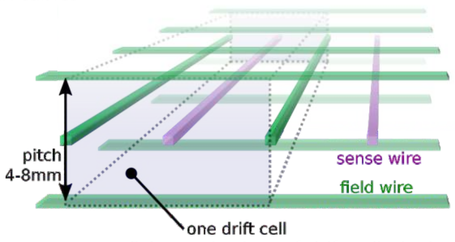
- operational since 2000 @ GSI, Darmstadt
- light and heavy ion or pion collisions in the 1 - 4.5 AGeV range
- up to 50 kHz trigger rate
- ~ 80,000 discrete detector channels
- mini-cell drift chambers as main tracking device



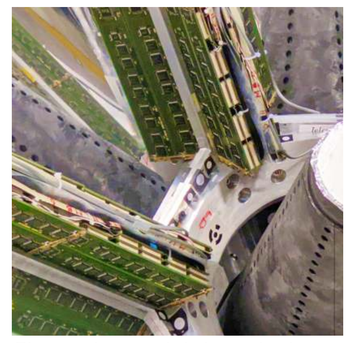
Drift Chambers

- 24 chambers with up to 3.2 m² active area each
- 6 layers of drift cells at 5 different stereo angles per chamber
- small drift cells below 1 cm side length for good position and double track resolution at high occupancies
- dE/dx measurement for particle identification
- 150 µm spatial precision per cell

One of 24 chambers during inspection in clean room. Electronics to be mounted to brown flex cables



Schematic view of drift cells / wire arrangement



Electronics are tightly packed between active detector volumes

Current MDC Electronics

- increased failure rates after 20 years of operation
- strongly fluctuating power consumption
- limited rate capability / slow data transfer
- electric contact and mechanical stability issues

Design Constraints

form factor fixed: position of connectors constraint within 1 cm w.r.t. chamber

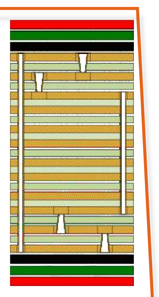
low noise requirement: no switching regulators allowed on front-ends

discharge protection: kV sparks in chamber

strict size limitations: must fit into insensitive detector spaces

limited heat dissipation: cooling of packed spaces between detectors with air difficult

PCB Design



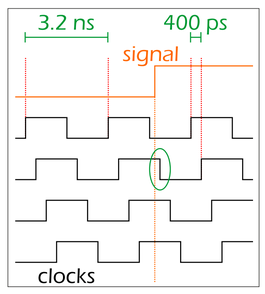
- 4 cm width constraint
- spatial separation of sensitive analog and fast digital signals needed
- 4 global and 11 local voltage rails
- BGA components with mainly differential I/O
- more than 800 components

➔ 12 layer board with 2 layers of blind vias

- detector design asks for two types of boards, with 64 and 96 inputs, respectively

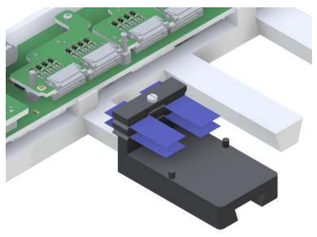
Time Measurement

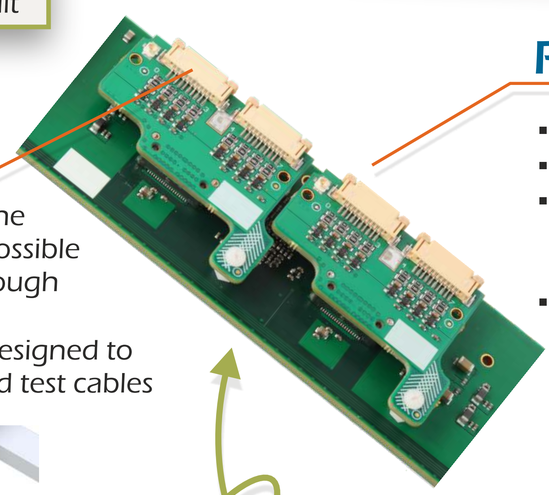
- intrinsic detector precision is above 1 ns
- clocked TDC approach: sample signal with several phase shifted clocks
- 312.5 MHz times 8 phases for 400 ps mean bin width
- non-perfect bin sizes due to routing tolerances of ±20%
- effective measured time precision 140 ps rms



Testing Tools

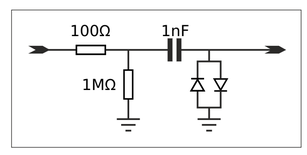
- a thorough testing of the readout chain is only possible by injecting signals through FPC inputs
- a special jig has been designed to efficiently plug and hold test cables



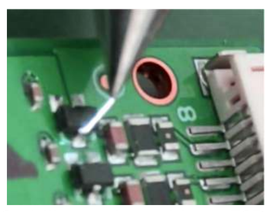


Passive Input Stage

- connectors for 4 FPC cables
- AC coupling, discharge resistor
- has to withstand 2 kV, 5 nF discharges without hampering signal quality
- board shape due to space constraints: optical fiber, flex cables, mounting holes, handling



Signal input stage



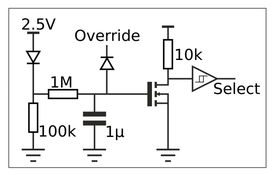
Stability testing with an ESD spark gun to simulate discharges in the detector

FPGA Platform

- Lattice ECP5-45 FPGA
- 1 communication FPGA: optical link to DAQ system, monitoring
- 2-3 TDC FPGA: 32 channels each, data and event handling, spike rejection
- common HADES TrbNet protocol for triggering, data transport and FEE control

Dual Boot

- firmware can be upgraded remotely while installed in inaccessible spaces
- two ROMs hold two versions of firmware for increased reliability
- simple analog timing circuit switches ROM after 2 s power on and 10 s off

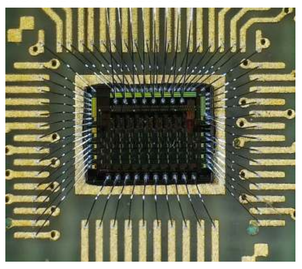


Auto-Config

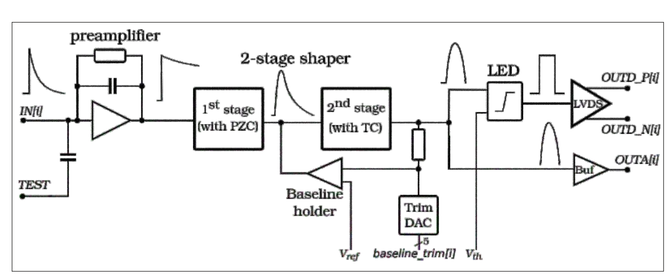
- automatic loading of all settings from internal Flash at power-up
- including ASIC configuration, thresholds and shaping parameters, FPGA configuration, network addresses

PASTTREC ASIC

The PASTTREC ASIC, bonded to a test board



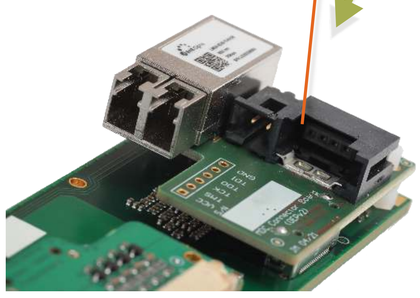
- amplifier, shaper and discriminator designed for drift cell detectors
- developed in Krakow for the PANDA Straw Tube Tracker project
- 8 channels per ASIC
- 35 mW/channel
- 8x8 mm² QFN housing
- adjustable gain, peaking time, tail cancellation and threshold
- further information in 10.1016/j.nima.2015.09.102



Signal input stage of the Pasttrec ASIC including amplification, signal shaping and discrimination stages. Most parameters are configurable at run-time (from: PASTTREC ASIC documentation)

Connectivity

- external connectors on raised AddOn for easy access and installation
- 2 Gbit optical transceiver (SFF)
- 2 voltage rails with common mode filters
- reference time input (LVDS)

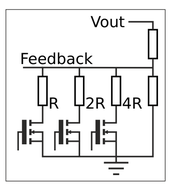


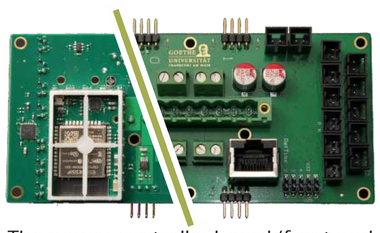
Powering Scheme

- on FEE only linear regulators can be used due to noise sensitivity
- long distance to power supply (10 m)
- strongly varying length of cables
- low voltage drop on FEE needed due to heat dissipation

➔ supply of FEE with 1.4 V & 3.6 V from intermediate voltage regulator board at edge of detector
  - low-noise DCDC converters (LT8650S)
  - adjustable via switchable feedback resistor network

➔ local power dissipation: ~ 6 W / FEE board



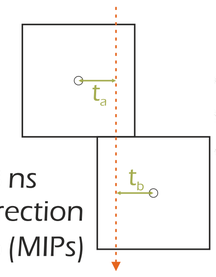


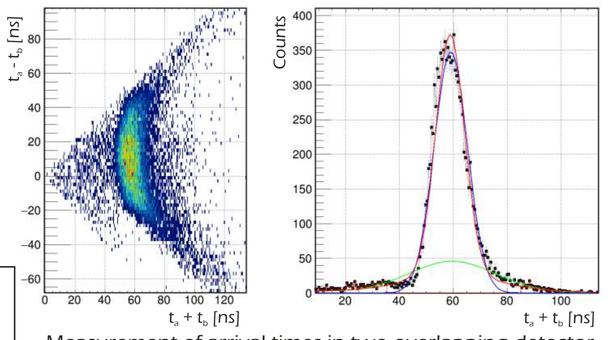
The power controller board (front and back side) with Ethernet connection, power distribution and reference time fan-out

The voltage regulator board (4 channels) with adjustable low-noise DCDC converters

Performance

- the sum of the arrival times of signals in two overlapping cells is a good measure for spatial and time precision
- measurements at COSY, Jülich
- raw timing precision per channel: σ = 3.8 ns before walk correction
- efficiency > 96% (MIPs)





Measurement of arrival times in two overlapping detector cells. Some correctable distortion can be seen close to borders of drift cells

This project makes use of the developments made within the TRB collaboration during the past years contributed by people from various institutes and experimental groups

Poster Download

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TRB collaboration: http://trb.gsi.de

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