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Electronics Upgrade for the HADES MDC Drift Chambers

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The drift chambers of the HADES spectrometer at GSI, Darmstadt/Germany, form its main tracking system. Designed more than twenty years ago, the whole front-end electronics chain is being replaced with state-of-the-art electronics.

The new analog signal processing is based on the PASTTREC ASIC, developed for the PANDA Straw Tube Tracker. The digitization of data happens in FPGA-based TDCs.

The main challenges of the project are the strict spatial constraints given by the experiment setup and the noise sensitivity of the large area gas detectors. In addition, the power consumption needed to be kept low due to thermal constraints.

Summary (500 words)

The HADES experiment is a di-electron and hadron spectrometer at GSI / FAIR in Darmstadt, Germany. Currently it is operated at GSI's SIS-18 synchrotron and is foreseen to be moved to the FAIR SIS-100 accelerator once it becomes operational.

The central tracking part of the spectrometer is formed by the MDC (Mini Drift Chamber) detector. The original read-out electronics were built 20 years ago and start suffering from increased failure rates and missing replacement parts.

A fully new set of read-out electronics has been designed: The analog signals will be shaped, amplified and discriminated by PASTTREC, an ASIC developed at AGH Krakow for the PANDA Straw Tube Tracker. Digitization is accomplished by FPGA-based TDCs that also contain all necessary data handling, filtering and event building features. The design and operation of the existing drift chambers posed a couple of challenges to the design of the electronics that will be explained in detail.

HADES has been designed as a high acceptance spectrometer leaving minimal space for infrastructure in the gaps between sensitive detector areas. Combined with fixed and short signal cables the geometry of the new electronics was restricted to narrow and long boards. Densely packed electronics also limit the allowable power consumption as cooling is only foreseen by air, including some forced flow in the most dense regions.

Another crucial aspect is the design of the powering scheme. Noise sensitivity of the detector does not allow for switching power supplies close to the read-out electronics. On the other hand, the distance to power supplies varies substantially (up to 15 m) and local power dissipation has to be kept low. The solution was a distributed scheme, employing adjustable low-noise DCDC converters just outside the detector and on-board LDO regulators for precise adjustment.

Further design considerations include easing installation and replacement operations. All connections for power, data and flex signal cables are located on Add-On boards that can easily be connected and removed in hardly accessible spaces. These Add-Ons also contain the whole signal filter and protection circuits as these are the components most likely to fail over time when subject to high-voltage discharges inside the detector.

The digital electronics stage is based on Lattice ECP5 FPGA that provide a low-power and low-cost platform to implement digitization and communications. Time measurement is accomplished by a common clocked TDC design running at a average bin size of 400 ps (140 ps RMS). Data is filtered by applying spike rejection

and trigger windows before it is forwarded to the data collection servers. All communications are based on the existing HADES DAQ network TrbNet that provides full control and monitoring access, triggering and busy time controls.

We are going to present a comprehensive summary of the read-out electronics and the design considerations leading to the final solution.

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