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# A prototype 4D-tracking demonstrator based on the TimeSPOT developments.

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We present first results obtained with a prototype 4D-tracking demonstrator, using sensors and electronics developed within the TimeSPOT project, and tested on a positive charged pion beam at CERN SPS. The setup consists of six small tracking layers in a row, having area of about 3 mm squared each, three of which equipped with 3D-trench silicon sensors and three with 3D-column diamond sensors. The six layers are then read-out by a KC705 Xilinx board on a PC. We describe the demonstrator structure and operation and illustrate results on its tracking capabilities.

## Summary (500 words)

The TimeSPOT 4D-tracking demonstrator has been tested on a positive charged 180 GeV/c pion beam at CERN SPS. The tracking setup consists of up to six small sensing layers in a row, having area of about 3 mm squared each. Three of the layers are equipped with 3D-trench silicon sensors and three with 3D-column diamond sensors. In previous tests, TimeSPOT 3D-trench pixels have been demonstrated being capable of an intrinsic time resolution below 10 ps, while 3D-column diamond pixels have intrinsic resolution below 80 ps.

The tracking layers are matrices of 32x32 pixels with 55 μm pitch, hybridized with and read-out by the Timespot1 ASIC, implemented in CMOS 28-nm technology. The hybrids are assembled on stations, based on dedicated PCBs. Each of the 1024 pixels of the ASIC integrate one fast Analog Front End and one high-time-resolution TDC. The TDC is capable of a time resolution of 20 ps rms, while the AFE has about 60 ps rms in average, with a spread in performance from about 20 ps to 100 ps, due to a well-known design problem in the offset compensation technique of the discriminator.

The six stations are configured using an I2C interface. Data link are output using LVDS cables (8 cables of 1.28 Gbps each per each layer). All the links are sent to a data-concentrating board (named Mezzanine), which is plugged on a KC705 Xilinx board. The Xilinx board formats and temporarily stores data on internal registers. Data are finally readout on a PC using an Ethernet protocol. The system clocks are distributed by one COTS clock-managing Si5341 board from Silicon Labs, configurable by means of an I2C interface.

In order to help the beam-alignment procedure, two mono-pixel layers are placed at the beginning and at the end of the tracking row. The mono-pixels can be read-out by dedicated single channel analog boards and an oscilloscope, acquired during the alignment procedure, before data-taking. The tracking stations are mounted on movable mechanical supports on an orientable rail, whose angle in the plane where the stations are placed can be adjusted to match the beam direction. All the stations are placed inside a metal box, which acts as an EMI shield. The DAQ system and the clock distributor Si5341 PCB are placed outside the same metal box. Pictures of the demonstrator can be found in the attachment files.

After beam alignment, data have been acquired and analyzed concerning the timing and tracking performance of the system. First results are presented in the paper.

**Primary authors:** LAI, Adriano (Universita e INFN, Cagliari (IT)); STABILE, Alberto (Università degli studi di Milano); CARDINI, Alessandro (INFN Cagliari, Italy); LAMPIS, Andrea (Universita e INFN, Cagliari (IT)); LOI,

Angelo; BRUNDU, Davide (Universita e INFN, Cagliari (IT)); COSSU, Gian Matteo (INFN, Cagliari (IT)); PASSALEVA, Giovanni (INFN Florence (IT)); PICCOLO, Lorenzo; ANDERLINI, Lucio (Universita e INFN, Firenze (IT)); ADDISON, Matt (University of Manchester (GB)); GARAU, Michela (Universita e INFN, Cagliari (IT)); VELTRI, Michele (Universita e INFN, Firenze (IT)); CADEDDU, Sandro (Universita e INFN, Cagliari (IT)); LIBERALI, Valentino (Università degli Studi di Milano)

**Presenters:** LOI, Angelo (Universita e INFN, Cagliari (IT)); LOI, Angelo

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