Prototype electronics for the silicon pad layers of the future Forward Calorimeter (FoCal) of the ALICE experiment at the LHC.

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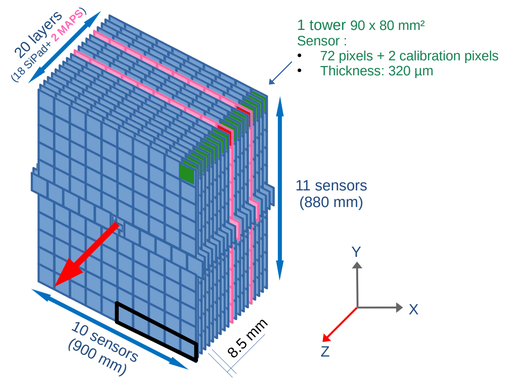
Overview

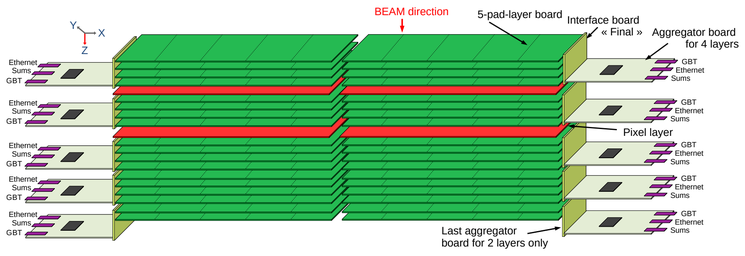
1) FoCal: electromagnetic calorimeter design

- FoCal will cover the pseudorapidity region $3.4 < \eta < 5.8$
- Sampling calorimeter segmented into 110 towers
- One tower is made of 18 silicon pad (SiPad) sensors



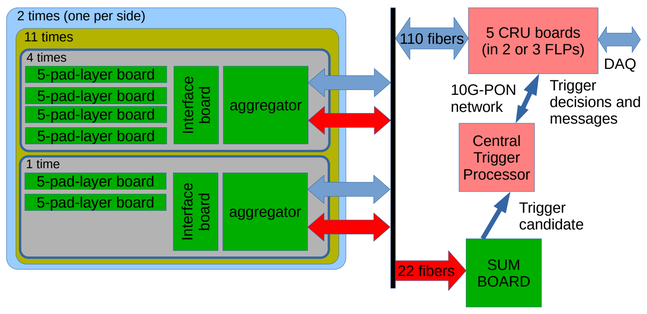
2) Proposed electronics architecture for readout at the time of the LOI (final system will be different)

- 5-pad-layer boards read out on each side by FPGA-based aggregator boards



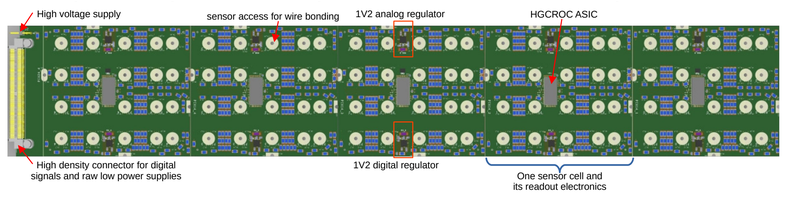
3) Focal-E in ALICE's framework

- 396 5-pad-layer boards
- 110 aggregator boards
- 110 'final' interface boards
- One SUM board

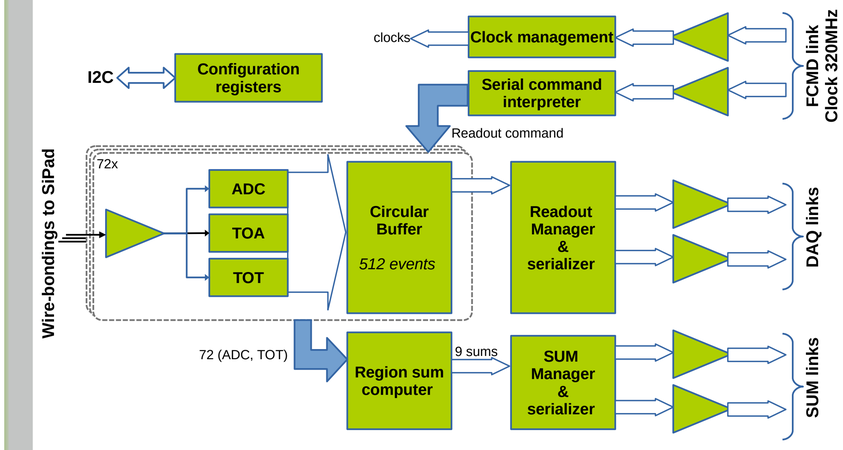


4) 5-pad-layer board

- One pad layer = 22 PCB having of $45 \times 8\,\mathrm{cm}^2$
- One PCB = 5 SiPad (backside) + 5 HGCROC (frontside)
- Expected power dissipation is about 6.75 W per board



Very front-end: HGCROC

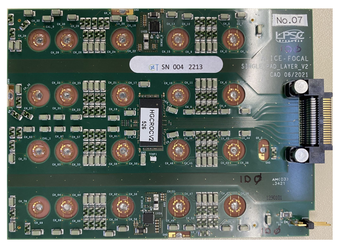


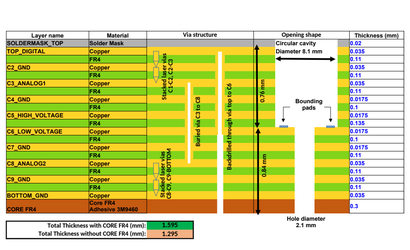
- 72 regular + 2 calibration channels ($0.2\,\mathrm{fC} \rightarrow 10\,\mathrm{pC}$)
- Output serial links at 1280 Mbps
  - DAQ: provide selected data, full frame needs 1.075 µs
  - SUM: continuous sending of 9 SUMs encoded on 7 bits
- Real time commands through Fast Command port
  - Trigger
  - Calibration
  - Bunch/Orbit counter reset
- Configuration through indirect I2C addressing

Prototype tower design

Single pad board

- Reduced model of the 5-pad-layer board
- High voltage (800 V), analog and digital signals
- 24 holes for the sensor to PCB connection by wire bonding

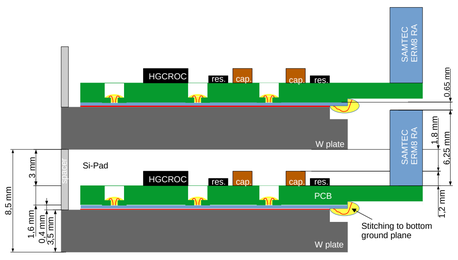


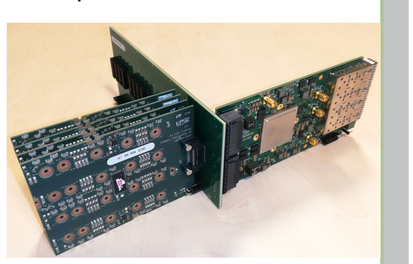


- PCB design adapted to wire bonder capability
- Deflection $< 10\,\mu\mathrm{m}$
- Wire bonding performed after board assembly

Tower stacking constraints

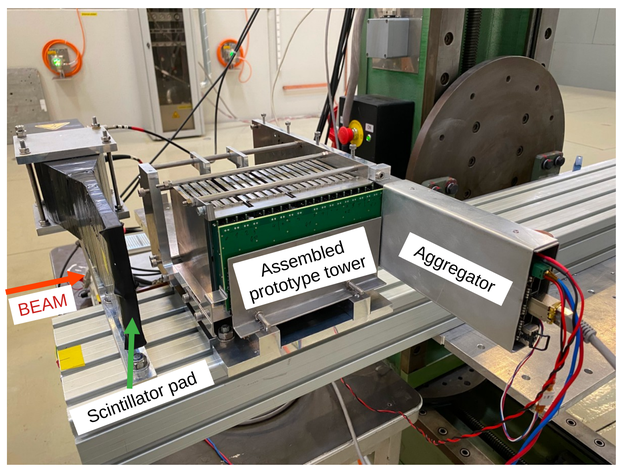
- Detector driven: 3.5 mm of Tungsten every 8.5 mm
- High voltage: Clearance between capacitor





Prototype electronics: one tower

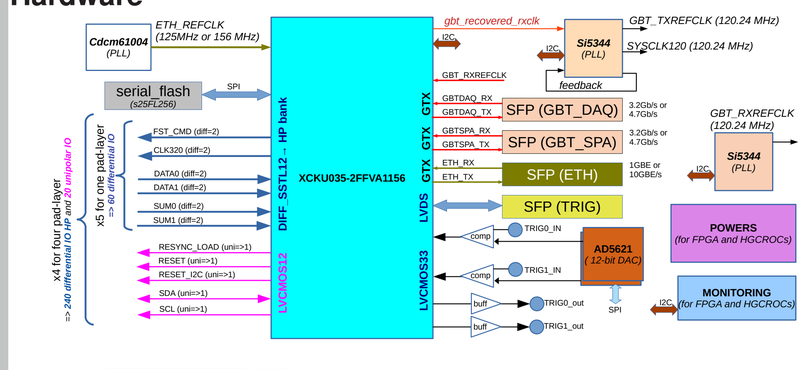
- Validation of the architecture with realistic readout
- Prototype installed on the T9 beamline at the CERN PS

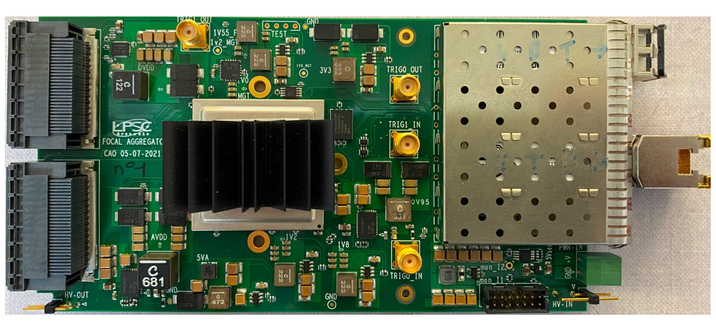


- 18 single pads, 1 'prototype' interface, 1 aggregator
- Readout/trigger through Common Readout Unit (CRU)

Aggregator board

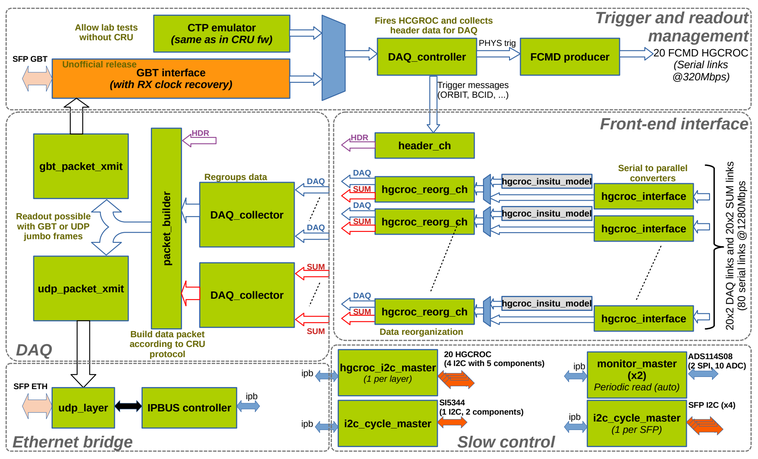
Hardware





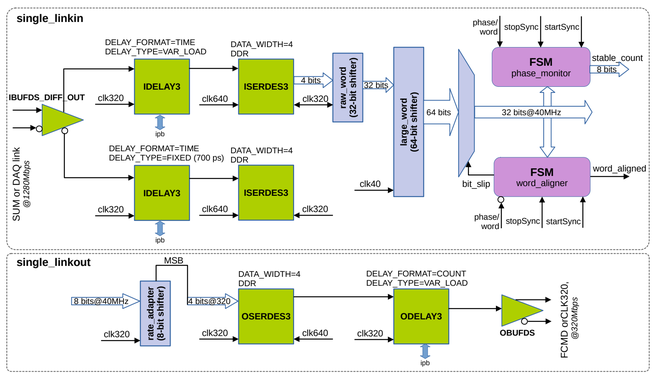
- Board dimension: $80\,\mathrm{mm} \times 150\,\mathrm{mm}$

1) Firmware: overview



- External/internal trigger (debugging/calibration)
- In situ simulation data producer
- DAQ: with ALICE framework (GBT) or reduced test setup (Ethernet)
- 1296 channels read-out at 33 kHz (without zero-suppression)
- Slow control for HGCROC, PLL, SFP, monitorings, ...

2) Firmware: serial link interfaces



- 144 input streams at 1280 Mbps
- 36 output streams/clocks at 320 Mbps
- Startup synchronization handled by a FSM for each tap delay

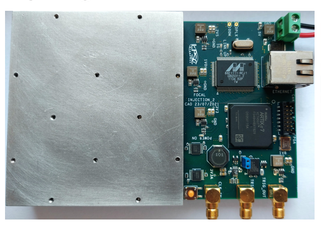
3)Firmware: total resource usage

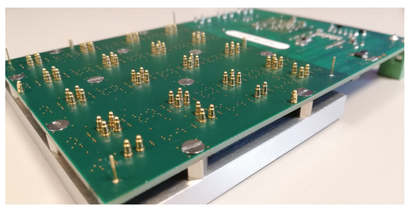
- 38,619 Look Up Tables (19%)
- 58,787 Flip-Flops (14%)
- 296 block RAMs (54%)

Charge injector board

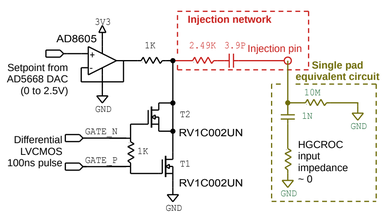
Overview

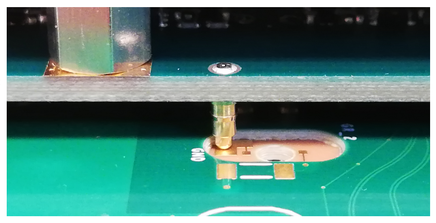
- Provide a testing tool for PCB before wire-bonding
- 72 + 2 charge injectors
- Spring loaded contact





Injection channel





- Gate individually controlled by FPGA (XC7A35T-2FGG484C)
- Injection level trimmed by 16-bit DACs

References

- ALICE collaboration, *Letter of Intent: A Forward Calorimeter (FoCal) in the ALICE experiment*, Tech. Rep. CERN-LHCC-2020-009, LHCC-I-036, CERN, 2020
- D. Thienpont et al., *Performance study of HGCROC-v2: the front-end electronics for the CMS high granularity calorimeter*, JINST 15 (2020) C04055
- O. Bourrion et al., *Versatile firmware for the common readout unit (CRU) of the ALICE experiment at the LHC*, JINST 16 (2021) P05019.
- M. Rauch, *Latest Results from ALICE FoCal Prototypes*, PoS ICHEP2022 (2022) 317

Acknowledgements

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