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Prototype electronics for the silicon pad layers of the future Forward Calorimeter (FoCal) of the ALICE experiment at the LHC

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A new Forward Calorimeter (FoCal) system has been proposed as part of the ALICE upgrades planned for LHC Run 4 which features a Si+W electromagnetic calorimeter. A first tower prototype corresponding to 1/5 of the nominal module of the electromagnetic calorimeter has been built in 2022. It is composed of 20 passive layers of tungsten absorber interleaved with 18 active layers of low-granularity silicon pads. Each pad layer is read out by 110 silicon pad sensors of 72 channels, amounting to a total of 1980 channels. This contribution describes the electronics developed from front-end to back-end.

Summary (500 words)

The prototype tower is a sandwich of tungsten and silicon sensors covering a surface of about 9x8cm^2. The sensors are 320 µm-thick p-type silicon PIN photodiode arrays segmented into 72 cells (plus two calibration cells of smaller size). The front-end solution used for the silicon sensor readout is the High Granularity Calorimeter Readout Chip (HGCROC) Application Specific Integrated Circuit (ASIC) developed for the CMS High Granularity Calorimeter (HGCal).

Dedicated printed circuit board (PCB), named “single pad boards”, were designed and fabricated to accommodate the silicon pad sensors glued on one side and the very front-end electronic components mounted on the other side. The sensors are wire-bonded to the single pad boards through sensor access holes for wire bonding.

The single pad board design was first validated with an FPGA evaluation kit and an external charge injection board (72 channels). This charge injector board, featuring an FPGA and driven synchronously by the acquisition electronics permitted the qualification of the 18 single pad boards before prototype assembly.

The 18 single pad boards are connected through a proprietary interface board, to a dedicated control and readout board, named “aggregator”. This board features a single FPGA that drives synchronously the 18 HGCROCs with a total of 36 downstream links, gathers the data provided in return by the 144 readout links and configures the ASICs via I2C links.

Each front-end ASIC is clocked by a eight-time multiple of the LHC machine frequency (320 MHz), triggered through a fast serial command link (320 Mbps) and read-out by four high speed links (each working at 1280 Mbps). Upon trigger reception, the HGCROC provides three measurements (ADC, TOA, and TOT) for each of its 72 channels.

The aggregator board handles the raw data and permits to either interface the prototype with the ALICE data acquisition through GBT links or with a standalone computer though Ethernet for in lab test and characterization. Without zero suppression and using the GBT links a maximum trigger rate of 33 kHz can be reached to record the 1296 channels.

To speed up firmware and software validation, several test features were embedded in the aggregator such as front-end fake data generators, ALICE Central Trigger Processor message generator. This enabled fast prototype commissioning in preparation for the three test beams conducted at CERN PS and SPS with the official ALICE O2 DAQ system.

This contribution describes, the electronics architecture, the technological choices and the firmwares developed to instrument a tower prototype composed of 18 silicon pad sensors. The companion tools developed will be presented as well.

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