Upgrade of the ATLAS Level-0 TGC Endcap Muon Trigger for HL-LHC

1-6 October, Geremeas, Sardinia, Italy
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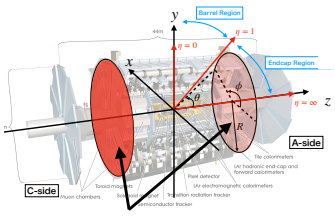
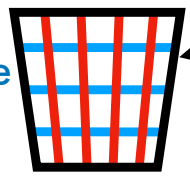
The Level-0 endcap muon trigger system for the ATLAS experiment at the HL-LHC, including the algorithms using Thin Gap Chamber (TGC), has been developed. Muon segments are reconstructed using all hits of TGC, then combined with information from other detectors for precise p_T reconstruction and reduction of fake hits. The trigger algorithm provides high efficiency for reconstruction of high-p_T muons, and suppresses muons with lower-p_T than threshold. Each step of the algorithm is properly implemented in the firmware, and all trigger firmware modules are fully connected as a trigger chain and expanded for processing trigger in the whole region. Logics in the trigger firmware are integrated on the 1st prototype of the trigger board (Sector Logic, SL) with large-scale FPGA. The integrated firmware is implemented with reasonable resource and latency.

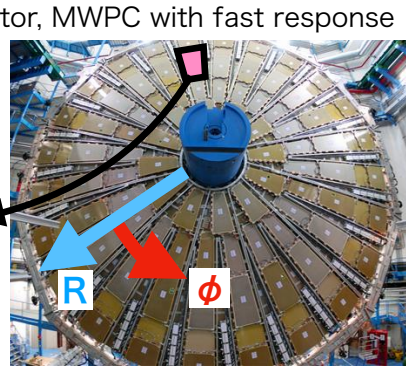
Thin Gap Chamber (TGC)

Muon detector for trigger in the ATLAS detector, MWPC with fast response

- 2D readout in Wire (R) and Strip (ϕ)
- TGC Big Wheel (BW) covers Endcap Region
- 7 Layers, 3 stations

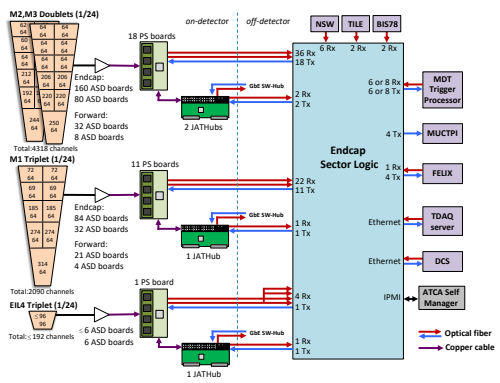


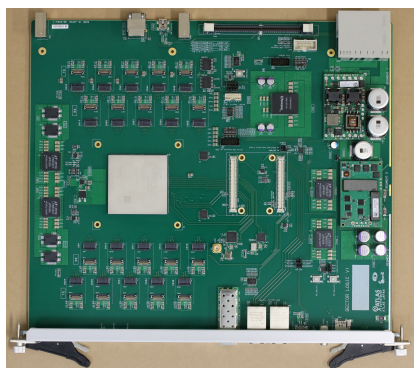




Upgrade Concept for HL-LHC

- Send every hit of 1/24 in ϕ to a trigger processor with a large-scale FPGA (Endcap Sector-Logic, SL) and process trigger here
  - FPGA : Xilinx Virtex Ultrascale+ XCVU13P
  - MPSoC mezzanine : Mercury XU5
  - Optical transceiver : FireFly RX (12ch) x 10, TX (12ch) x 10
- Far less limitation for data in halfway, more complex algorithm





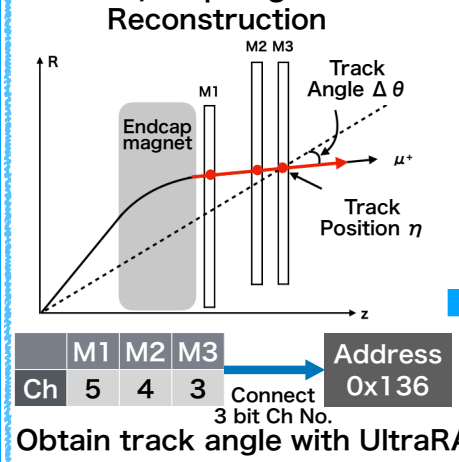
Development of Trigger Algorithm

Objective of the trigger algorithm:

- Reconstruct muon and its transverse momentum (p_T)
- Reject candidates not coming from IP, muons with lower-p_T than threshold
- Develop logics within strict latency (~ 1.1μs) and limited FPGA resource

Muon reconstruction separated in several steps

Wire/Strip Segment Reconstruction

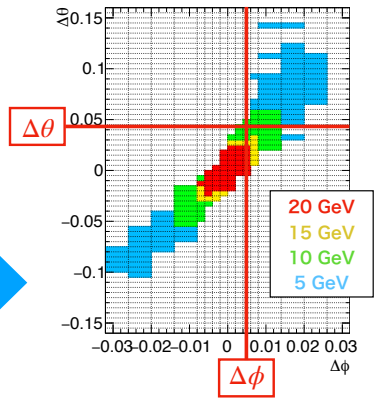


Obtain track angle with UltraRAM

Extract information without fitting procedure

- **Simple, fixed No. of steps, minimum resource usage**

Wire-Strip Coincidence

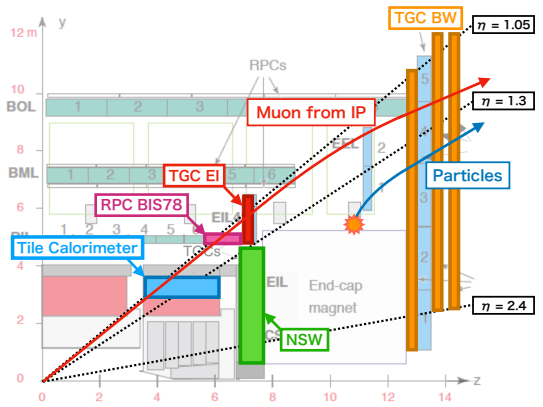


Obtain p_T using BlockRAM

Set track angles as address

- Get corresponding p_T without calculation

Inner Coincidence

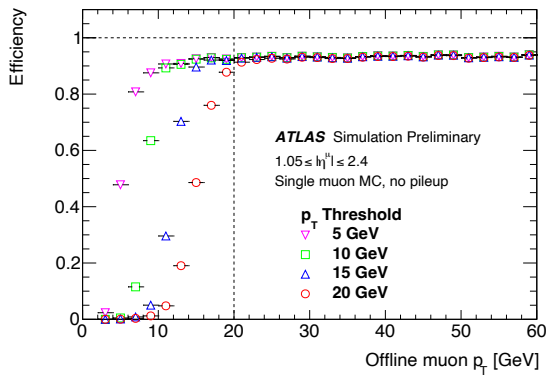


Take coincidence with inner detectors

Use position/angle information for getting more accurate p_T using RAMs

- Suppress fake trigger
- Reduce low p_T muons

Estimated efficiency with Single Muon MC sample

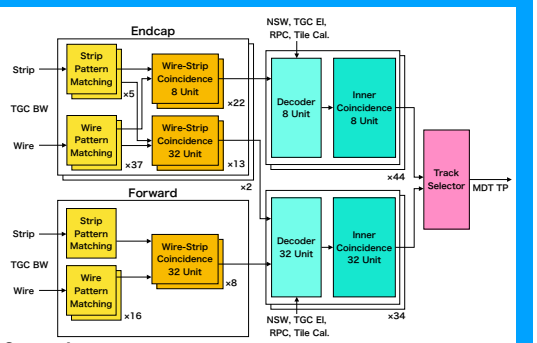


Level-0 Endcap muon trigger efficiency in each threshold

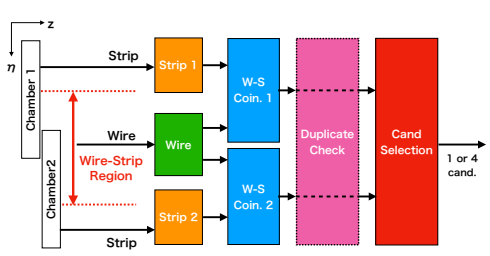
- **High plateau efficiency**
- **Suppression of low p_T muons**

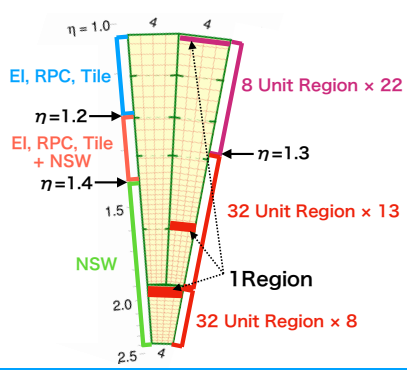
Implementation with the Firmware

- Completed whole chain of trigger modules in small area
- A SL covers large area (1/24 in ϕ)
  - Expanded to the whole region
  - Implemented modules consist of simple submodules
    - Used in the whole area



- Each module covers different size of region
  - Consider its boundary and connection
  - Properly connected all trigger modules

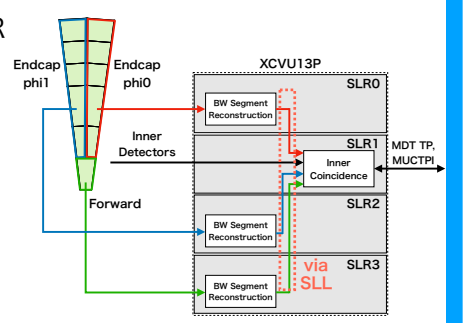




Integration on the SL 1st Prototype

FPGA (XCVU13P) consists of 4 silicon die (Super Logic Region, SLR)

- Send hits in each sector to individual SLR
  - Process BW reconstruction
- Send reconstructed track to SLR1 using Super Long Line (SLL)
  - The number of SLL is limited
  - Takes long time for transportation
  - Causes timing violation
    - Optimization of pipeline registers,…
- Optimized each module and reduced information sent to SLR1
  - **Integration of all logics finished**, further sophistication ongoing



	CLB LUT	CLB Register	BRAM	URAM
SLR0	58%	26%	74%	52%
SLR1	81%	27%	29%	50%
SLR2	59%	27%	80%	52%
SLR3	26%	13%	33%	20%

Total Latency at SL:
~ 0.49 μs

Requirement : ~1.1 μs

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On behalf of the ATLAS Collaboration

ATLAS EXPERIMENT