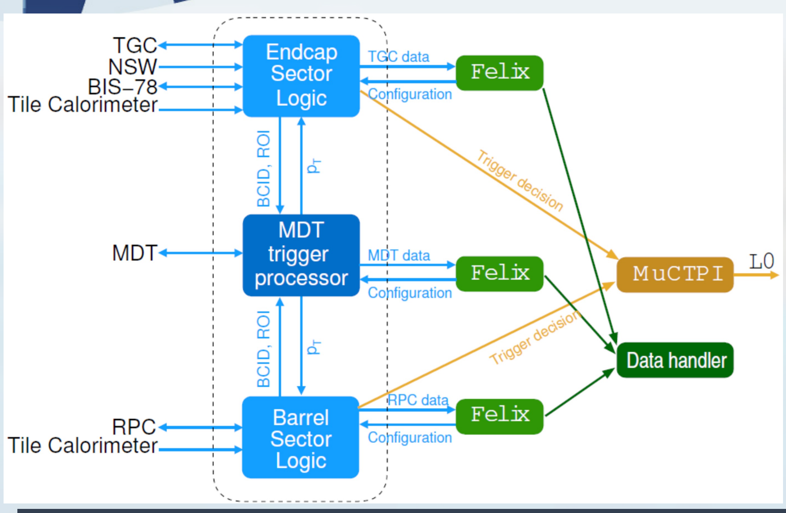
Status of the MDT Trigger Processor for the ATLAS Level-0 Muon Trigger at the HL-LHC

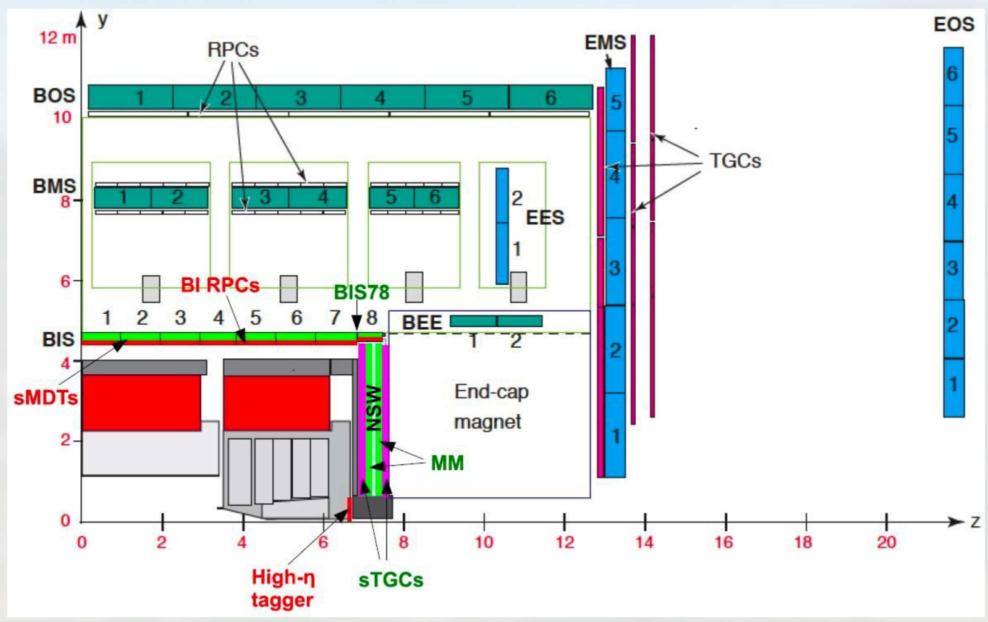
Rimsky Rojas[1] (rimsky.rojas@cern.ch)
on behalf of the ATLAS TDAQ collaboration
[1]University of Massachusetts

Introduction



The Monitored Drift Tubes (MDT) Trigger Processor (MDT-TP) is a key ATLAS Level-0 Muon trigger upgrade component designed to meet HL-LHC requirements. The MDT-TP will use the high-resolution tracking capabilities of the MDT hits in the hardware-based trigger for the first time in ATLAS to improve the performance [1].

A total of 64 MDT-TP boards are required for ATLAS. Each MDT-TP directly interfaces with several Chamber Service Modules (CSM) to collect hit-timing information, configure/monitor the MDT front-end electronics, and distribute TTC signals. Thus, the MDT-TP is also responsible for DAQ and is the only interface to FELIX [2]. Fixed latency in response to the incoming muon trigger candidate is required.

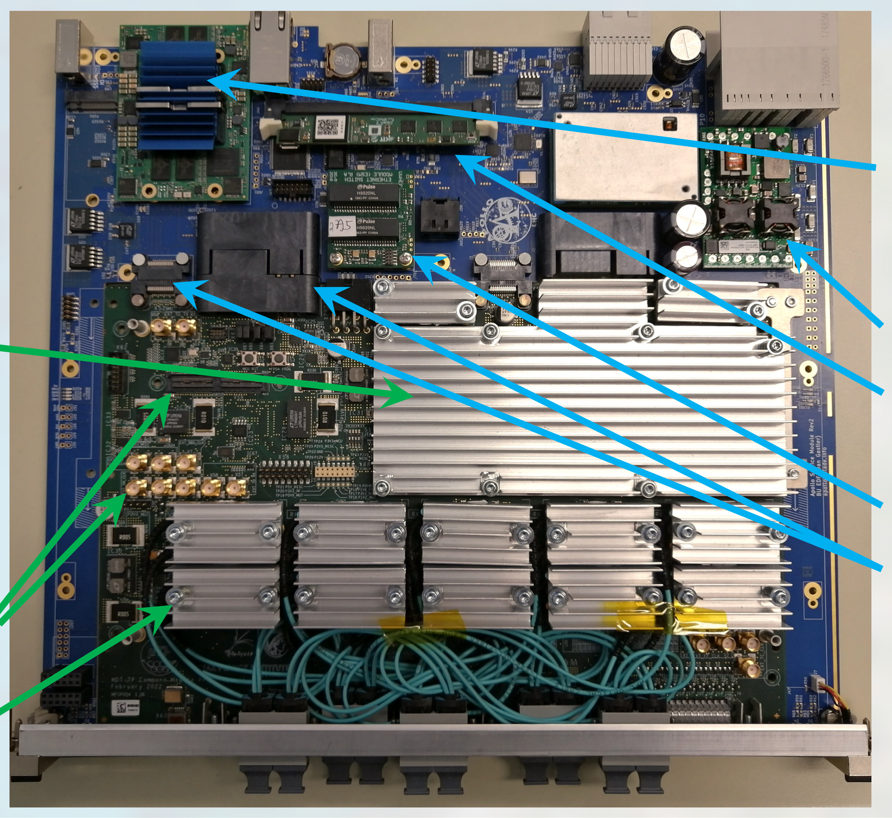


MDT-TP Hardware

Hardware is based on the open-source platform Apollo [3]. Comprised of two PCB modules as seen in the picture of a fully assembled MDT-TP prototype:

1. Command Module (CM): application-specific module provides

- Ultrascale+ FPGA VU13p (CM-FPGA).
- Flexible clock scheme based on clock synthesizers (Si5345x) with clock recovery capability implemented.
- MCU for slow control of peripherals.
- SMA and high-speed connectors for debugging.
- 120 optical transceivers up to 14Gbps.



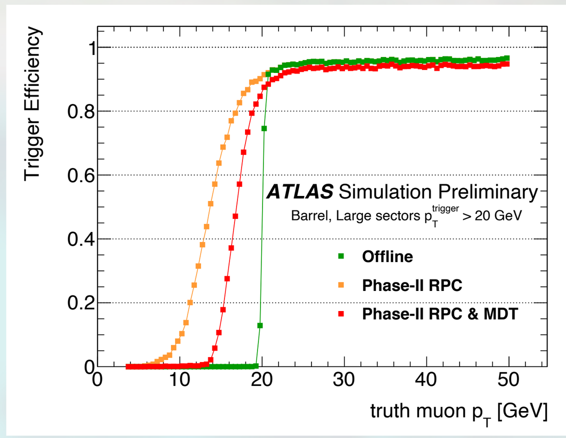
2 Service Module (SM): common to all Apollo applications. It provides:

- A powerful system-on-module (SoM), running Almalinux8, control and monitoring using systemd daemons.
- Power entry and conditioning.
- ATCA Intelligent Platform Management Controller (open-IPMC).
- Ethernet switch and connectors.
- Flexible communications infrastructure. e.g., Chip-Chip between SoM and CM-FPGA allow register mapping from CM-FPGA to SoM OS as endpoint.

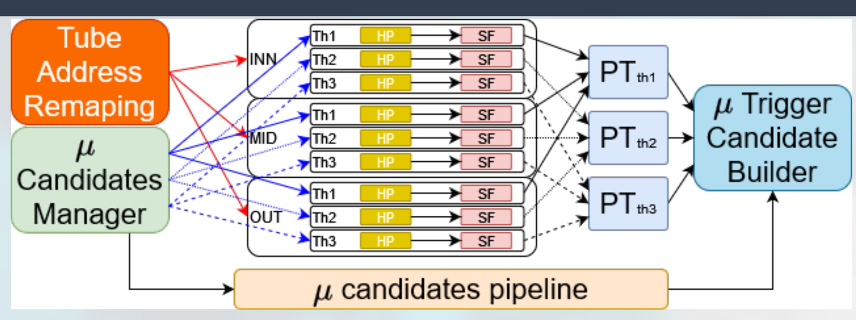
Performance [1]

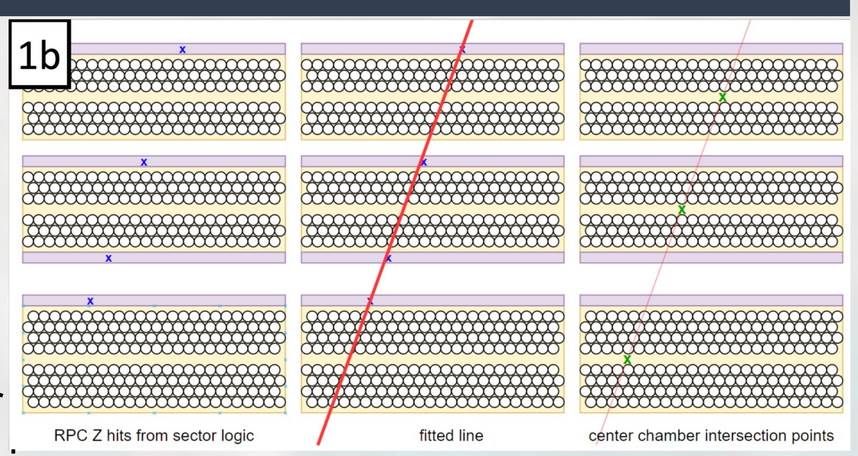
The MDT-TP trigger algorithm will:

- Help to reject fake SL candidates.
- Improve the momentum resolution.
- Reduce the output rate ~50-70% while keeping high efficiency for muons with momenta above the 20 GeV threshold.



Algorithm





Trigger overview:

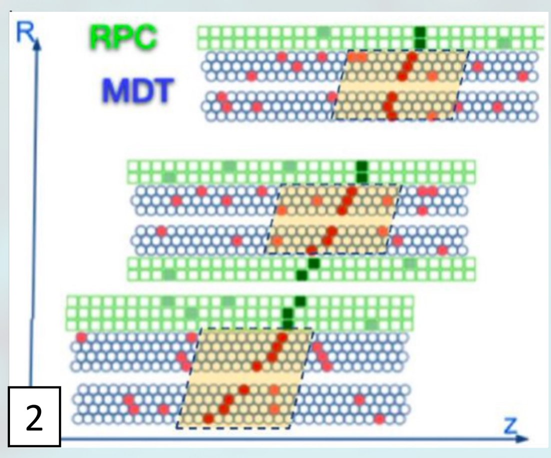
- Capable of processing 3 simultaneous candidates per trigger sector containing SL-BCID/ROI used to determine the instant of the hit and reduce the number of tubes to read.
- Latency budget of 1.764 us for the full algorithm.

1a. Tube Address Remapping (TAR):

- MDT hit coordinates are calculated.
- Pipelined waiting for the candidate to arrive.

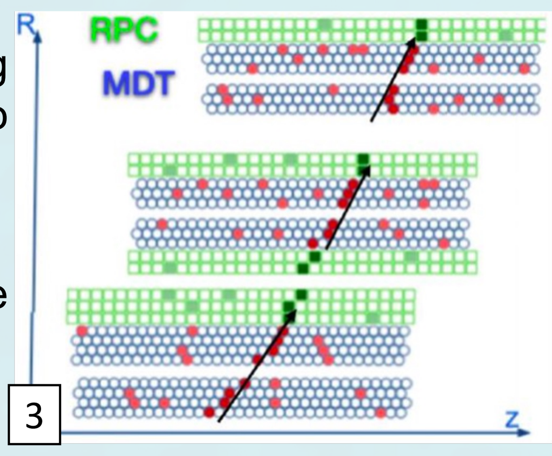
1b. Muon Candidate Manager (UCM):

- Sorts the candidates from the Sector Logic (SL).
- Manages the multithreaded architecture.
- Processes the candidates to obtain the track angle and crossing position at each MDT station from the **SL RPC/TGC seeds** to determine the Region-of-Interest (ROI).



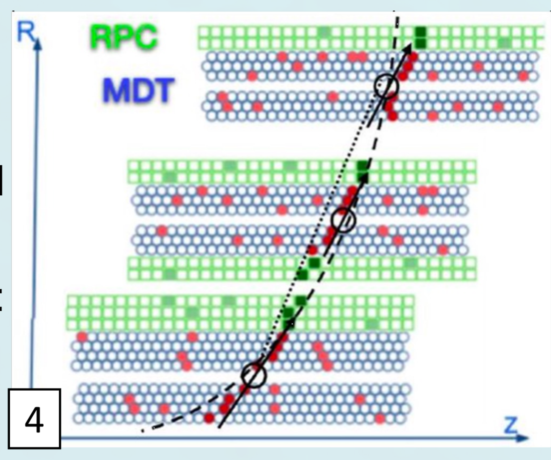
2. Hit Processor (HP):

- Filters the MDT hits in space and time using the candidate information to define the boundaries of the filters.
- The valid hits are then processed to obtain their drift radius
- Calculates local position of the tube respect to the ROI window origin.



3. Segment Finder (SF):

- Calculates the muon track segment at each MDT station.
- For each segment, it measures its precise position and angle and sends them to the momentum estimation block.
- Two different implementations are available with different algorithms: Legendre Transform SF (LSF) and Compact SF (CSF).

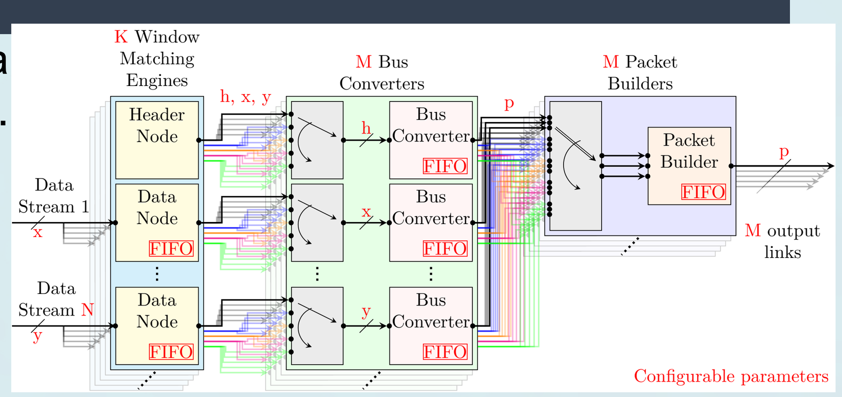


4. p_T estimator:

- Muon track segments are combined to obtain the track momentum.
- Two algorithms used depending on number of available segments: when 3 segments (Fig. 2-4) Sagitta algorithm and when 2 segments the deflection angle.

Readout: DAQ Level-0 Accept (L0A) readout module:

- Performs a flexible concurrent timestamp-based data selection and packet formatting upon the receiving a L0A.
- Each L0A activate a window matching engine (WME).
- Multiple WME can be active at same time.
- Data from chambers in each station is serialized and presented to respective time windows, the filtered data is formatted into a packet when selection is finished (time window closed).
- For each station, output packets are distributed to multiple links in a round-robin fashion to meet bandwidth requirement.

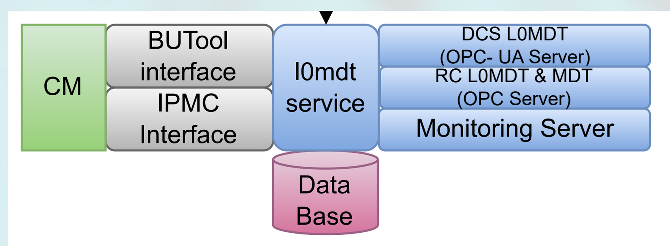


Status of Developments

Firmware:

- All firmware blocks are developed and being debugged, tested and validated.
- Validation done with VHDL testbench & cocoTB framework [4].
- Code management and Continuous integration handled using Hog (HDL-on-Git)[5].
- Algorithm resources estimated to be within parameters.
- Progress to complete integration of FW blocks and meet timing.
- Integrating control & monitoring blocks, including fast monitoring system, to spy the internal buses and perform playback tests.

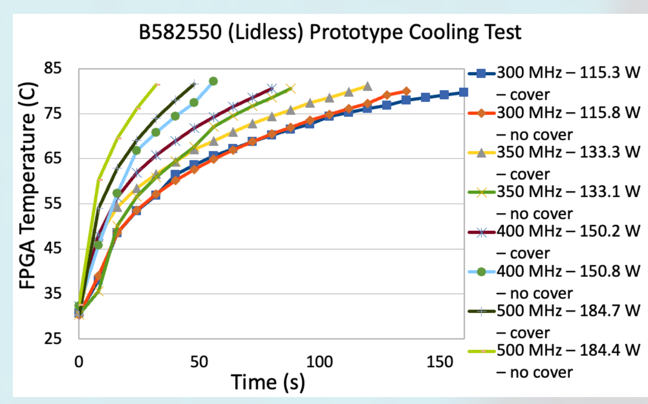
Software on Service Module SoM:



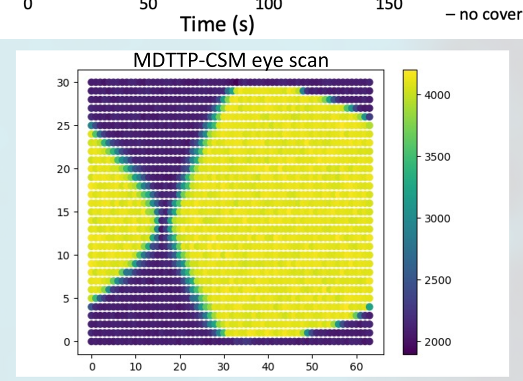
- L0MDT services as core of board operations, control and monitoring is being developed.
- Core elements in place to help testing.
- Integration of external systems as Run Control & DCS in progress. First FELIX computers with Phase 2 FELIX [2] prototypes cards expected soon to start integration. Test stands at institutes and CERN ready and working.

Prototype validation

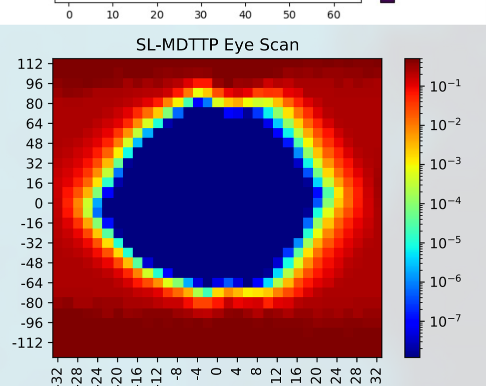
- **Hardware testing of the CM Prototype**
  - Test of all IC in this fully functional prototype.
  - Testing all the communication paths such as including optical links, SM-CM C2C, etc.
  - Stress/cooling tests performed in ATCA crate.



- **CSM communication tests**
  - Eye diagrams taken and able to communicate to lpGBT at 10.24Gbps.



- **Sector Logic communication tests.**
  - Eye diagram between both boards at 9.6Gbps.
  - Test of firmware modules ongoing.



- **FELIX communication tests.**
  - Firmware modules tested on another hardware, tests in prototype ongoing.

References

- [1] https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults
- [2] https://atlas-project-felix.web.cern.ch
- [3] https://apollo-lhc.gitlab.io
- [4] https://github.com/cocotb/cocotb
- [5] https://cern.ch/hog