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Status of the MDT Trigger Processor for the ATLAS Level-0 Muon Trigger at the HL-LHC

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The MDT Trigger Processor (MDTTP) is a key ATLAS Level-0 Muon trigger upgrade component designed to meet High-Luminosity LHC requirements. The MDTTP will use MDT hits in the trigger for the first in ATLAS to improve the momentum resolution of muon candidates provided by RPC and TGC detectors and reduce fake muon trigger rate.

The MDTTP hardware is based on the Apollo ATCA platform. The pre-production prototype includes a VU13P-FPGA, high-speed FireFly optical transceivers, peripherals, and other improvements learned from using the previous hardware demonstrator. We present the prototype status, firmware implementation, core algorithm, slow-control software, and first integration tests.

Summary (500 words)

The first-level muon trigger (L0Muon) of the ATLAS experiment will be upgraded to operate in the substantially increased luminosity environment of the HL-LHC. The moderate spatial resolution of RPC and TGC trigger chambers limits the selectivity of the current system. The Monitored Drift Tube (MDT) chambers, currently used for offline precision tracking, will be included in the trigger to improve the transverse momentum resolution and reduce the rate of fake muon triggers.

Hit data with moderate spatial resolution from RPC or TGC are used to determine muon candidates at the Sector Logic. These candidates define regions of interest for the MDT trigger processor (MDTTP) to process MDT hits matching the regions in space and time. Those hits are used to form track segments, which are combined to determine the transverse momentum. The MDTTP will also reject low-quality sector logic candidates for which no MDT track segments could be found.
According to simulation studies, the MDTTP is expected to reduce the L0Muon output trigger rate by up to 70%, while keeping the efficiency plateau at 95% for a single muon trigger with a threshold of 20 GeV.

The MDTTP will be implemented using the open-source platform Apollo. An Apollo ATCA blade is comprised of two PCB modules called Service Module (SM) and Command Module (CM). The SM, common to all Apollo applications, provides the required ATCA Intelligent Platform Management Controller (IPMC), power entry and conditioning, a powerful system-on-module (SoM) computer, and flexible clock and communications infrastructure. The application-specific CM provides the processing FPGA, the FireFly transceivers for communication with the other systems inside ATLAS, and a few peripherals.

A pre-production prototype of the MDT trigger processor CM has been produced and is currently under test, featuring one large Xilinx VU13P FPGA and eight 12-channel bidirectional optical transceiver modules, with a link speed up to 25 Gbps. The prototype is based on the first test results of the hardware demonstrator.

In addition to the trigger processing tasks, the MDTTP will also be responsible for configuring and monitoring the MDT Chamber Service Module (CSM) and transmitting MDT hit information to the FELIX system when a L0 acceptance signal is received.

The MDTTP firmware is designed to have a fixed latency of approximately 1.7μs and is divided into Hardware Abstraction Layer (HAL) and User Logic (UL). The HAL firmware implements the low-level interface to Sector Logic, CSM, SM, and FELIX, providing control and data to the UL at 320MHz clock frequency. Results of the

first tests interfacing CSM, SM, and FELIX are presented. The UL firmware implements the trigger, data acquisition, control, and monitoring logic. While a reduced version of the firmware has been tested on the demonstrator board with the KU15 FPGA, a full version is currently being implemented targeting the VU13P FPGA. The design fits well in the chosen FPGA, satisfying the latency constraint. The status of the slow control software running on the SM and the integration into the ATLAS Detector Control System infrastructure are also presented.

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