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System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC

Tuesday 3 October 2023 15:00 (20 minutes)

For the High-Luminosity Large Hadron Collider era, the trigger and data acquisition system of the Compact Muon Solenoid experiment will be entirely replaced. Novel design choices have been explored, including ATCA platforms with SoC controllers and newly available interconnect technologies with serial optical links with data rates up to 28 Gb/s. Trigger data analysis will be performed through sophisticated algorithms, including widespread use of Machine Learning, in Xilinx UltraScale+ FPGAs. The system will process over 50 Tb/s of detector data with an event rate of 750 kHz. The system design and prototyping are described and examples of trigger algorithms reviewed.

Summary (500 words)

The High-Luminosity LHC will open an unprecedented window on the weak-scale nature of the Universe, providing high-precision measurements of the standard model, as well as searches for new physics. Such precision measurements and searches require information-rich datasets with a statistical power that matches the high luminosity provided by the upgrade of the LHC. Collecting those datasets efficiently will be a challenging task in the harsh environment of 200 proton-proton interactions per LHC bunch crossing.

For this purpose, the Compact Muon Solenoid (CMS) collaboration has designed an efficient data-processing hardware trigger (Level-1) that will include tracking information and high-granularity calorimeter information [1]. The system design will take full advantage of advances in FPGA and link technologies over recent years, providing a high-performance, low-latency (<12.5 us) computing platform for large throughput and sophisticated data correlation across diverse data sources.

Modern technologies offer an effective solution to achieve these goals. The upgraded system will make use of Xilinx UltraScale+ FPGAs hosted on ATCA hardware platforms, including SoC controllers and communicating through optical interconnects at up to 28 Gb/s.

In order to enable the physics programme sophisticated trigger algorithms are required, for example to combine data from different detector elements optimally. Machine Learning algorithms will be used widely and a range of algorithms have been prototyped, in many cases using High Level Synthesis tools to produce firmware which has been tested in prototype hardware.

The talk will cover the technological aspects of the HL-LHC upgrade to the trigger system, emphasising the results of recent prototyping and slice tests, and their impact on the system design. Examples of conventional and Machine Learning algorithms that have been implemented and tested in prototype boards will also be presented.

[1] CMS Collaboration, The Phase-2 Upgrade of the CMS Level-1 Trigger, CERN-LHCC-2020-004 (http://cds.cern.ch/record/2714892)

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