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Adaptability and efficiency of the CMS Level-1 Global Trigger firmware implementation for Phase-2

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We present details on the new Level-1 Global Trigger at CMS for the upcoming high-luminosity operation of the LHC. Our focus is on the newly developed firmware, which employs a bottom-up generic approach to enhance menu adaptability and accommodate the increase in upstream information. We also highlight our efficient pipelining strategy that ensures excellent routability at 480 MHz. Furthermore, we discuss the three Serenity boards for which a prototype exists, together with their current and future testing and validation endeavours.

Summary (500 words)

In preparation for the Phase-2 operation at the high-luminosity LHC, scheduled to commence in 2029, the CMS detector is undergoing significant upgrades to its detectors and readout electronics. The increased luminosity also poses additional challenges for the CMS trigger system. To ensure that the physics performance is maintained or improved under the new pile-up conditions, a completely new Level-1 trigger system is being designed as part of the upgrade. The new system will process information from the calorimeter, the muon systems as well as reconstructed tracks from the silicon tracker. An increased latency budget of 12.5 µs, compared to 3.5 µs in the current trigger, will also allow for sophisticated algorithms such as vertex finding, particle flow reconstruction and the extensive use of neural networks, which were previously only possible at later software-driven stages of the trigger system. From the side of the final stage of the Level-1 trigger pipeline, the Global Trigger is being entirely redesigned, including a modern continuous-integration-driven development and testing infrastructure and a completely rewritten firmware to cope with the increase of available data from the upstream trigger systems. Here, we employed the approach of writing every module as generic as possible, which not only guarantees that they are usable with a wide variety of upstream information but also that the menu is highly adaptable to the changing run conditions at CMS. Conversions to a common scale ensure that comparisons can be performed irrespective of the subsystem that provided the trigger object.

In terms of implementation, the Phase-2 firmware is designed to operate at 480 MHz, a frequency that is twelve times the LHC clock, allowing for the efficient reuse of comparator and calculation logic. This is accomplished by pipelining objects and later combining the aggregated comparator results in a final step before arriving at a decision for a specific physics signature check. This approach is applicable not only for simple checks on individual quantities such as pT, eta, phi, z0, etc., but also for correlational quantities that involve calculations, such as invariant mass, ΔR, transverse mass, combined pT, charge, and others. Albeit for correlational checks, only one of the two involved object collections can be pipelined, while the other has to be available in parallel to form all possible correlation pairs within an event. The efficient pipelining technique we have implemented is a crucial aspect of maintaining routability of the design at such a high clock frequency.

The CMS collaboration has developed new generic ATCA processing boards capable of handling the data rates during high-luminosity operation. These feature either a Xilinx Virtex Ultrascale+ VU13P, VU9P or a Xilinx Kintex Ultrascale+ KU15P FPGA. Prototypes of our firmware currently exist for all three of them. While the algorithm implementation remains consistent across all prototypes, variations are observed in the interface design, the number of algorithms, and the distribution of input information across Super-Logic-Regions. The VU13P FPGA has been designated as the target for the final implementation, while the other boards are retained for testing and prototyping.

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