Universal test system for boards hosting bPOL12V DC-DC converters.

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On behalf of the CMS collaboration

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Abstract:

ECAL Barrel (EB) and MTD Barrel Timing Layer (BTL) subdetectors of the CMS are approaching series production of electronic boards, including voltage conditioning PCBs: LVR and PCC respectively. 2448 LVR and 864 PCC will be installed during LS3 of the LHC. These boards are hosting radiation-tolerant bPOL12V ASICs which convert a broad input voltage range into required voltage levels for microelectronics between 1.2 – 2.5 V. Each card must be tested multiple times at various production stages to ensure its quality. This contribution describes a methodology of testing bPOL12V conversion quality including the detection of instability regions at certain load levels.

Summary:

CMS phase II upgrade is approaching the series production of electronic components which will be installed during LS3 and must reliably operate in the HL-LHC era. Testing these electronic boards prior to installation is crucial to ensure the proper operation of subdetectors because maintenance and replacement of faulty boards is not foreseen within their lifetime.

There was a common decision in the CMS to use bPOL12V for the point of load DC-DC conversion. These ASICs convert 7-12 V supplied to the detector into 1.2-2.5 V required to supply microelectronics. EB and MTD BTL use them on boards conditioning voltage – Low Voltage Regulator (LVR) and Power Conversion Card (PCC) respectively.
We designed a universal testing methodology which will be applied to both mentioned PCBs. Testing equipment, validation conditions and data storage will be described in this contribution with a particular focus on instability regions detection of bPOL12V converters.

The test system architecture is presented in Figure 1. DMM with waveform acquisition is a key component to assess whether we are in the region of instability of the bPOL12V converter. It is acquiring output voltage with a 100 kHz sampling rate for a period of 20 ms. Based on standard deviation (SD) or pk-pk of this waveform we discriminate whether there are oscillations at certain operating points. Example comparison of stable and unstable operation is shown in Figure 2. Oscillations measured are periodic, sine-shaped signals, which are usually within 10-20 kHz range with a pk-pk value of up to 40 mV.

On top of the equipment, a dedicated Python software with a GUI was implemented, which may be used by unskilled personnel to perform a full test of a board. To assess the quality of PCBs, the program validates:

- Initial temperature and thermal equilibrium of the PCB
- Idle input current and output voltages
- Input current when all channels are disabled (enable pin of bPOL12V is used)
- Load regulation curve
- Conversion efficiency versus load curve
- Voltage SD versus load curve

For scalar values, we check whether values are within fixed (configurable) bounds. For load-dependent curves, we use a template curve fit to obtain a scalar value from the plot and then compare it with fixed bounds.
Each production board has its unique barcode and test data is stored in a relational database, which will be kept until the end of the lifetime of the detector. We expect to have a few measurements for each PCB, done at certain stages of production.

The test system was validated with the final PCB prototypes: 80 PCC boards and 52 LVR boards hosting 448 conversion channels in total. Based on that, preliminary bounds were determined that will be used in the factory acceptance test. Validation methods proposed not only determine completely faulty boards, but also boards that have significant deviation from the expected distribution (are outliers). These outliers will be assessed on the individual basis and, if the deviation does not prevent from using them, they are kept as spare parts.