lpGBT – Calibration of Analog Peripherals

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on behalf of the lpGBT team

TWEPP 2023 Link User Group Meeting

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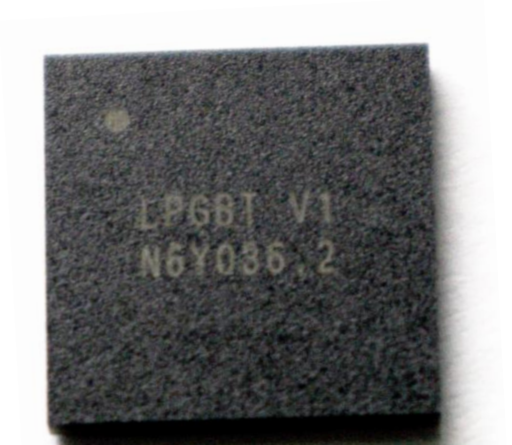
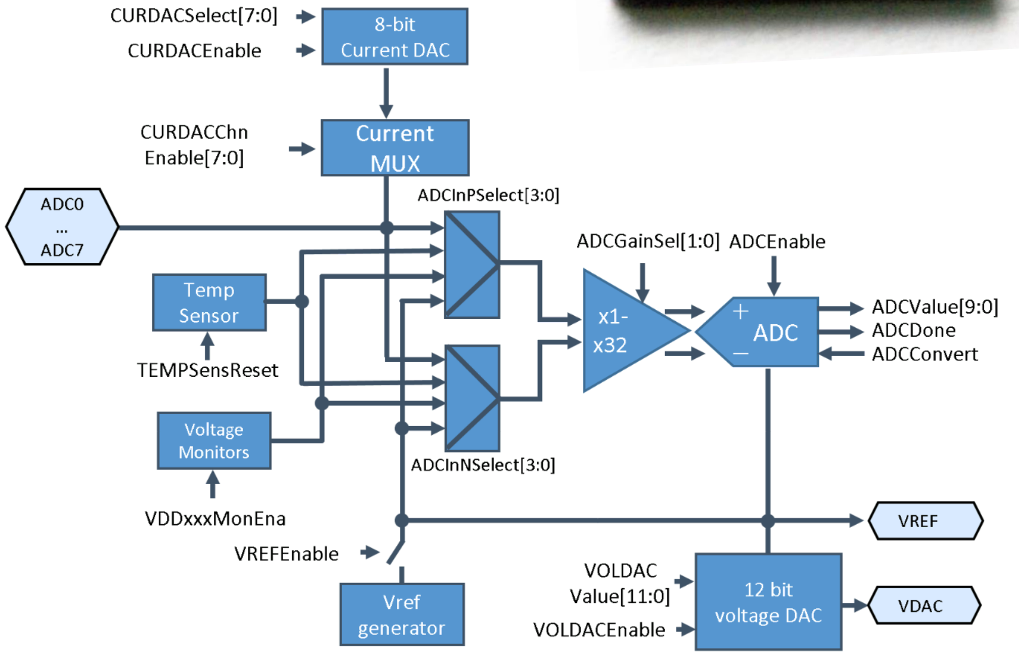
Motivation & Goals

- The lpGBT provides analog peripherals for experiment monitoring and control
  - Bandgap reference voltage generator
  - 16 channel, 10 bit ADC
    - 8 external inputs
    - Temperature sensor
    - Supply voltage monitor
  - 8 channel, 8 bit current DAC
  - 1 channel, 12 bit voltage DAC
- Calibration required for best performance
  - Process variations (chip-to-chip, wafer-to-wafer)
  - Temperature variations
- Today
  - Methods, Scope, Example, Issues





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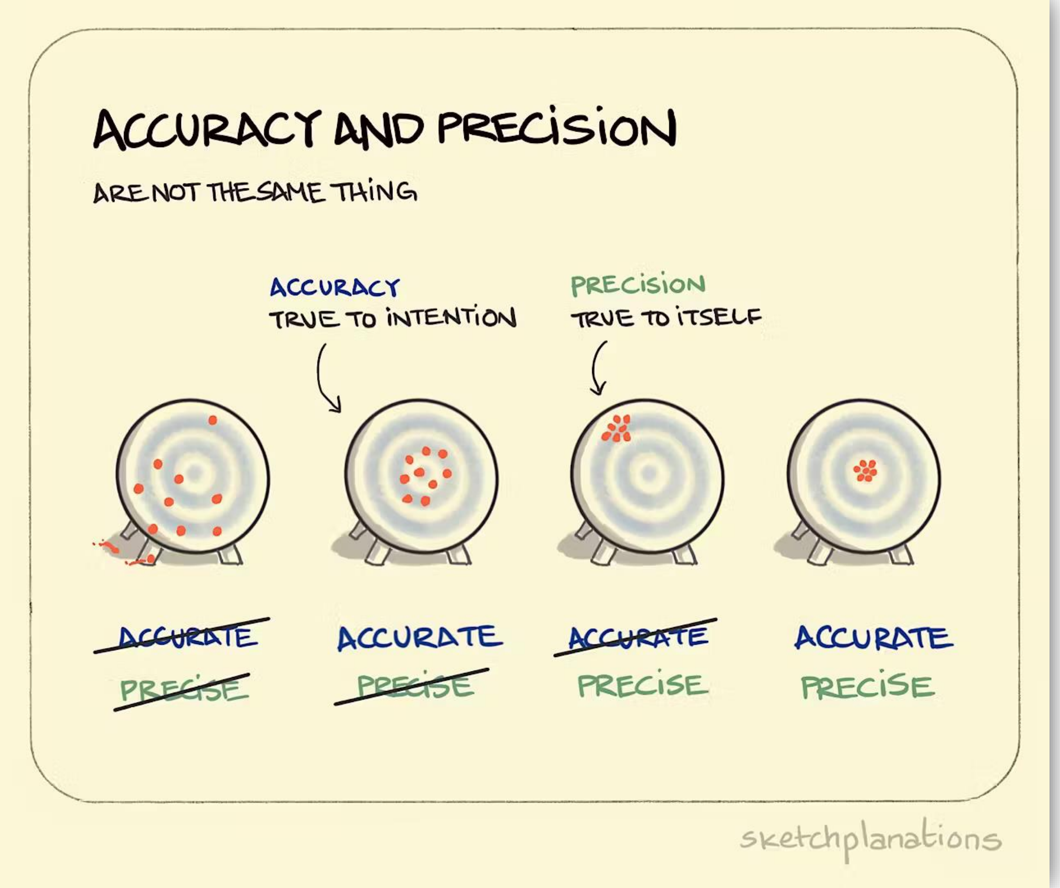
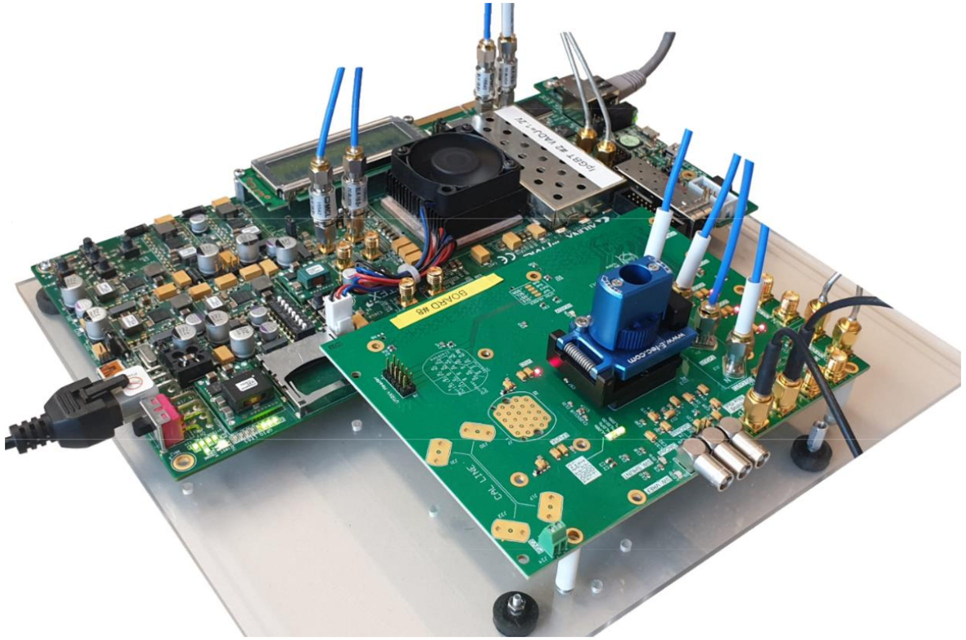
Motivation & Goals

- Goals of calibration effort
  - Define a range of environmental conditions where accuracy can be guaranteed
  - Develop the required procedures and per-chip calibration constants for users
  - Produce accuracy estimates for calibrated devices
  - Establish user access to this data
- Guided by JCGM 100:2008 (Guide to the expression of uncertainty in measurement)
  - Identification and assessment of all important contributors to final uncertainty budget
  - Long process (schematic and datasheet reviews, calculations, simulations, measurements, …)



Test System & Scope of Calibration

- Production testing was performed using lpGBT test system
  - Contains calibrated instrumentation for testing of analog peripherals
- Per-ASIC calibration measurements performed during volume production testing
  - At two temperatures (above and below 0°C)
  - At 1.20 V (only)
- Calibration data provided only for production-grade lpGBT v1 ASICs (2023)
  - No data available for pre-2023 samples (v0 and pre-production v1 devices)
- No per-device data available to calibrate against other parameters (e.g. VDD)



[1] J. Mendes et al: "lpGBT Tester: an FPGA based test system for the lpGBT ASIC", TWEPP2019
[2] N. Guettouche et al: "The lpGBT production testing system", TWEPP2021

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Calibration Models

- Choice of calibration model is important
- Models chosen for lpGBT analog subsystem
  - Linear models – used for single-point process/temperature calibration
    - Fixed offset (process), fixed slope (temperature)
  - Temperature-dependent linear models – used for transfer function corrections
    - Offset and slope have linear temperature dependence
- Already with these models, sensitivity to other variables dominate uncertainty
  - No improvement achieved by higher order calibration
- Calibration coefficients also take care of 'unit conversion'
  - ADC LSB → Volt, Ampere → LSB, Voltage → °C

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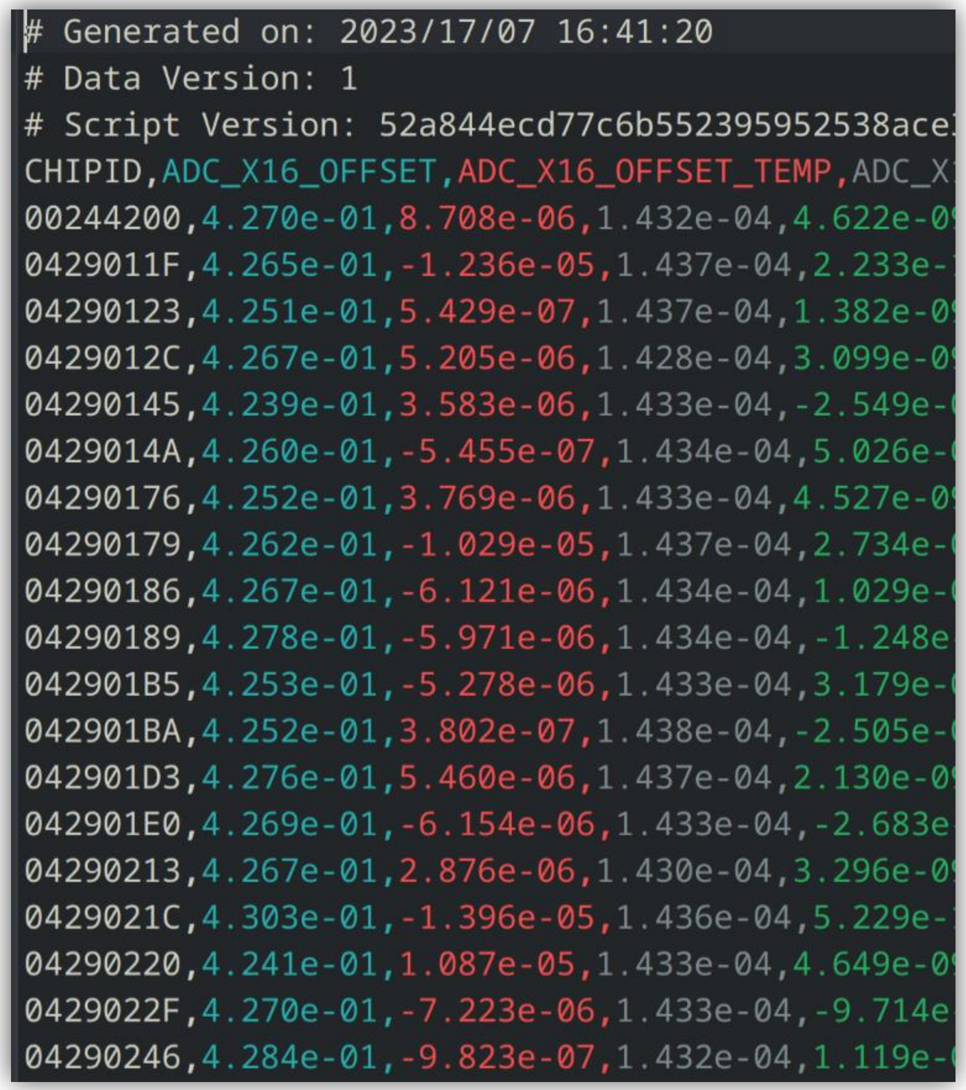
User Access to Calibration Data

- Reminder: Calibration data is NOT stored in eFuses
- Instead, CHIPID is used to look up calibration data
  - Database for all ASICs available online
  - May be updated/amended in the future
- Procedures for performing calibration are documented in the manual
- Reference implementation of each procedure available in the *lpgbt_control_lib* (lpGBT driver library)
  - Also used for validation of the calibration



```
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# Data Version: 1
# Script Version: 52a844ecd77c6b552395952538ace
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04290123,4.251e-01,5.429e-07,1.437e-04,1.382e-0
0429012C,4.267e-01,5.205e-06,1.428e-04,3.099e-0
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0429021C,4.303e-01,-1.396e-05,1.436e-04,5.229e-
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04290246,4.284e-01,-9.823e-07,1.432e-04,1.119e-
```

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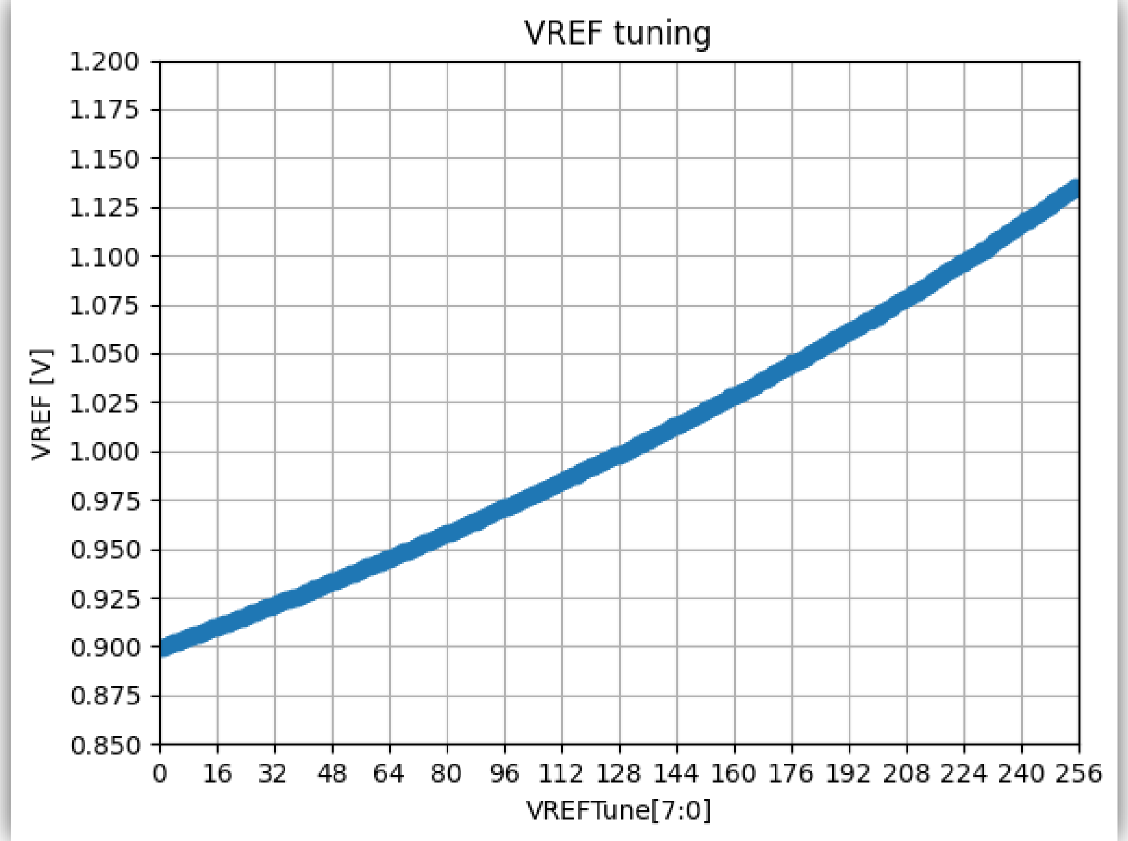
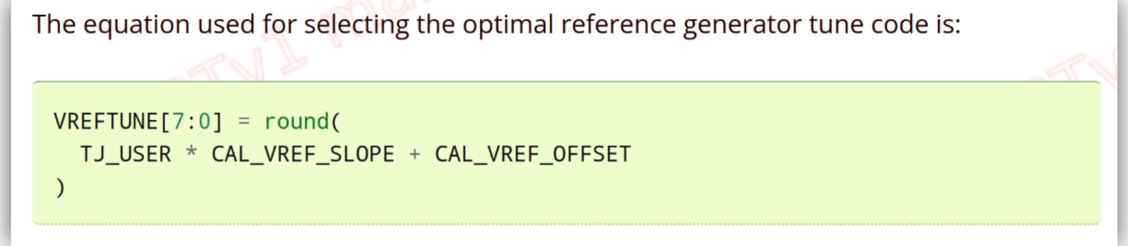
Example: Reference Voltage Generator

- Bandgap reference + voltage multiplier with 8 bit control
- Tune value calculated using estimated junction temperature
- Uncalibrated error is large, dominated by
  - Bandgap parameter spread
  - Temperature sensitivity
- Calibrated error dominated by
  - Supply voltage uncertainty
  - Uncertainty of junction temperature




The equation used for selecting the optimal reference generator tune code is:

```
VREFTUNE[7:0] = round(
  TJ_USER * CAL_VREF_SLOPE + CAL_VREF_OFFSET
)
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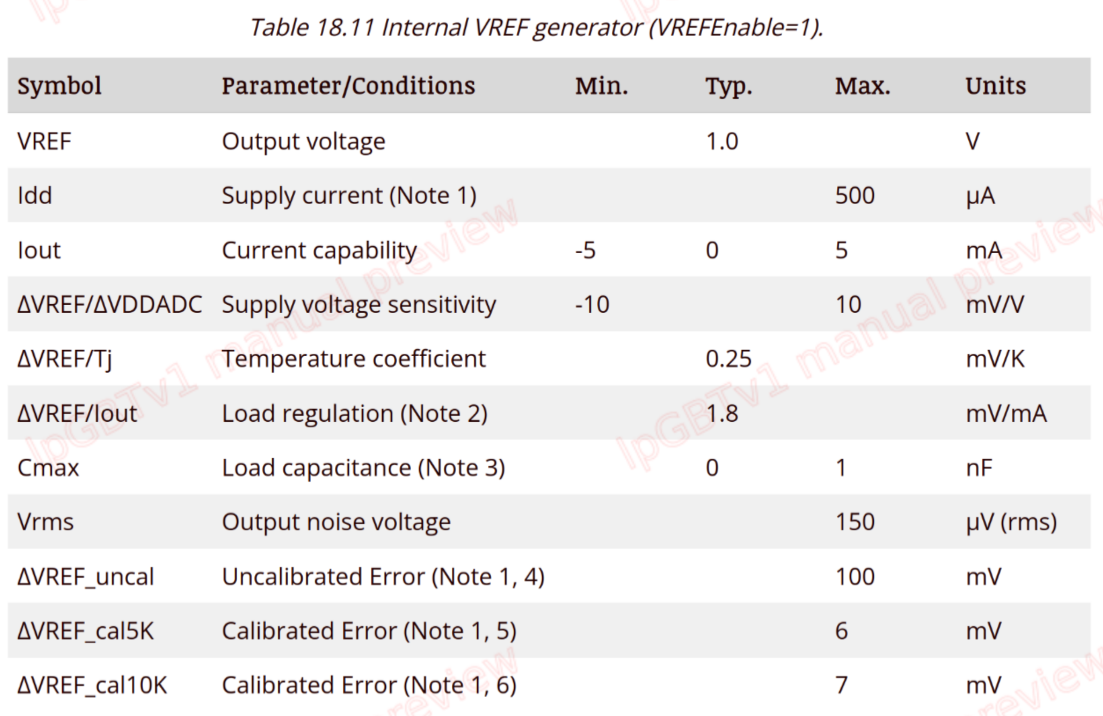
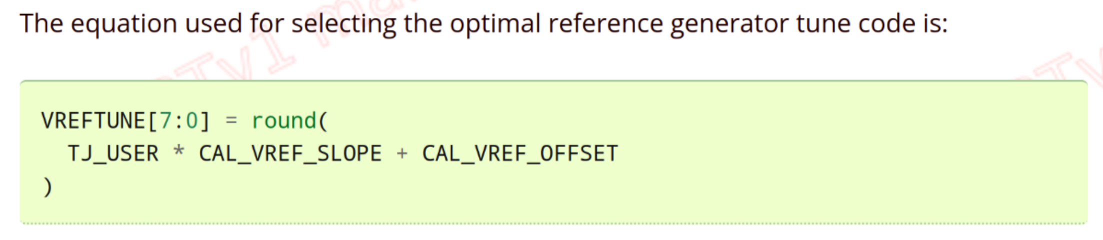


Table 18.11 Internal VREF generator (VREFEnable=1).

Symbol	**Parameter/Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
VREF	Output voltage		1.0		V
Idd	Supply current (Note 1)			500	µA
Iout	Current capability	-5	0	5	mA
ΔVREF/ΔVDDADC	Supply voltage sensitivity	-10		10	mV/V
ΔVREF/Tj	Temperature coefficient		0.25		mV/K
ΔVREF/Iout	Load regulation (Note 2)		1.8		mV/mA
Cmax	Load capacitance (Note 3)		0	1	nF
Vrms	Output noise voltage			150	µV (rms)
ΔVREF_uncal	Uncalibrated Error (Note 1, 4)			100	mV
ΔVREF_cal5K	Calibrated Error (Note 1, 5)			6	mV
ΔVREF_cal10K	Calibrated Error (Note 1, 6)			7	mV



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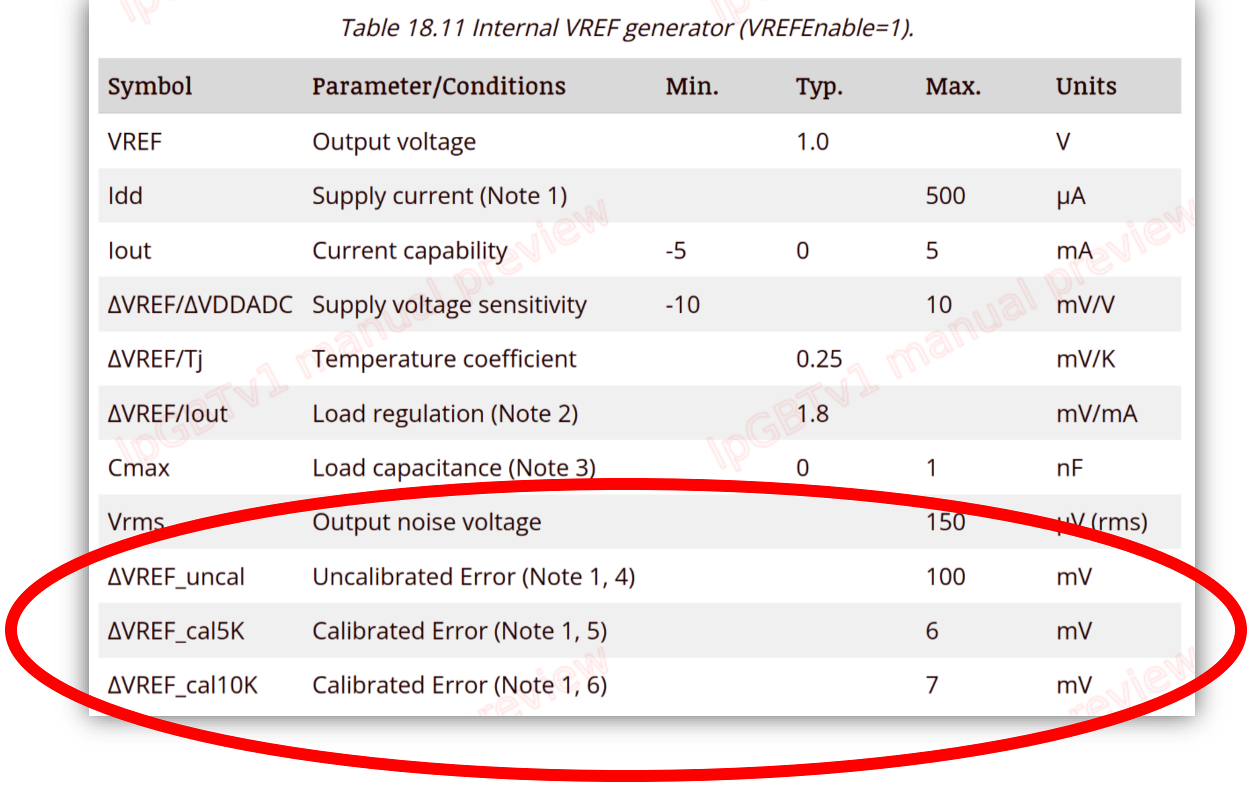

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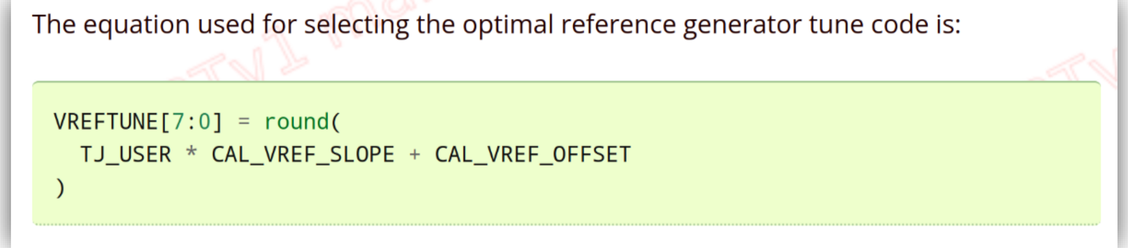

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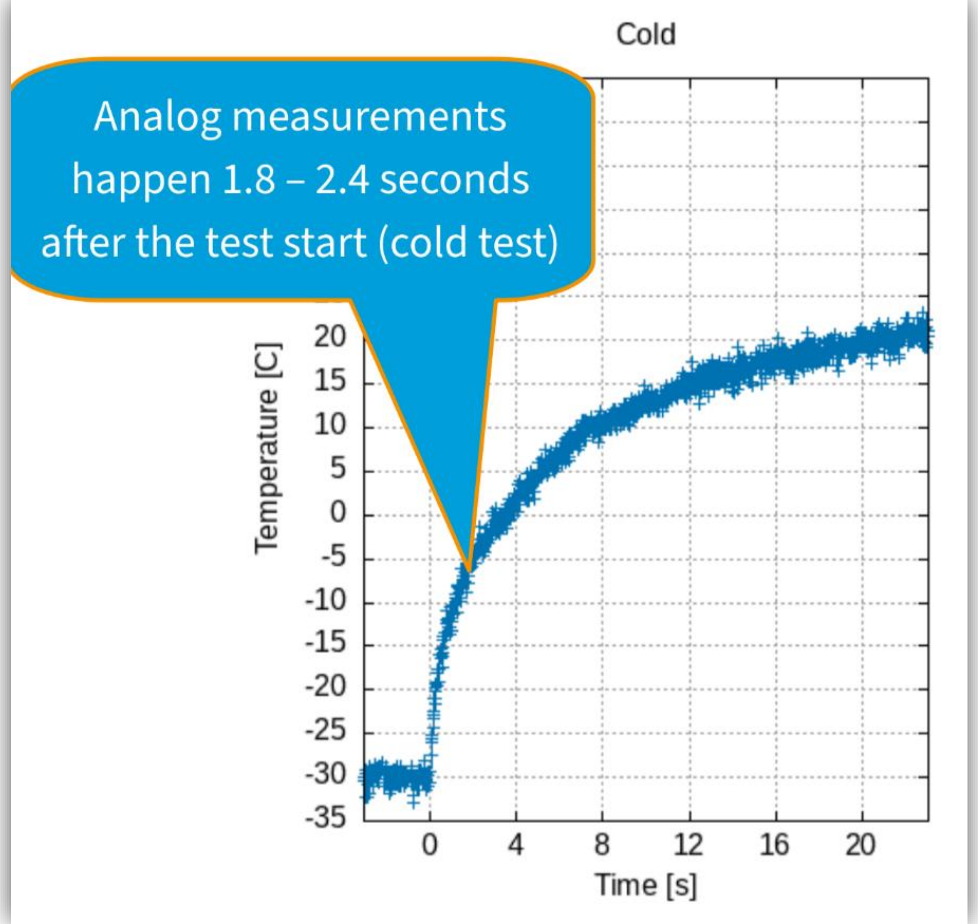
Thermometry

- Accurate calibration depends on accurate temperature measurements
  - During production testing
  - During use of ASICs
- Steady-state and transient analysis of production testing flow performed
  - Characterization of ASIC thermal properties
  - Large contributers to calibration uncertainty budget
- Users will also need to estimate the temperature of the ASIC!
  - Raising questions for applications that want to accurately <u>measure</u> temperature



Analog measurements happen 1.8 – 2.4 seconds after the test start (cold test)

Analysis of transient temperature behaviour during volume testing

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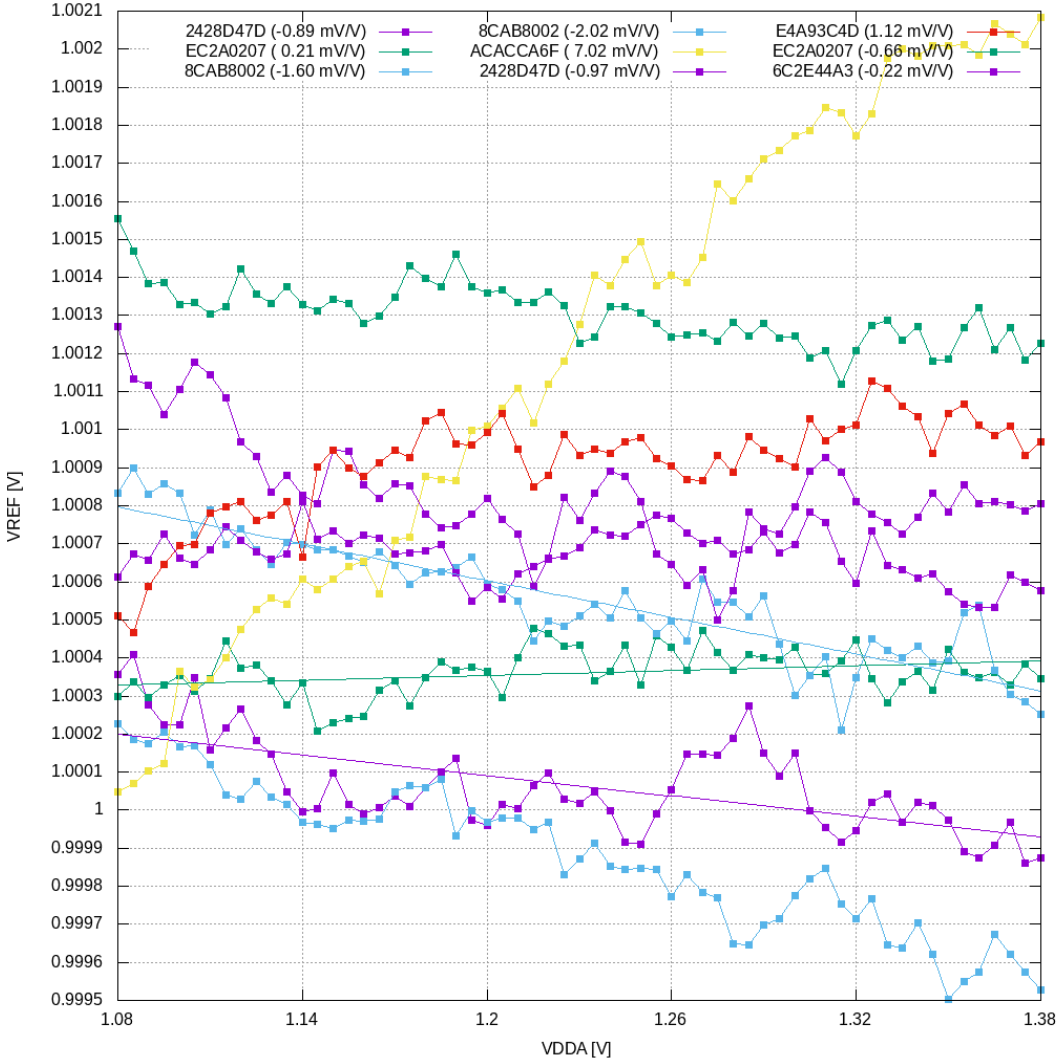
Supply Voltage Sensitivity

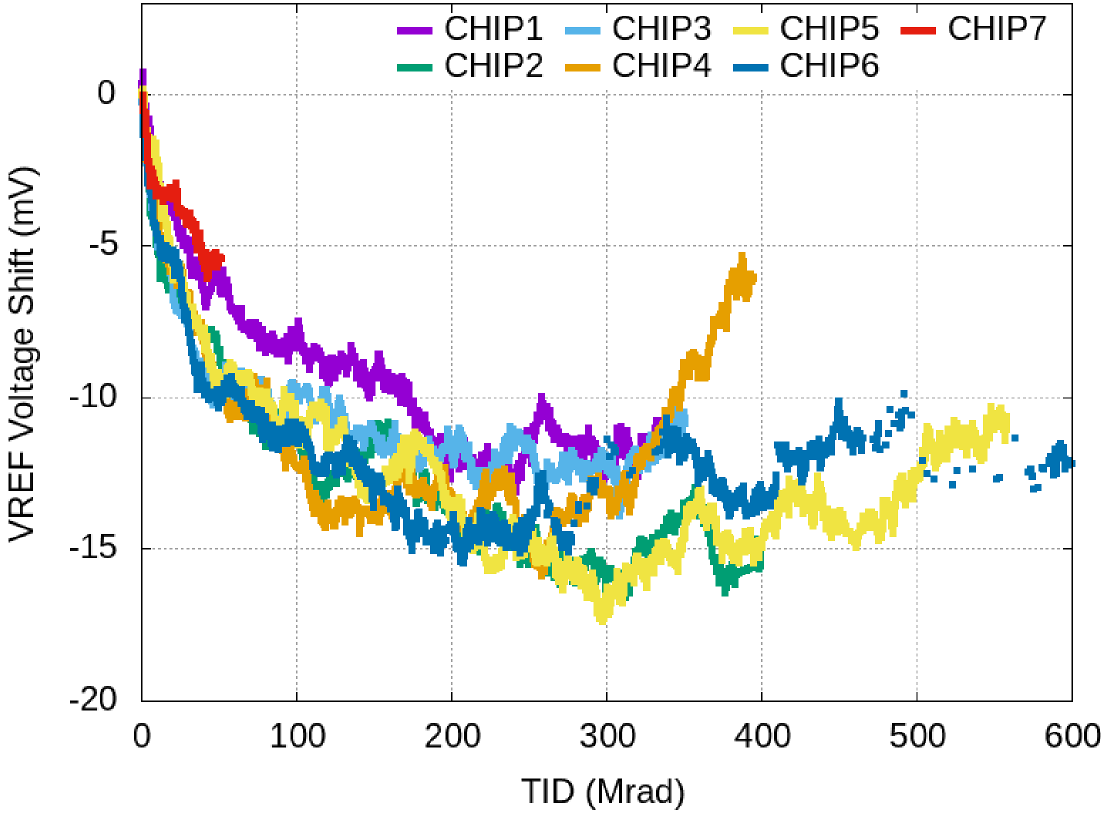
- Supply voltage largest remaining factor after applying calibration
- Explicitly not in scope of end-user calibration
  - Large variability
  - Accurate in-situ measurements usually not available
  - Change of VDD always coupled to temperature (VDD → P_{diss} → T_j)
- Characterization still required and performed
  - Indicative figures available in the manual
  - Worst-case VDD sensitivity considered for uncertainty assessments



Sample supply sensitivity characterization data

Radiation Response

- TID-induced changes will compromise the accuracy of calibration
- Had to remain outside the scope, due to limitations of our TID campaigns
    - Temperature sensitivity
    - Dose rate sensitivity
    - Annealing (bias & temperatures)
    - Sensitivity to displacement damage
    - Variability between chips, wafers, batches
- Recommendation: Use pre-irradiation measurements as reference values, and expect gradual changes (loss of absolute calibration and accuracy) over time



Typical X-ray radiation response of the reference voltage generator (indicative only)

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Summary

- Calibration effort for production lpGBT v1 devices was concluded in 2023
    - Identified achievable performance and design limitations
    - Key sources of uncertainty: thermometry, supply sensitivity, radiation
- Procedures and data now available to all users
    - Documentation: https://lpgbt.web.cern.ch/lpgbt/v1/analog.html#calibration
    - Electrical Specs: https://lpgbt.web.cern.ch/lpgbt/v1/electricalCharacteristics.html
- Feedback is welcome & appreciated!
    - Interested in applications and if calibration as provided is useful
    - LpGBT support forum / mailing list: https://lpgbt-support.web.cern.ch/

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Backup

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Lessons Learned

- Accuracy goals and how they can be achieved need to be considered early
  - Question of system design as much as circuit design!
  - 'Designing a 10 bit ADC' vs. 'Achieving 10 bit-level accuracy' - <u>very</u> different challenges!
  - Otherwise: System may fall short of silent expectations!
- Test system performance must be well known and trustworthy
  - Requires its own calibration and qualification effort!
- Thermometry very challenging aspect of calibration
  - Precise measurements of junction temperature
  - Analysis of transient effects (e.g. during ASIC handling)
    - Often not enough information and/or time available to carry out these studies
    - In these situations, must assume large uncertainty → negative impact on total accuracy
- Providing calibration guarantees is VERY challenging when TID is involved
  - Too many confounders, not aware of a viable analysis/qualification approach

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