EUROPRACTICE

Technology update for the HEP community via the EUROPRACTICE services

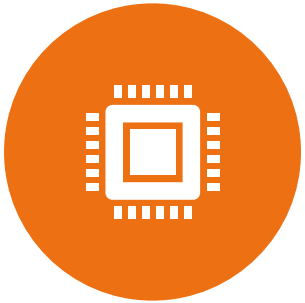
Paul Malisse, imec

European Commission

EUROPRACTICE has received funding from the European Unions H2020 Framework Programme for research, technological development and demonstration under grant agreement No 825121

THE 3 PILLARS OF THE EUROPRACTICE SERVICE

- EUROPRACTICE is a true one-stop shop that lowers the barrier to access all services that you need to design and fabricate electronic circuits and smart integrated systems:



FABRICATION SERVICES

DESIGN TOOLS

TRAINING & WEBINARS

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TODAY

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TODAY's Foundry Offerings

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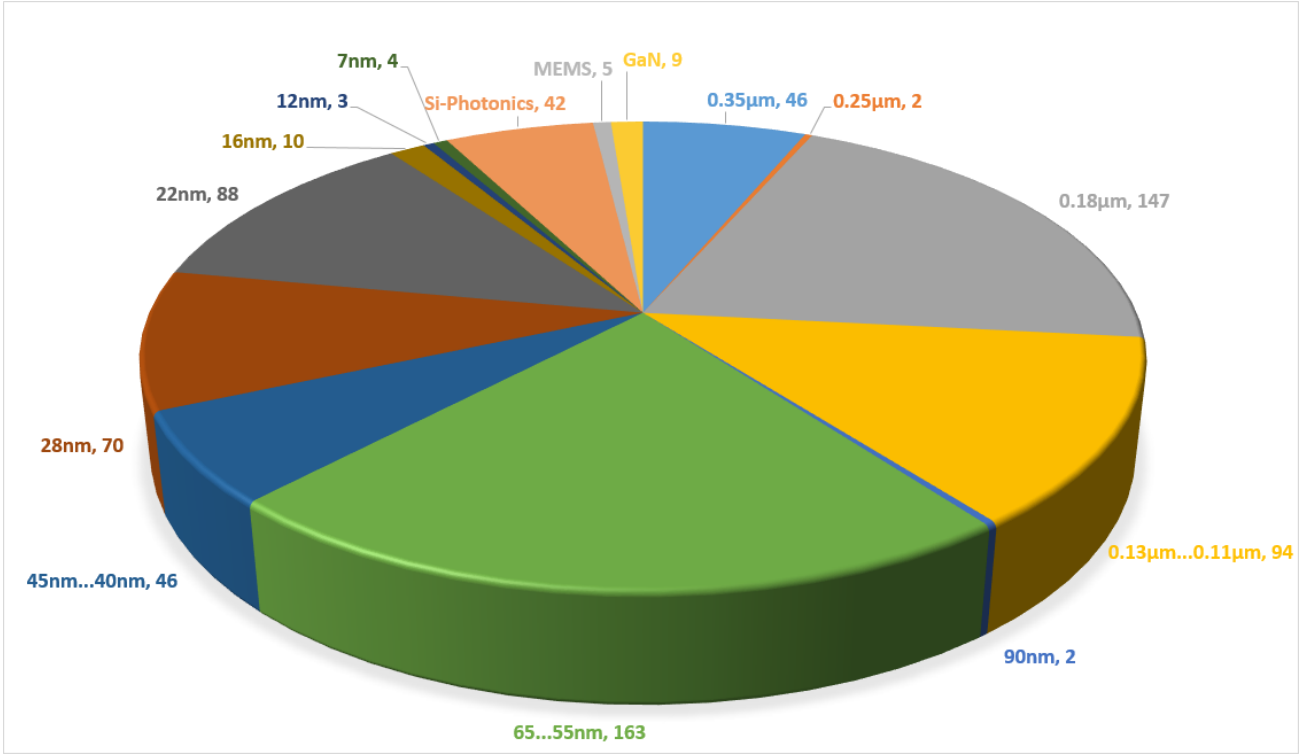
TODAY's ASIC technology usage - anno 2022



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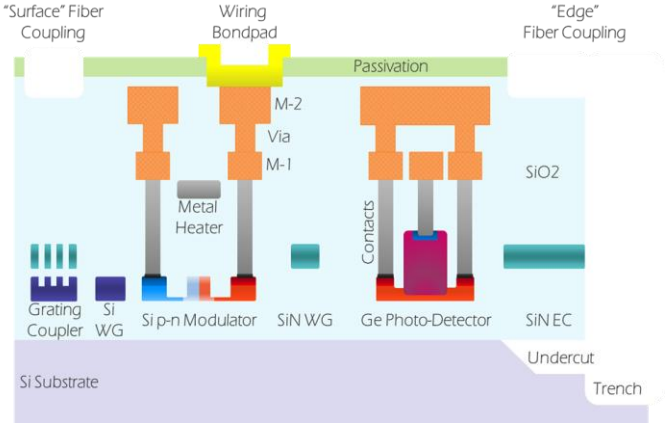
Update on Photonics MPW

- New **PDK release v. 3.3.6** – with improved cells and documentation
  - New PDK release coming 2024

- Upgrade of iSiPP200 platform: **iSiPP200N**
  - LPCVD SiN low loss WG
  - LPCVD SiN CWDM
  - LPCVD edge coupler



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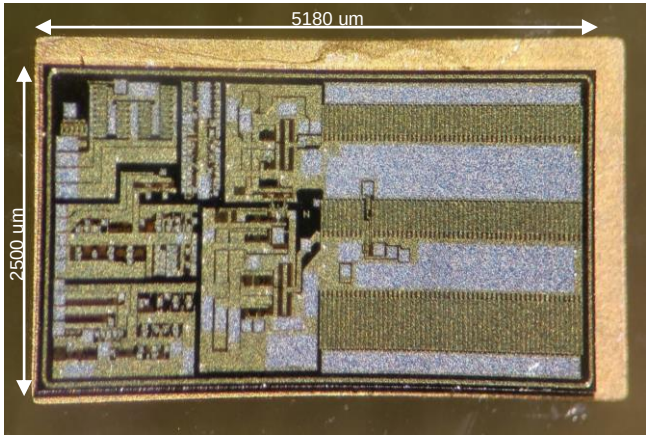
Update on GaN-IC MPW

- New **650V PDK release v. 2.2.0** – with improved cells
  - New PDK release coming 2024 with RDL for wire bonding

- Highly complex demonstrators successfully characterized
  - HVGaNCon HB with integrated drivers and control circuits - all-GaN
  - Monolithic HB 200V for space
  - 400V, 1MHz, 200W high-efficiency totem-pole PFC converter*



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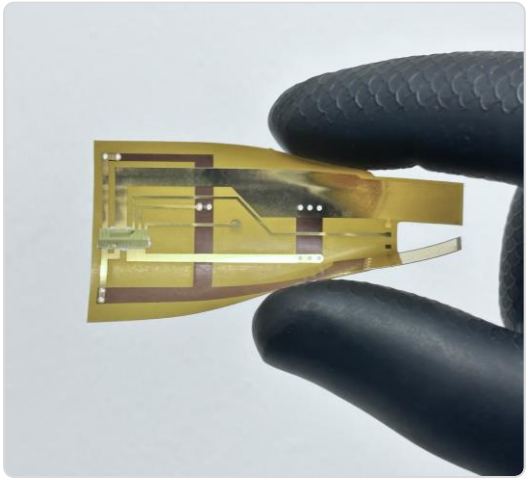
Pragmatic's Flexible Integrated Circuit (FlexIC)

Pragmatic Semiconductor (Cambridge, UK), the world leader in ultra-low-cost flexible integrated circuits



FlexICs use thin-film transistor (TFT) technology in combination with conventional semiconductor processing to deliver the world's most complex flexible circuits.

Ultra-thin
~30µm

Flexible
5mm bend radius

Low cost

Shock resistant

n-type FET

Metal
4 layers

Channel Dimension
600nm

Turnaround time
~6 weeks

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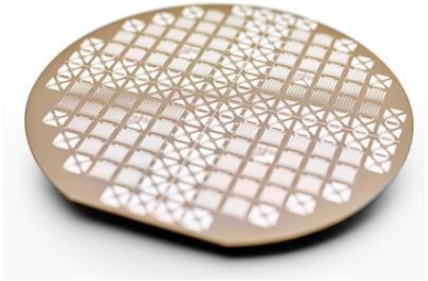
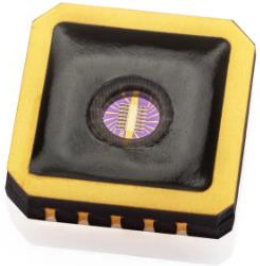
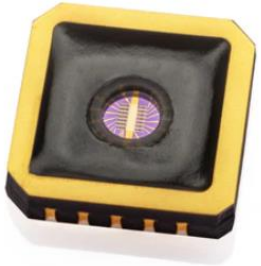
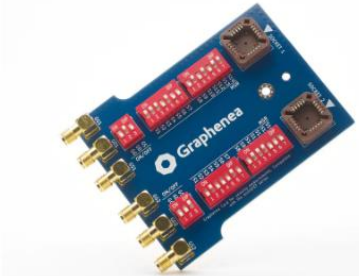
Cooking - Graphene MPW

Graphenea









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TSMC FinFet Program

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TSMC FinFet program

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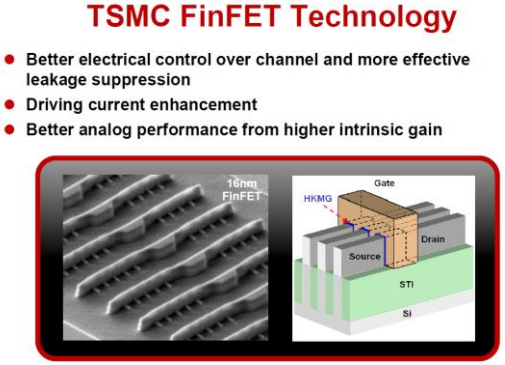
TSMC FinFet program: PROGRAM HIGHLIGHTS

- Offering the Industry's Most Successful FinFET Technology Family to EUROPRACTICE-member Universities
  - Starting with TSMC N16 and N7 (including RF)
  - Tapeout and manufacturing services
  - Incentivised price offerings
- Design Collaterals for Both Teaching and Research
  - N7 and N16 Design Collateral: For test chip MPW
  - N16ADFP (Academic Design Foster Package): For Teaching Purpose Only



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TSMC FinFet program: ACCESS

- Academia
  - Application for 1, 2 or 3 packages
  - Approval by TSMC
  - NDA & Security questionnaire
  - Focus is University research, publication oriented
- R&D
  - Grey zone
  - Industrial NDA
  - Ambition to offer ADFP package for training mission at R&D

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CAPACITY situation

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Slowing Industry Conditions Temporarily Eases Supply Strain in 2023 for Silicon and SOI Wafers

January 10, 2023

Investments in increased capacity not expected to alleviate strain until 2024-2025

Ref: Techcet

- The perfect storm is over – no more surprise effect
- Strong focus on forecasting – more control
- Overseas expansion
- 65nm remains the most strained technology but for a different reason now

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MPW reservation Flow

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MPW reservation challenges

- The perfect storm is over –

Lessons learned - also for MPW

- 180 stopped, 65 highrunner
- 2021 and 2022 very stressful
- Increased operational tasks (for example Export …)
- IMEC-TSMC commitment to get design on the run based on two condition
  - Reservation between 4 and 8 months before deadline
  - Touchpoint 2 months before deadline

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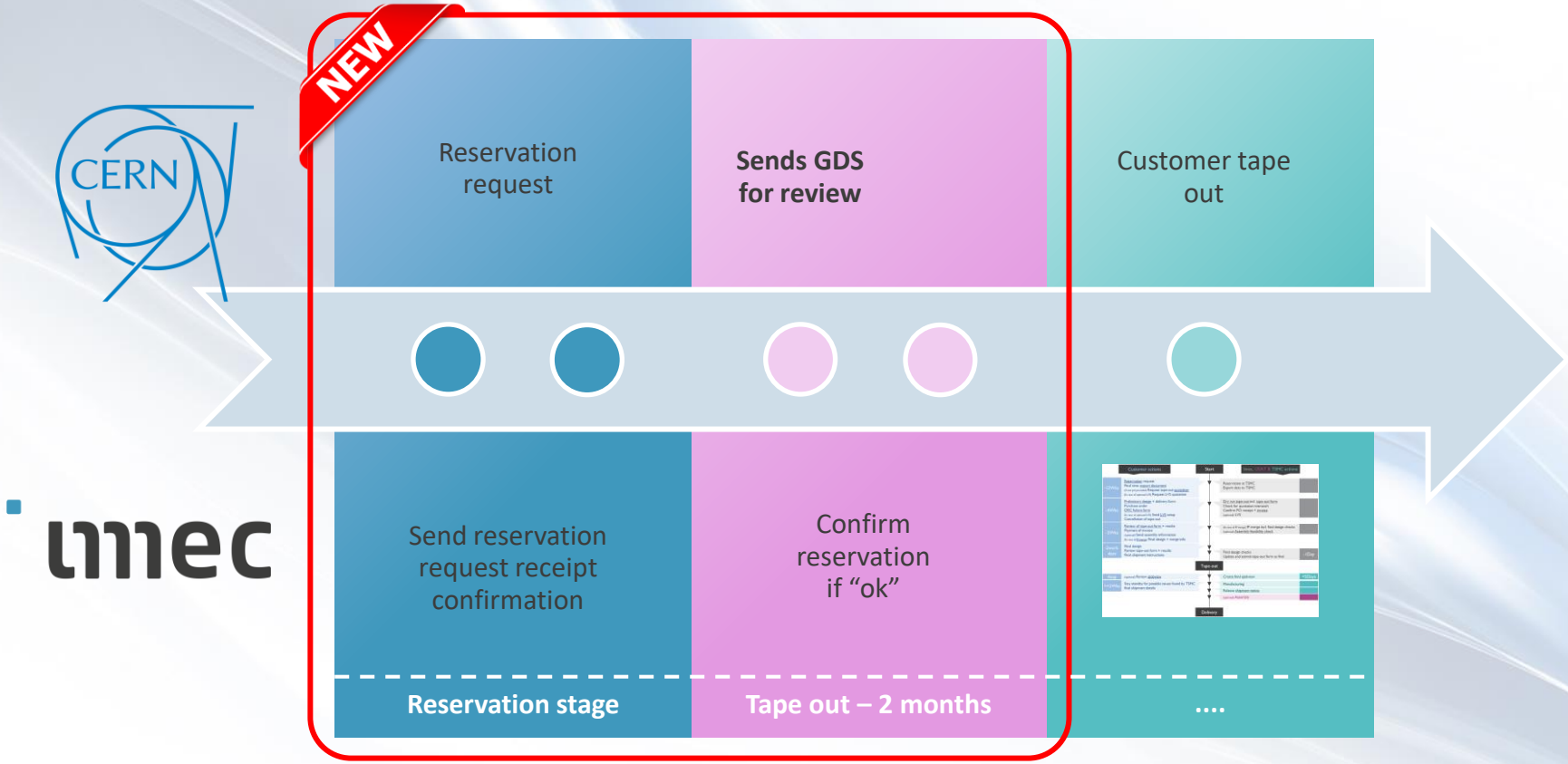
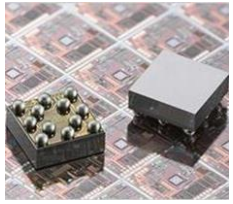
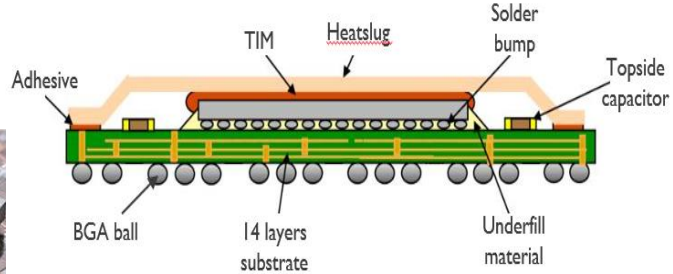
New flow


NEW
Reservation request
Sends GDS for review
Customer tape out
Send reservation request receipt confirmation
Confirm reservation if “ok”
Reservation stage
Tape out – 2 months
....

TODAY's assembly techniques

- Standard packages are available and used frequently
- Complex circuits and technologies require more advanced assembly techniques.
  - Wire bond Ball Grid Array's
  - Wafer Level Chip Scale Package (WLCSP)
  - Flip Chip Ball Grid Array's with complicated substrate design





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THE ECONOMICS

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INTRODUCTION OF MFU as from 28nm

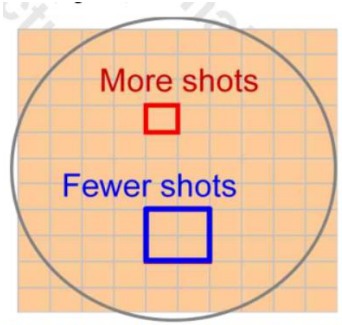

Figure 3: Number of shots to create dice on a wafer.

MFU Price Adjustment		
Actual MFU	NTO on and after 1/1/2020	
	≤ 28nm & ≥ 6nm	5nm & 4nm
MFU≥95%	-3%	-3%
90%≤MFU<95%	-2%	-2%
85%≤MFU<90%	-1%	-1%
80%≤MFU<85%	0%	0%
75%≤MFU<80%	1%	1%
70%≤MFU<75%	2%	2%
65%≤MFU<70%	3%	3%
60%≤MFU<65%	4%	4%
55%≤MFU<60%	5%	6%
50%≤MFU<55%	6%	8%
45%≤MFU<50%	8%	10%
40%≤MFU<45%	10%	12%
35%≤MFU<40%	12%	16%
30%≤MFU<35%	14%	20%
25%≤MFU<30%	32%	50%

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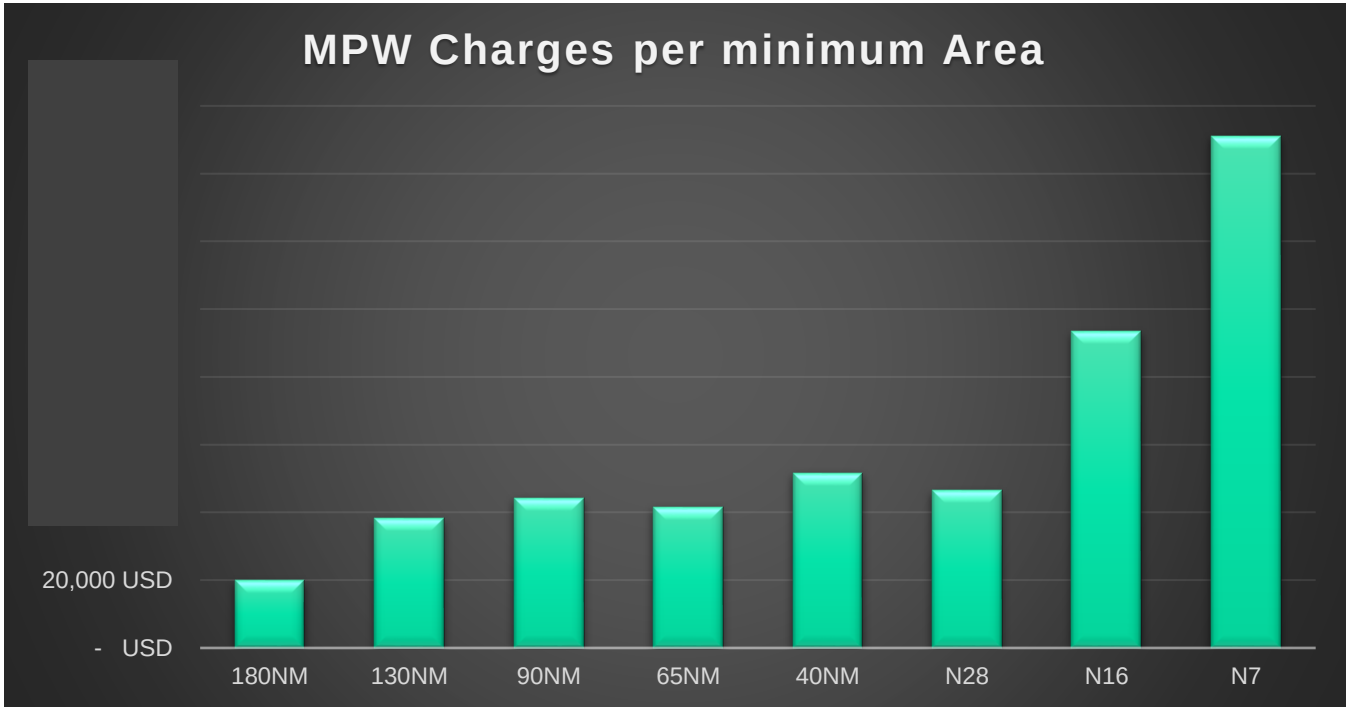
FinFet MPW are more expensive – MASK impact



Budgetary numbers

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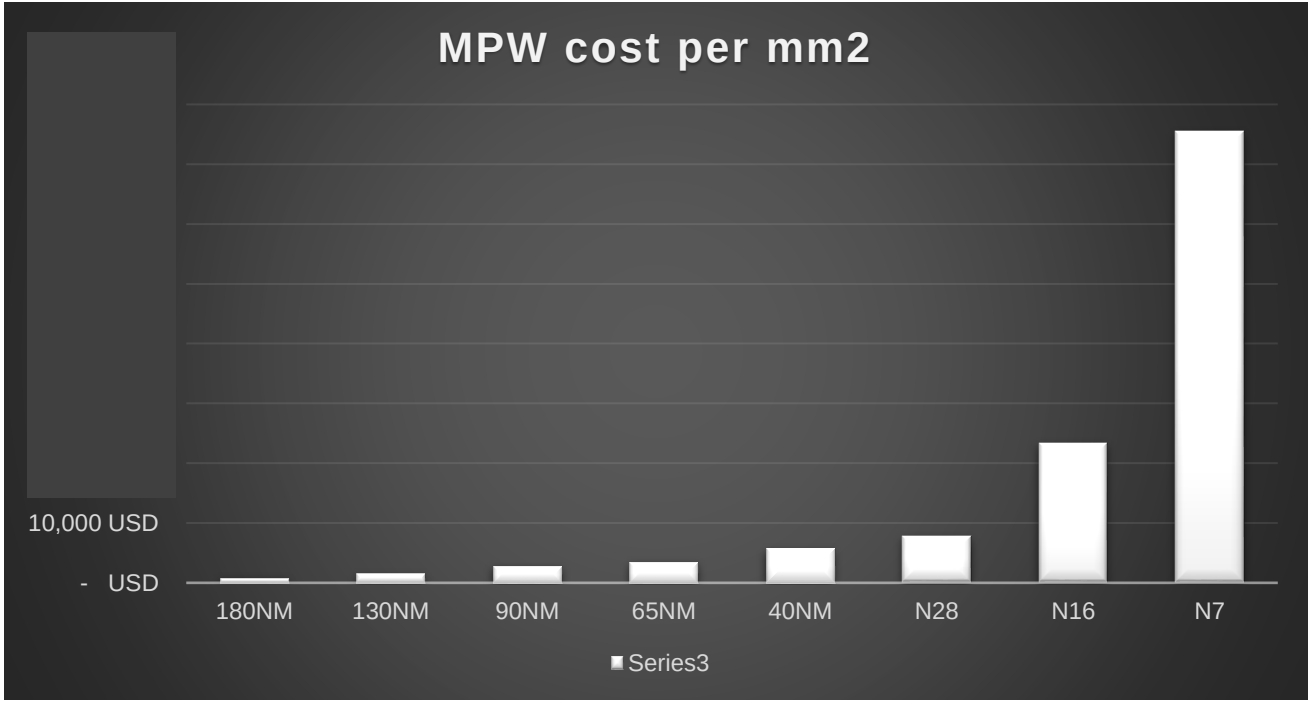

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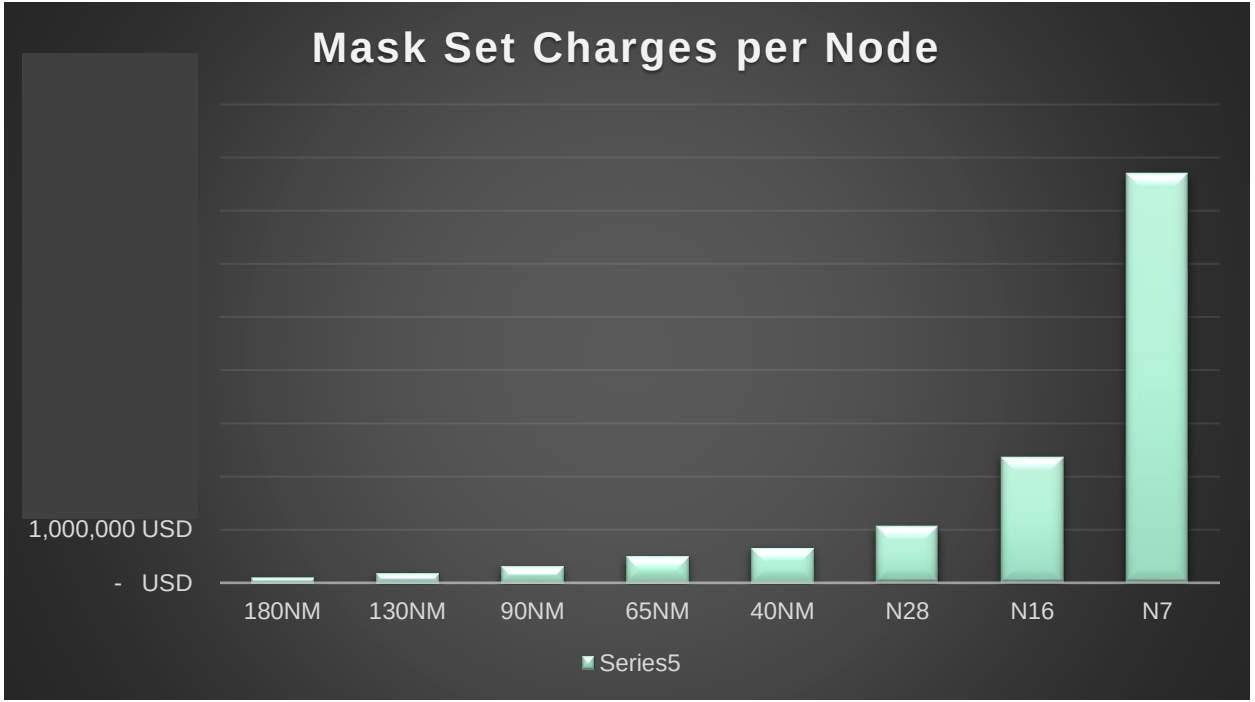
MASKS EVOLUTION



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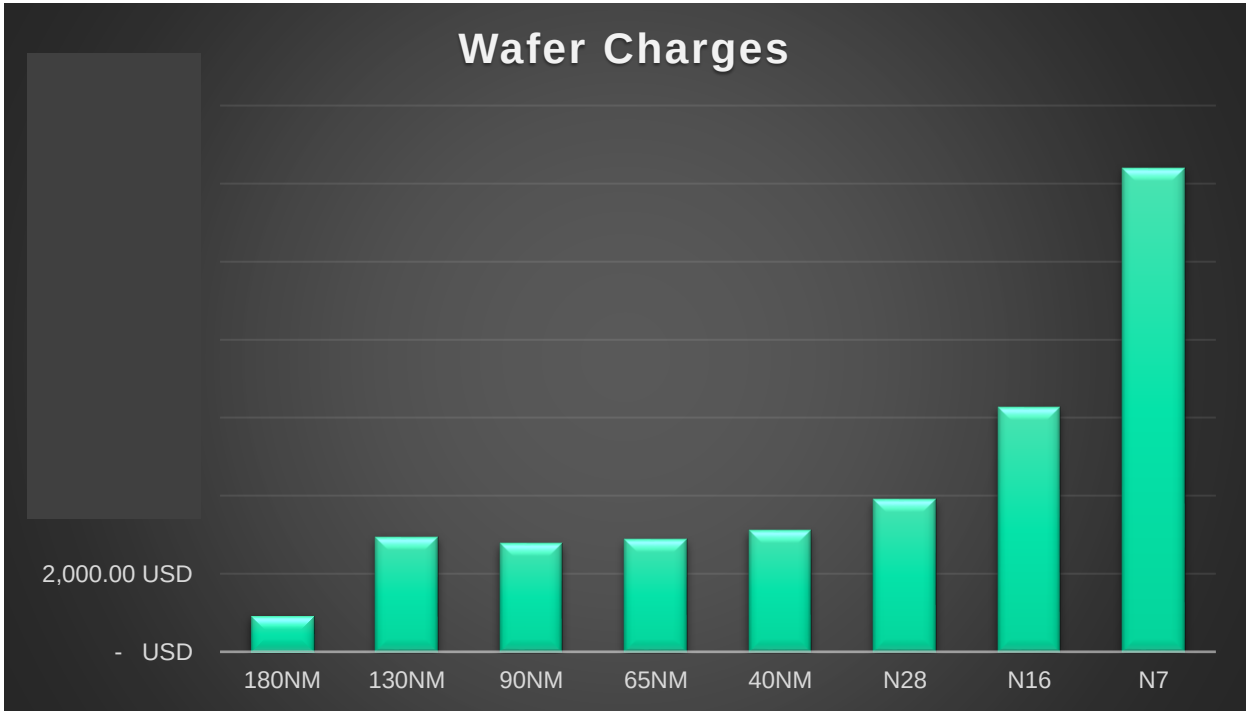
Normalized wafer charge for a fixed nr of METALS



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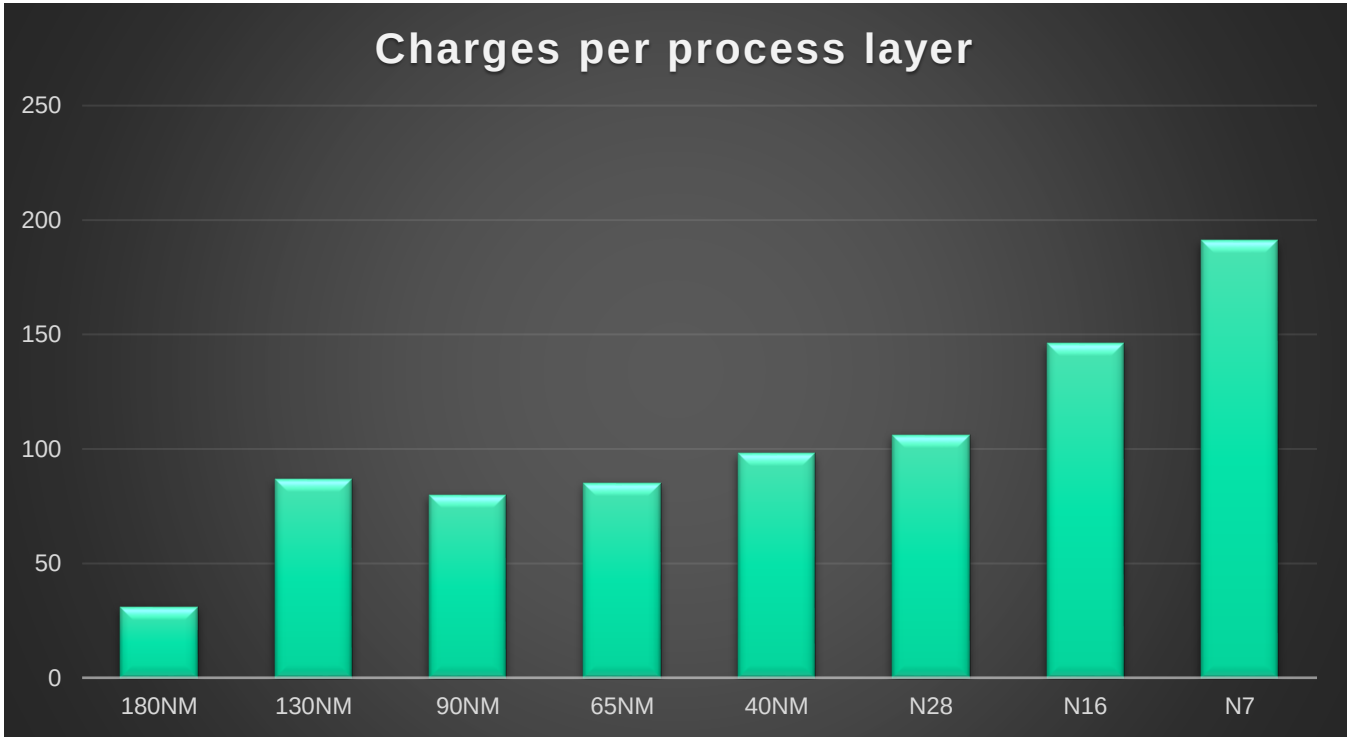
Normalized towards process layers



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THE NEXT LEVEL

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MORE than SILICON: New Assembly Techniques

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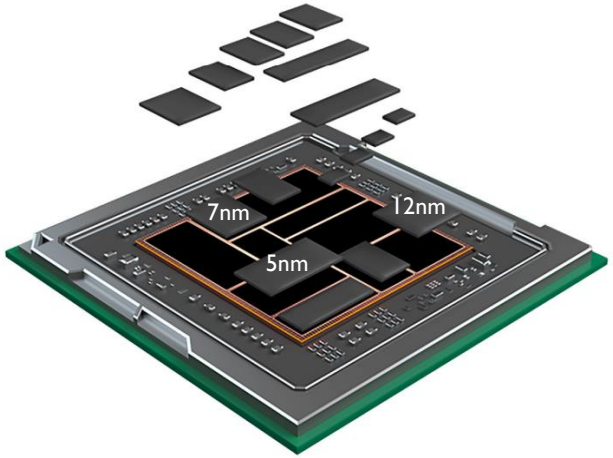
MORE than SILICON: CHIPLETS

- Different ASIC, Different TEAM
- Different Semiconductor and foundries combinable
- Cost optimization
  - Higher Yield (KGD)
  - HW Reuse
  - Dedicated technology for dedicated functions
- System Flexibility
  - customized and upgraded easily
- Reliable - Test coverage
- Shorter Time to Market - Modularity
- Performance scaling



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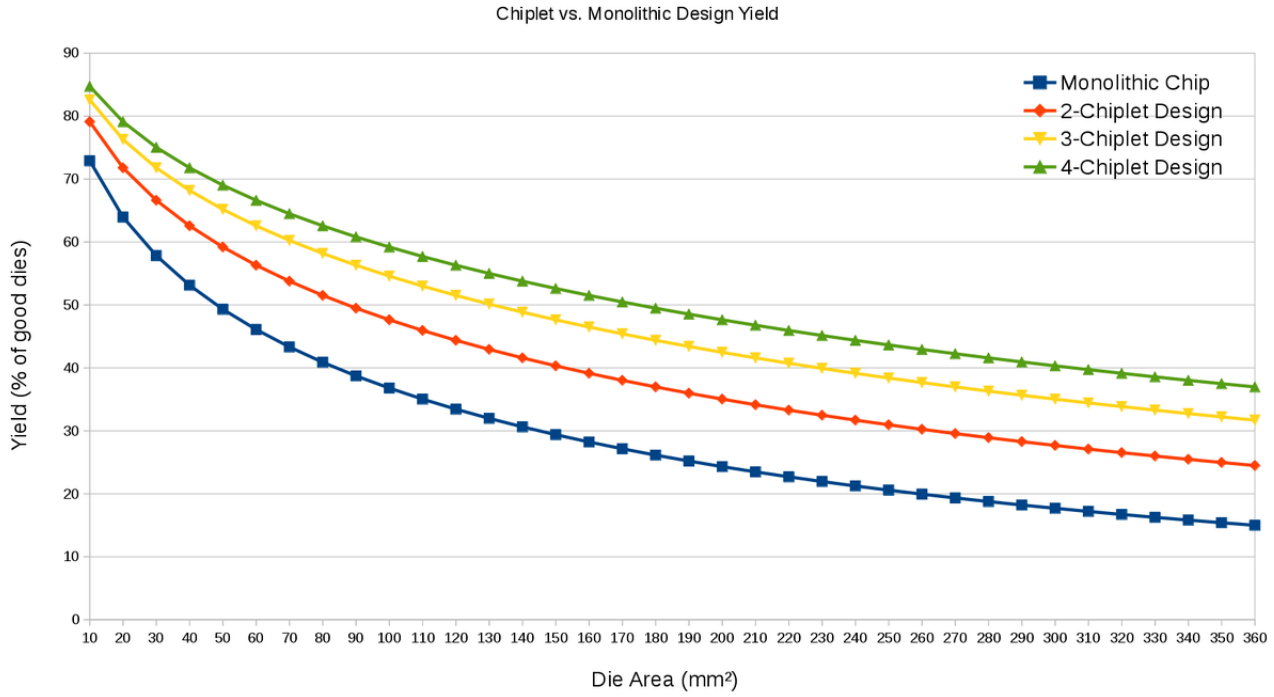
MORE than SILICON: CHIPLETS



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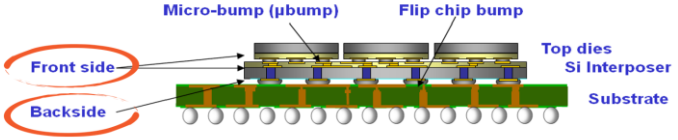
MORE than SILICON: COWOS

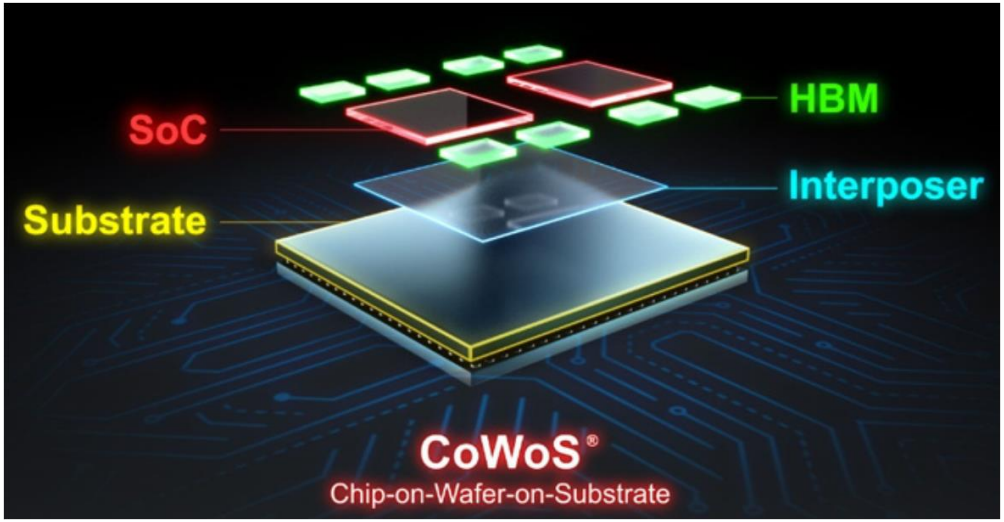
CoWoS (Chip on Wafer on Substrate), *also known as **TIS** – Through Interposer Stack*

- A 2.5D advanced packaging technology offered by TSMC
- Incorporates multiple dice side-by-side bonded using micro-bumps on a silicon interposer
- Uses TSVs on silicon interposer to connect to package substrate using C4 bumps



Front Side Interconnect – interconnect between top dies (e.g. HBM dies) to the silicon interposer using micro-bumps.

Backside Interconnect – interconnect between the silicon interposer (with TSV) to the flipchip bump and to the package substrate



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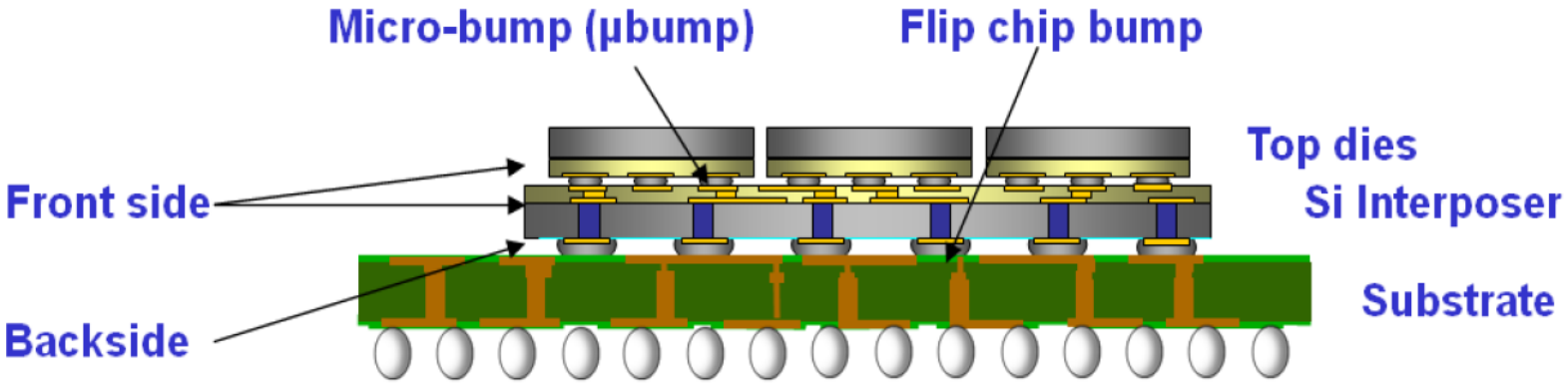
MORE than SILICON: COWOS

- **CoWoS** (Chip on Wafer on Substrate), *also known as* ***TIS*** *– Through Interposer Stack*



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CONCLUSIONS – The REALITY

- **MORE ADVANCED TECHNOLOGIES ARE IN REACH**
- **ASSEMBLY PROCESSES BECOMING functional part of the component**
  - **Performance, Economics, Form Factor, Security of IP**
- **NRE's will become even more dominant for smaller projects**
- **CO-DESIGN and VERIFICATION becoming more important**
  - **New Tool flows**
  - **New Skillsets**

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QUESTIONS

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