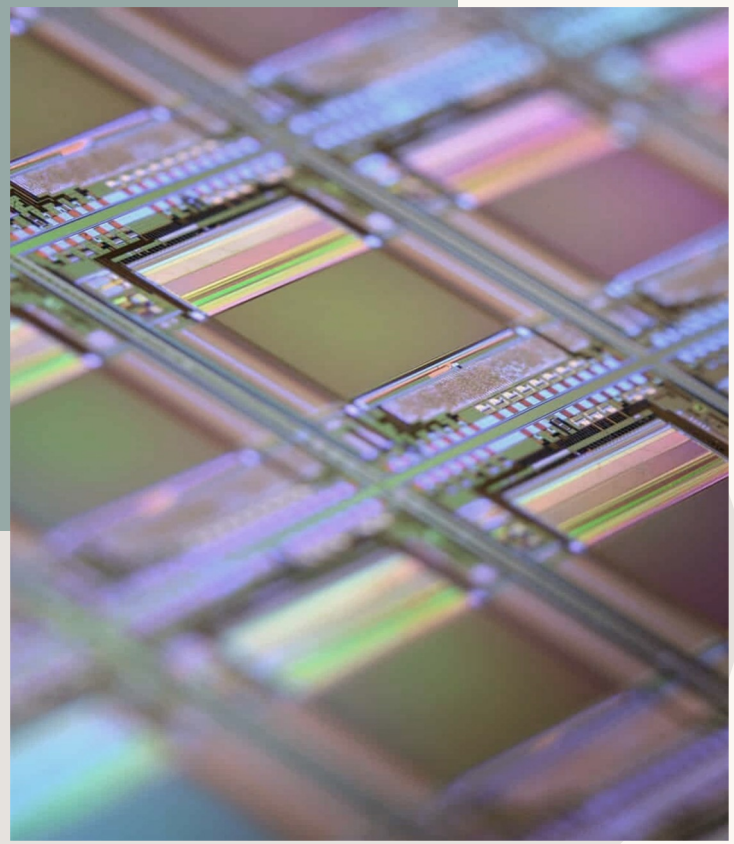
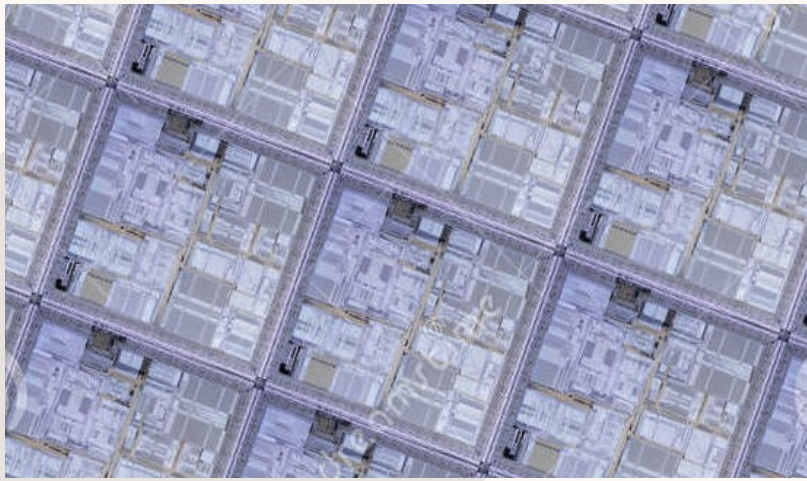


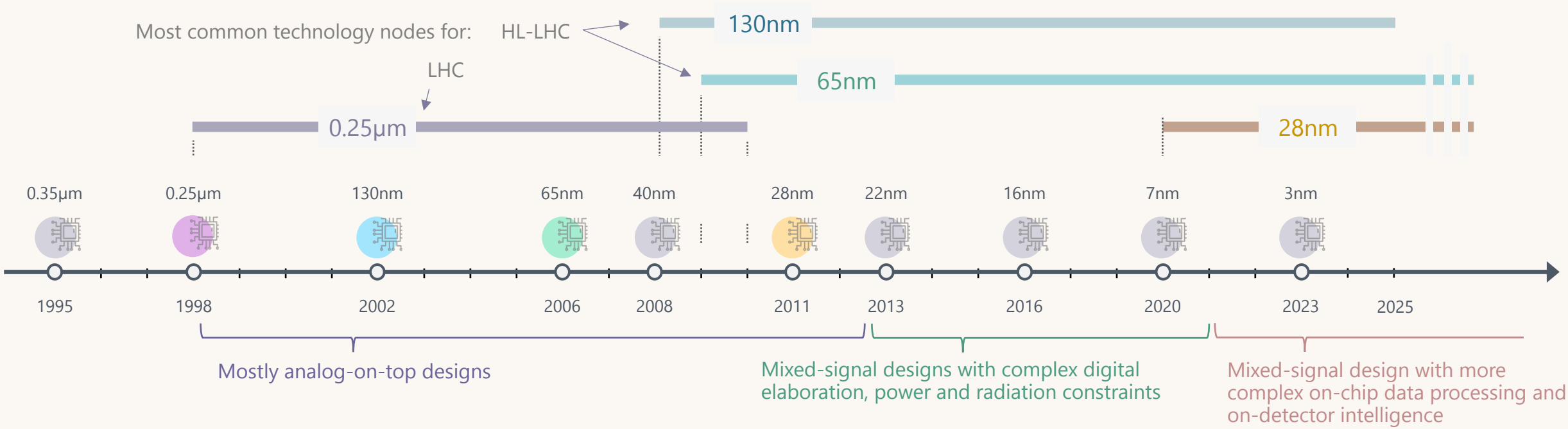


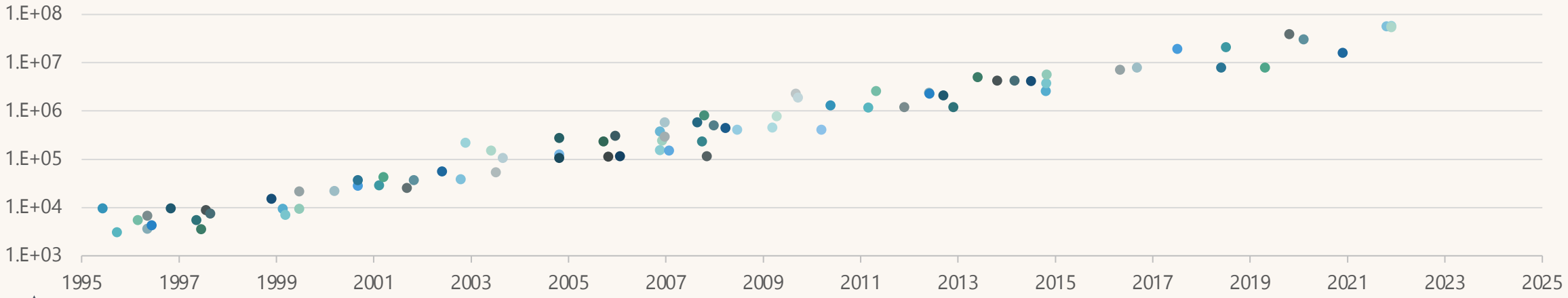
ASIC Support & Foundry Services

Alessandro Caratelli – Kostas Kloukinas – Marco Andorno

alessandro.caratelli@cern.ch – microelectronics users group 2023

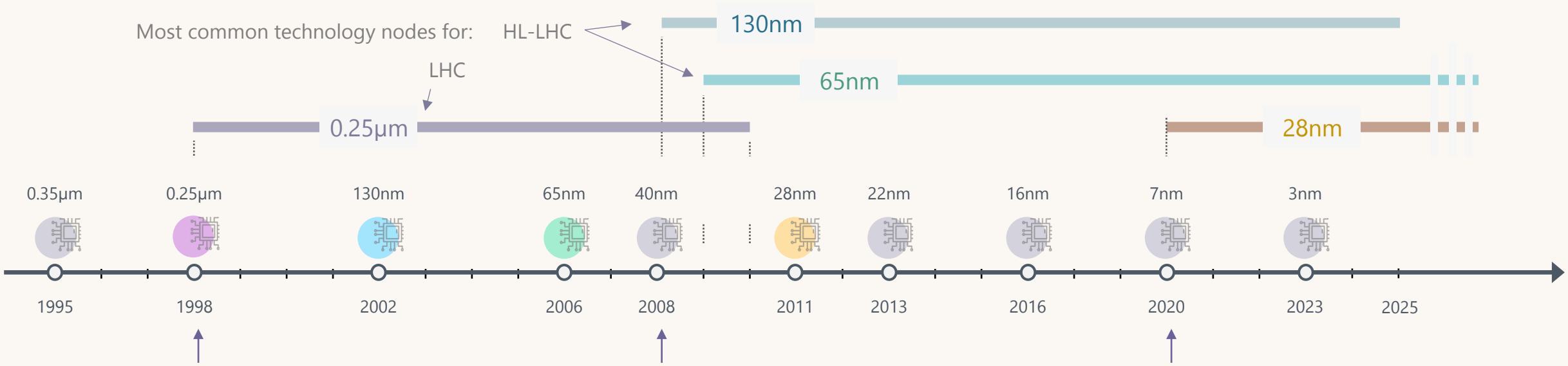
A bit of history of CERN EP-ESE services for the HEP community





Average number of transistors per chip, [source ourworldindata.org]

A bit of history of CERN EP-ESE services for the HEP community



Introduced the CERN Foundry Access Services

Share prototyping costs

Multi-institute designs requires special NDAs that allow for collaborative work

Special terms where negotiated the first time back in the '97 with the IBM 0.25um process
Later, with other foundries, for a set of selected technologies (the most commonly used in HEP)

Engineering & Production runs needs a coordination

Introduced the ASIC Support Service

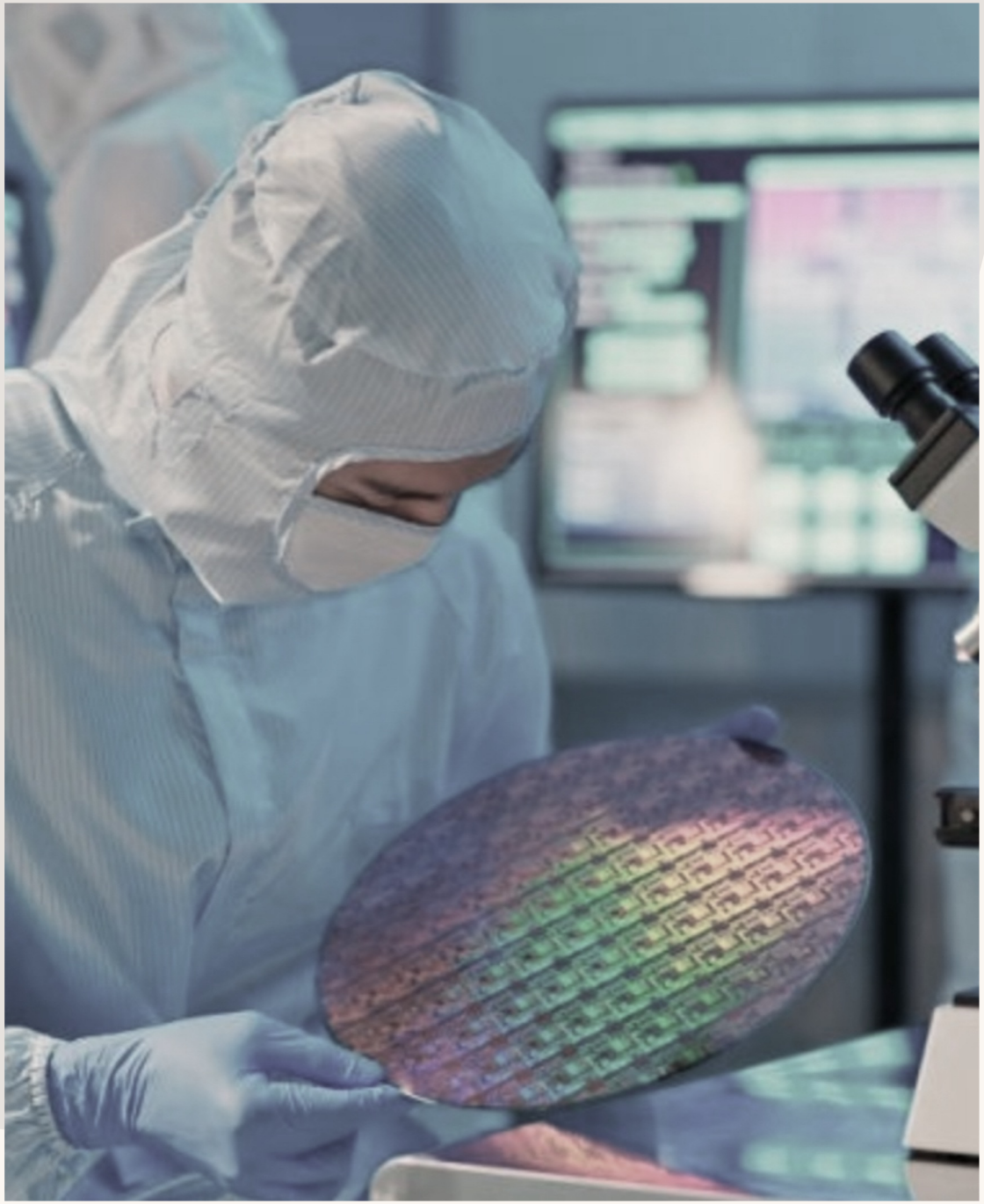
Later, it becomes more important to unify the design process, providing common PDKs and common IP blocks.

The support to the community was then enhanced providing technical support hotline, design flows and strategies, training and more services

But now we need to lock at future detector needs

Introduced the C.H.I.P.S. Design Services

In 2020, to help design in difficulty, the CHIPS service was introduced with the purpose of acting as a firefighting service in case of necessity.



The CERN Foundry Access Services

Establish Commercial Contracts with silicon vendors

Establish NDAs that allow for collaborative work

Organize prototyping Multi Project Wafer runs,
for sharing fabrication costs

Coordinate silicon fabrication:
MPW, Engineering & Production runs

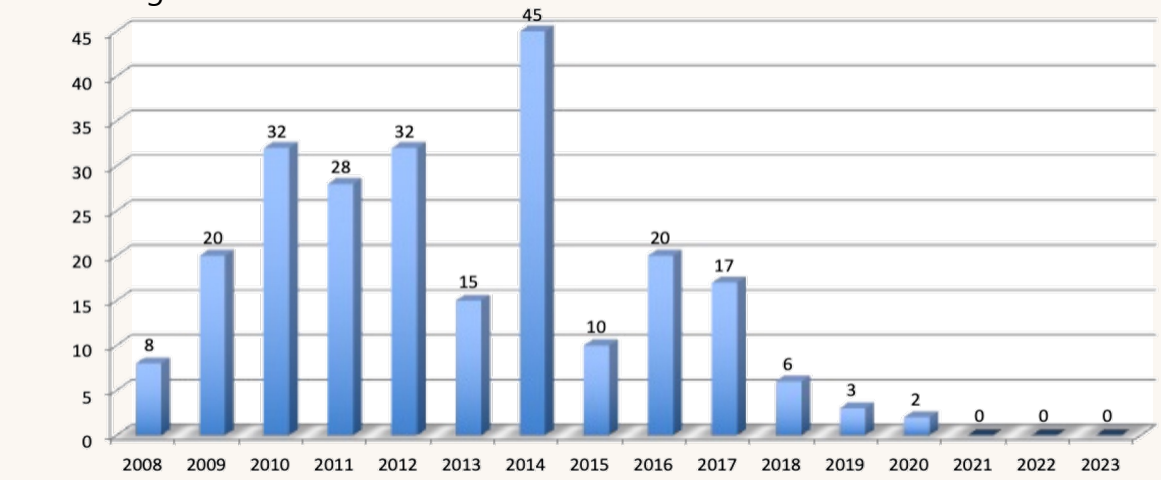
Kostas Kloukinas – Foundry services coordinator

Cinzia Pinzoni – Administrative procedures

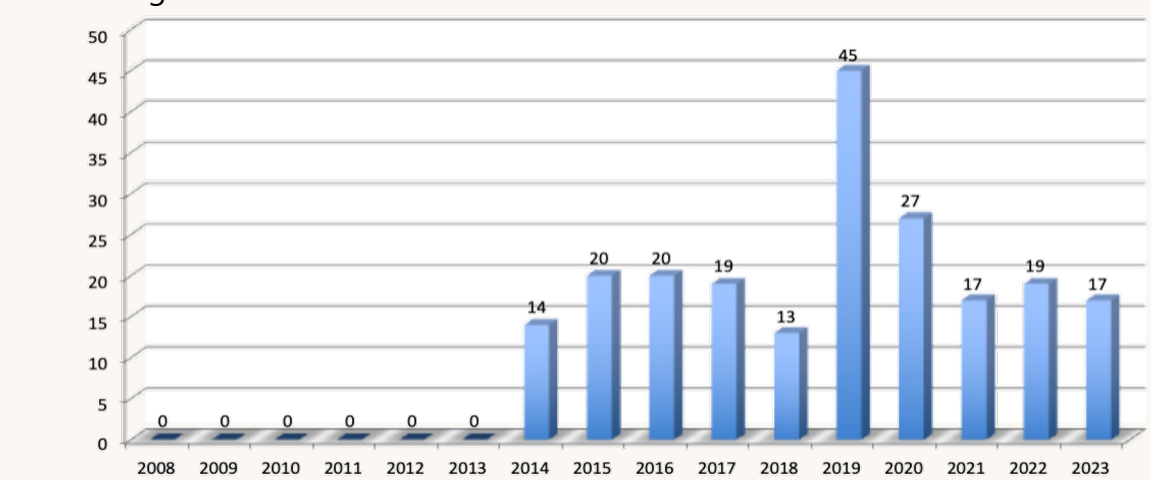
Maxence Ledoux – Logistics

Foundry Services activity 130nm

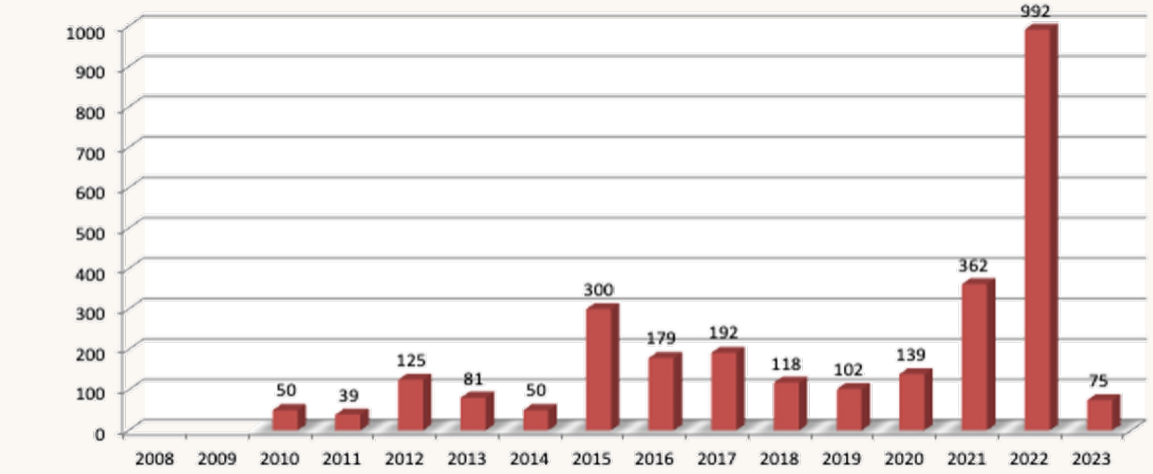
Foundry1 130nm Prototyping activity



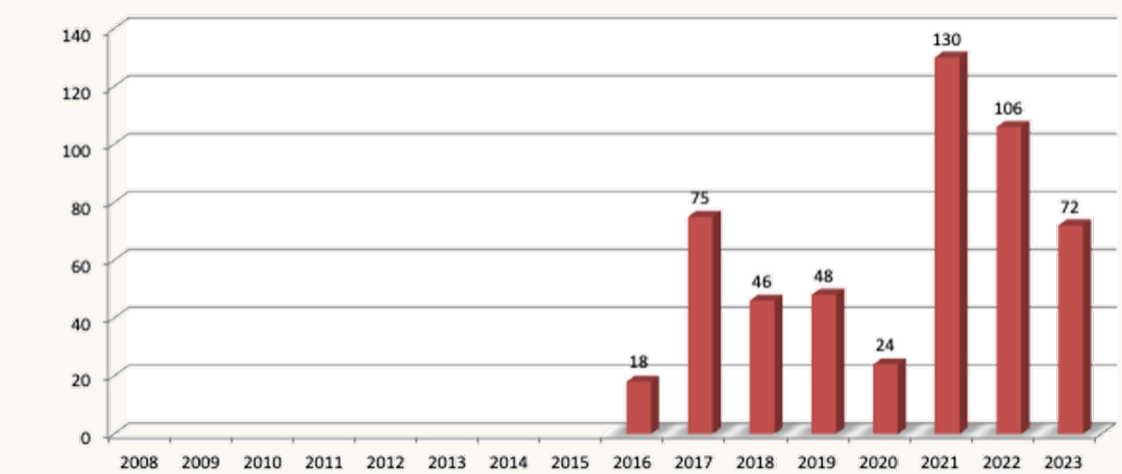
Foundry2 130nm Prototyping activity



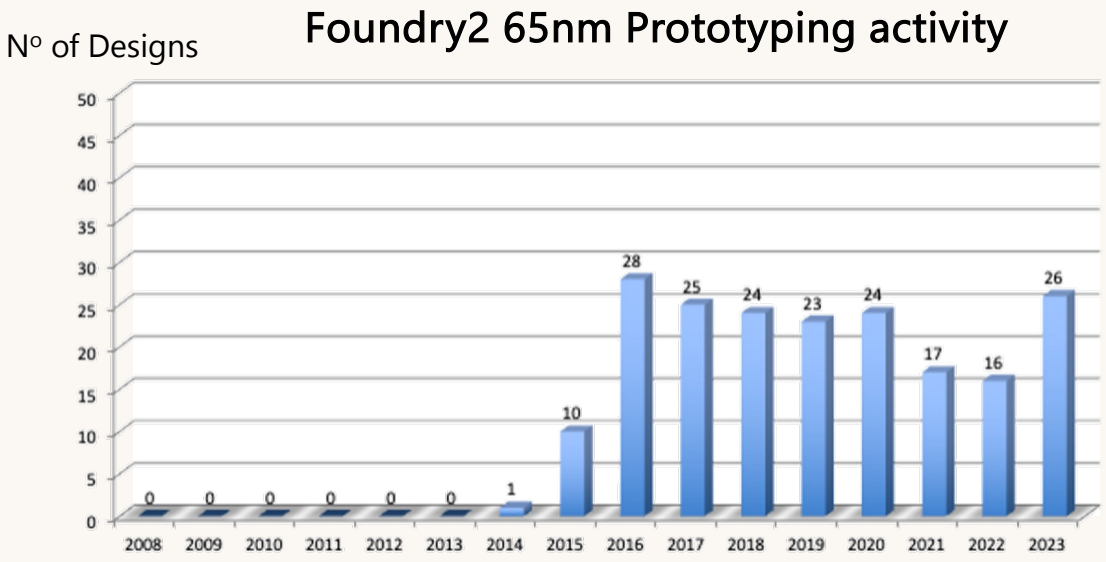
Foundry1 130nm Production Activity

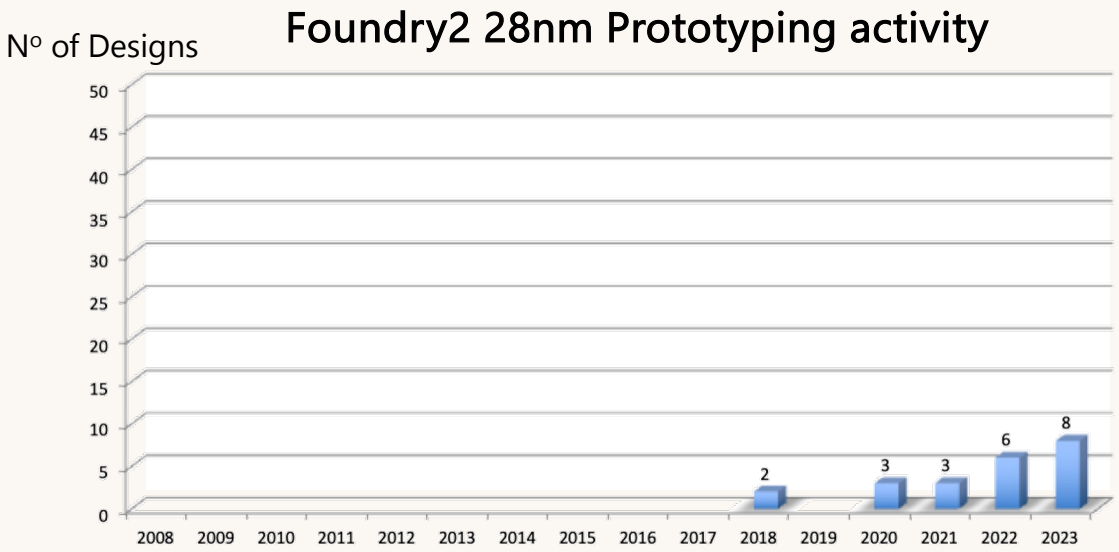


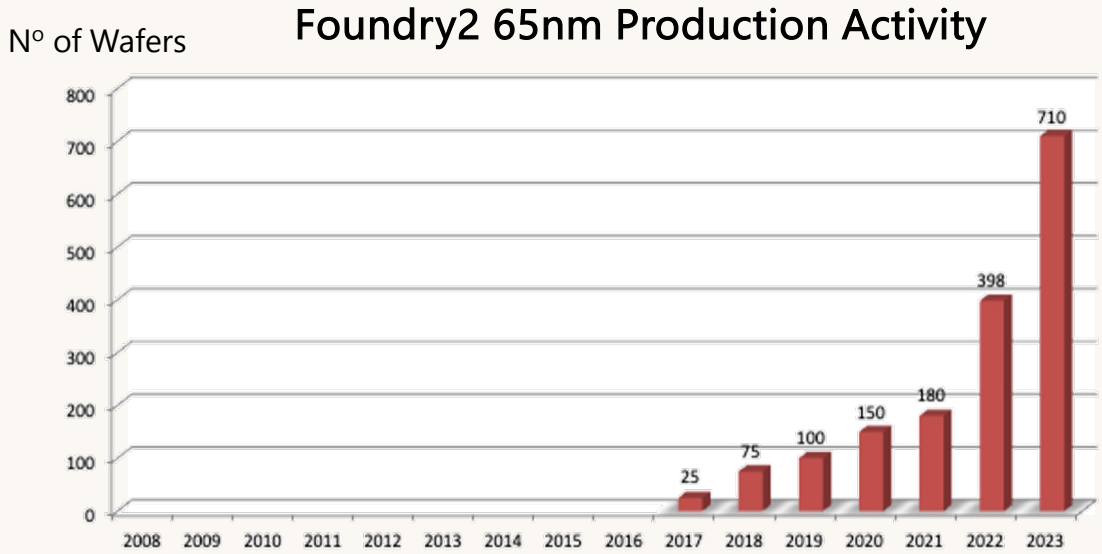
Foundry2 130nm Production Activity



Foundry Services activity 65nm and 28nm

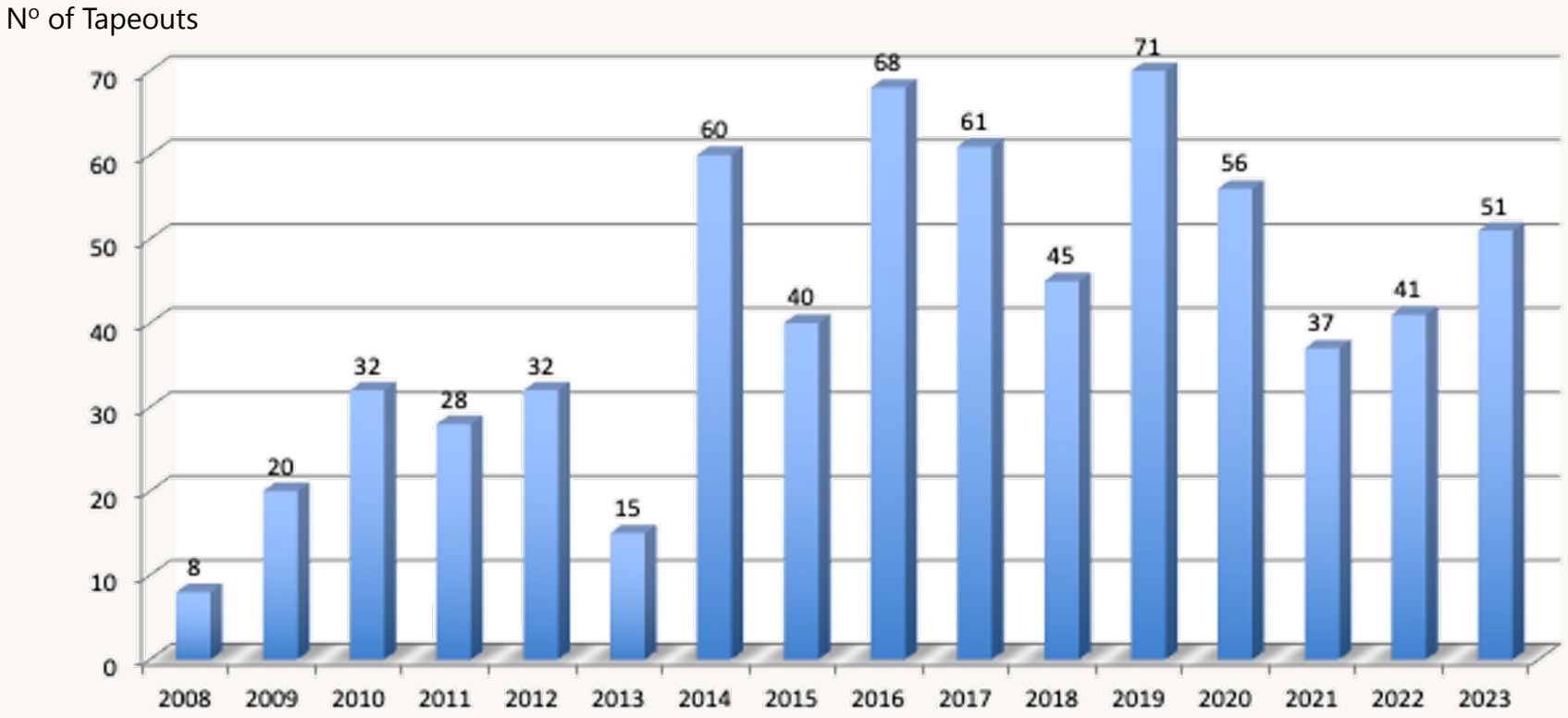






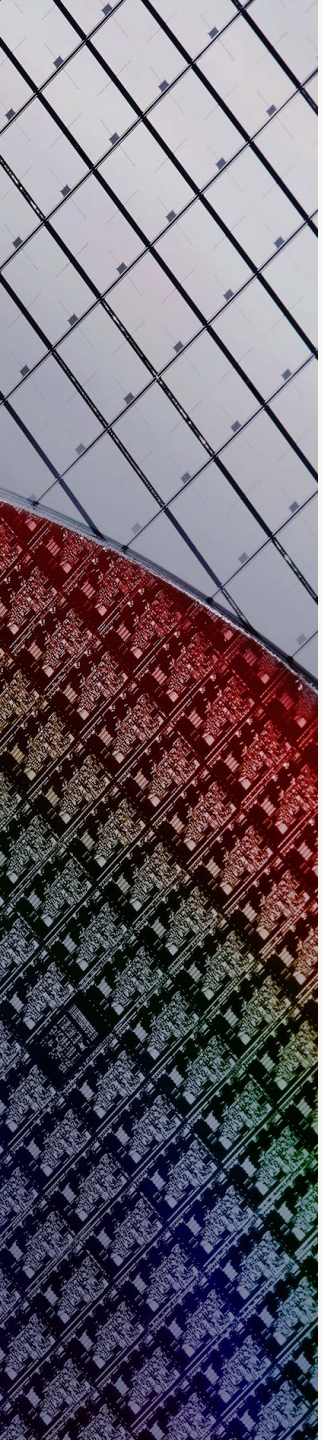
- 65 nm & 130 nm
  - Expected peak of production: 2023-2025
  - Prototyping with new design starts
  - First large-scale full mask-set engineering run: CMS-OT MPA-SSA v1 and RD53A
- 28 nm
  - prototyping activity is ramping up

Foundry Services throughput



Available to HEP community since 1997 (IBM 250nm)

In average 42 designs per year (MPWs, Eng. & Prod. runs) from 2008 till now)



28nm access

The foundry “standard” NDA des not allow the disclosure of technology information to third parties and thus prohibits collaborative work

CERN, IMEC and the Foundry negotiated a HEP **specific 3-way NDA** that **permits the collaborative work among HEP institutes and universities**

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INSTITUTES THAT HAVE SIGNED THE 3-WAY NDA

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CHIPS PROTOTYPES in 2022-23

If interested, Institutes can contact CERN ASIC Support Service
asic.support@cern.ch

Full list available on the CERN ASIC Support Website https://asicsupport.web.cern.ch

28nm 3-way NDA gives you access to

- Exchange of design files among institutes and possibility of collaborate on projects
- Digital design flows and other scripts for EDA tools
- Technology characterization information and design practices
- Tested and supported PDKs with additional limited-access files as the standard cell layout views
- Documentation website and exchange forum
- Training courses for 28nm
- A growing library of analog RadTol IP blocs
- Foundry IP blocks as the memories

If interested, Institutes can contact send a request to the CERN ASIC Support Service at asic.support@cern.ch

then Every engineer at each institute that wishes to have access on the technology has to sign an “Individual NDA”.

The CERN ASICs Support Services

Develop and distribute the Common Design Platforms for mixed-signal ASICs design

- Enhance, update and maintain the PDKs for commonly used technologies in HEP environment
- Distribution and maintenance of common macro blocks
- Preparation and maintenance of design flows of general use
- Support for System-on-Chip design enablers

Provide support to HEP IC designers community

- Support requests related to microelectronics technologies and to EDA tool usage
- Promote the collaborative works and knowledge sharing
- Organize training workshops about design for HEP environment

Kostas Kloukinas – ASIC Support coordinator
Alessandro Caratelli – Support engineer
Marco Andorno – Support engineer

For info: https://asicsupport.web.cern.ch

The common design platforms

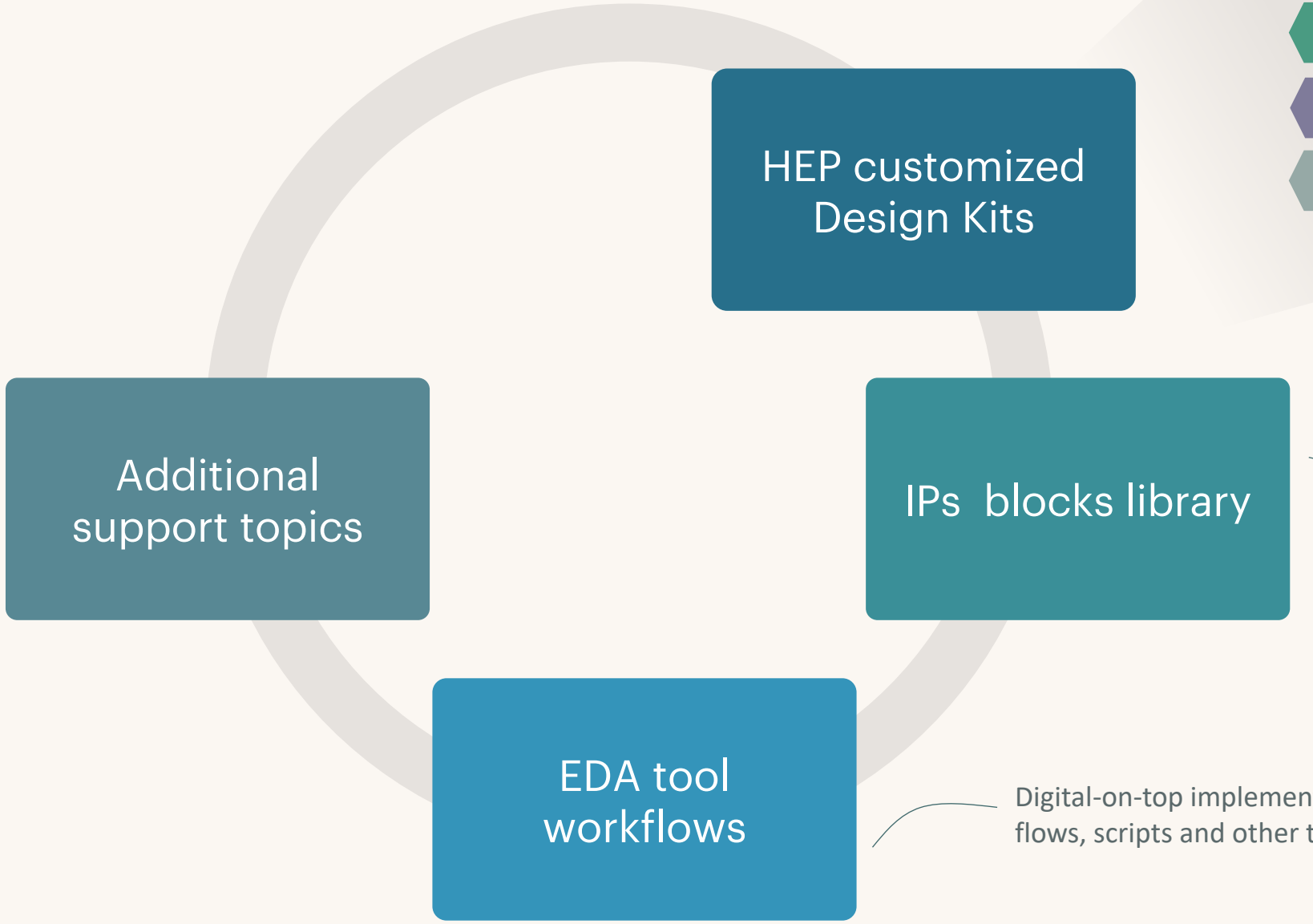
F1 130nm

F2 130nm

F2 65nm

F2 28nm

Advanced tech



Library of tested radiation tolerant IP blocks for multiple selected technologies

Digital-on-top implementation flows, scripts and other tools

The Common Design Platform provide a stable and reliable solutions.

It allow the design of common projects and will be always updated and maintained.

To tackle the challenges of the design for future experiments, it is important that the community move forward in adopting industry practices and early adopt latest technologies

We are open and we would like to engage in collaboration

Please contact asic.support@cern.ch

The common design platforms

F1 130nm

F2 130nm

F2 65nm

F2 28nm

Advanced tech

From EP-R&D program to the community

SoC design enablers

HEP customized Design Kits

IPs blocks library

Library of tested radiation tolerant IP blocks for multiple selected technologies

EDA tool workflows

Digital-on-top implementation flows, scripts and other tools

Additional support topics

The common design platforms

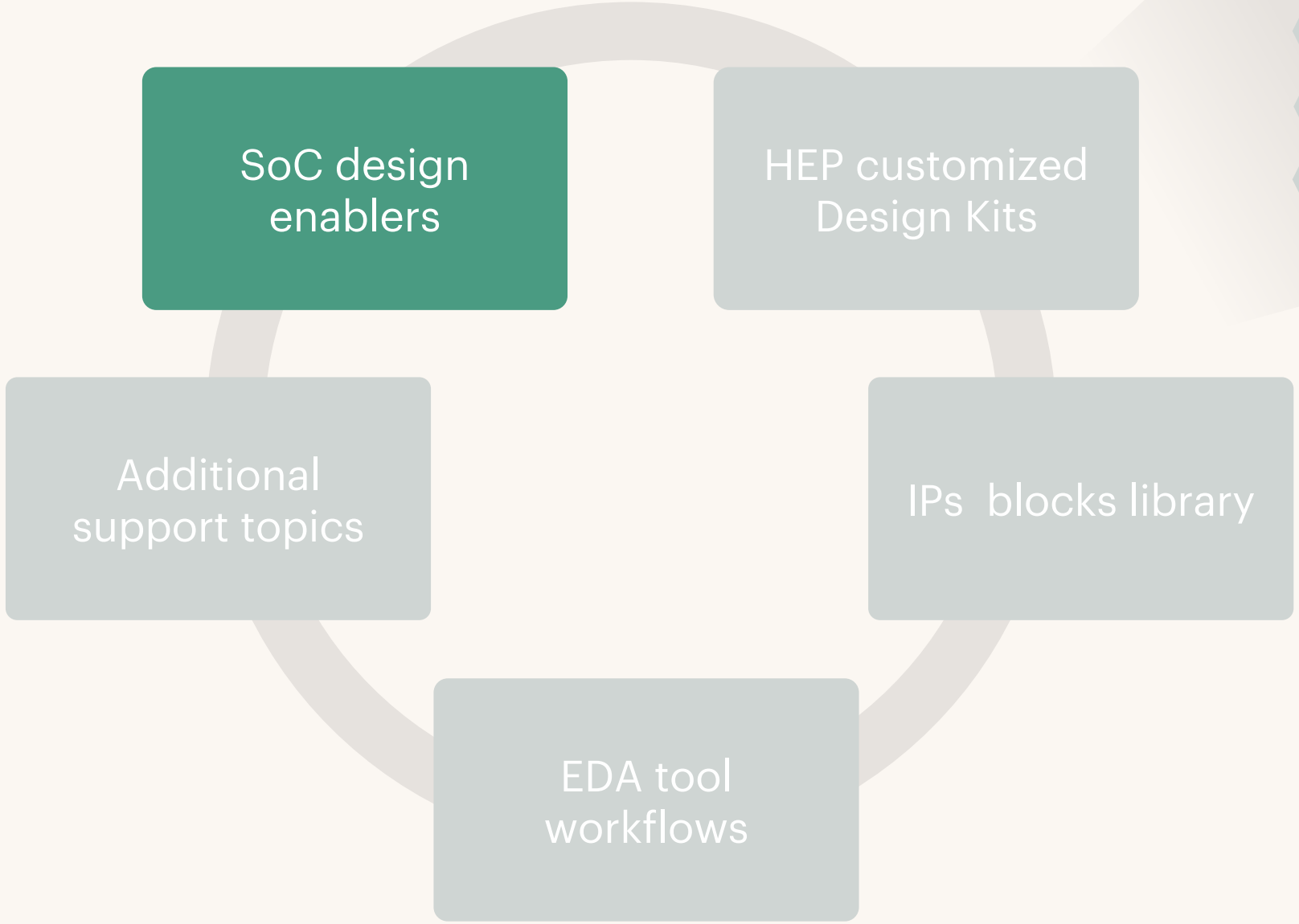
F1 130nm

F2 130nm

F2 65nm

F2 28nm

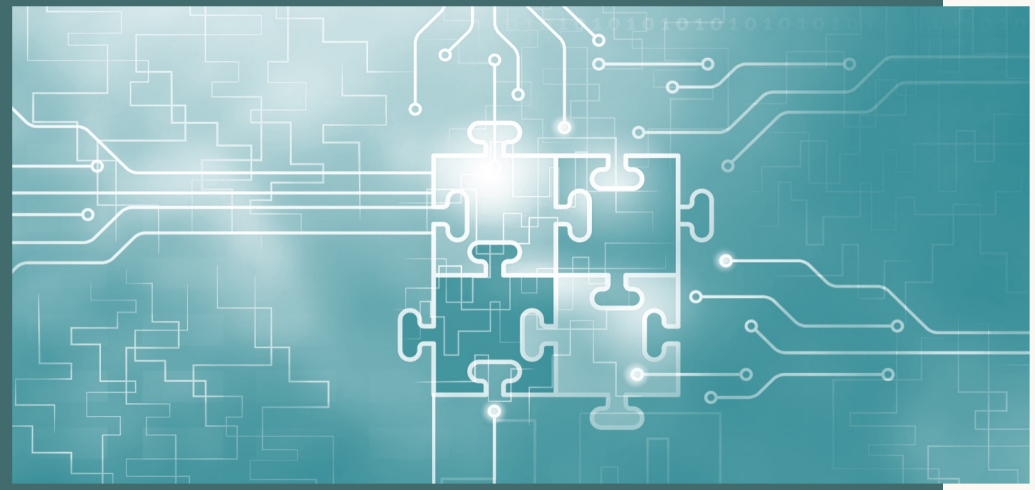
Advanced tech



System-on-Chip design approach motivation

Future detector upgrades will require more complex ASICs

They require advanced technology nodes, that come with high development costs in terms of design time, verification and costs



An abstract design methodology, focused on programmability and reusability will provide:

- Develop reusable IP blocks
- Standardized interconnects for IP blocks
- Replace state machines with a control processor (RISC-V based)
- Programmable, flexible logic blocks (SoC Ecosystem, cores, eFPGA, NoCs)
- Enhance Hierarchical Digital Implementation and Verifications

System-on-Chip design approach

Introduce Programmability in the detectors

- Allows retargeting an ASIC for different applications
- Change the algorithms during runtime

Simplify system integration and reduce design time

- Introduce modularity with self-contained blocks
- Accelerate digital design and speedup verification
- Accelerate physical implementation

Provide a RadTol Digital IP blocks library

- Provide pre-verified building blocks
- All IPs are coherent with a standardize interconnect
- Helps design reusability within the community

A System-on-Chip platform provides the necessary shift from design for application to design for resources.

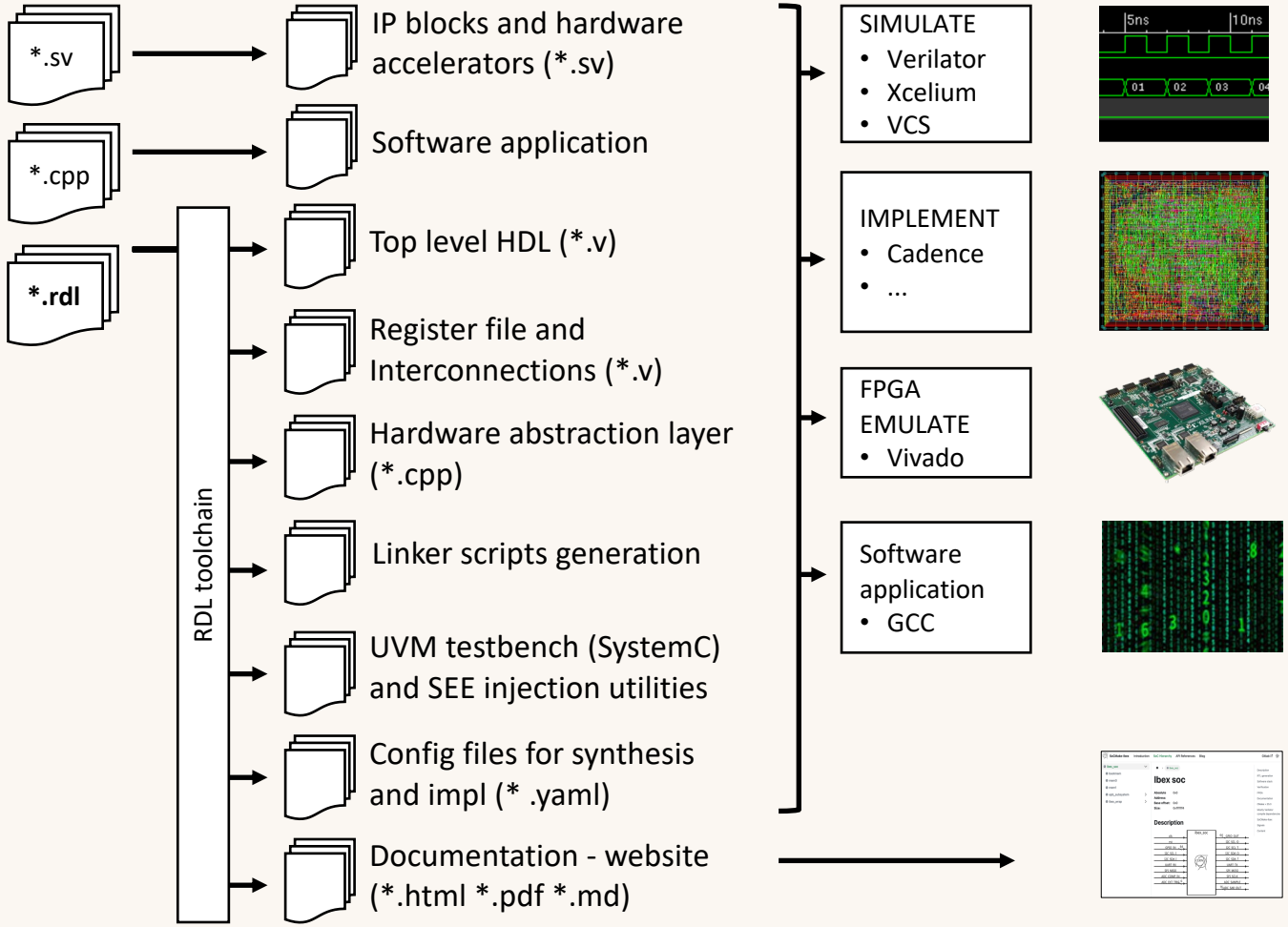
Hardware generation Software generation

SoCMake

DOC: https://socmake.docs.cern.ch

GIT: https://gitlab.cern.ch/socmake

- Open-source SoC generator tool
- From a single SystemRDL description file, automatize the generation of:
  - Hardware design
  - Software toolchain
  - Verification platform
  - Documentation
- Generate custom SoCs
- Rapid SoC prototyping
  - Quickly build different architectures with different IP blocks, hardware accelerators and different CPUs
- Work in progress
- Design team: R. Pejasinovic, M. Andorno, A. Caratelli, A. Nookala, K. Kloukinas



A System-on-Chip generation ecosystem

work in progress

GOAL: Provide the possibility of quick generating **highly-customizable systems that can be integrated in your custom ASICs** (hardware, verification and software toolchain support)

Build system

- ✓ Execute SoC generator tools in an integrated environment
- ✓ Cross-compile application software
- ✓ IPs management
- ✓ Dependencies management
- ✓ Documentation and website generation

Hardware generation system

- ✓ Generate the top-level SoC
- ✓ Integrate IP blocks
- • *Integrate hardware accelerators*
- ✓ Infer interconnects (crossbars, adapters)

Software generation system

- ✓ Generate Hardware abstraction layer
- • *Generate low-level drivers*
- ✓ Generate linker scripts

Verification environment

- ✓ *Assemble simple verification environment*
- • *Generate complete SystemC-UVM environment*
- • *FPGA prototyping*
- ✓ SEE injection framework
- • *Metrics analyzer*

LEGEND: ✓ Development in advanced stage
• *Development in early stage*

SoC platform components

CPU Core

Memory Subsystem

Digital and analog IPs

Hardware accelerators

Interconnect bus

For the moment 4 popular cores supported:

- LowRISC Ibex
- ChipsAlliance (WD) EL2
- Syntacore SCR1
- Picorv32

Support for multiple interconnect busses

- APB4 → APB-RT
- AXI4-Full → AXI-RT
- Axi4-Lite → AXI-Lite-RT
- NMI, OBI

Radiation tolerant version:
Triplicated control signals
Encoded data and address lines

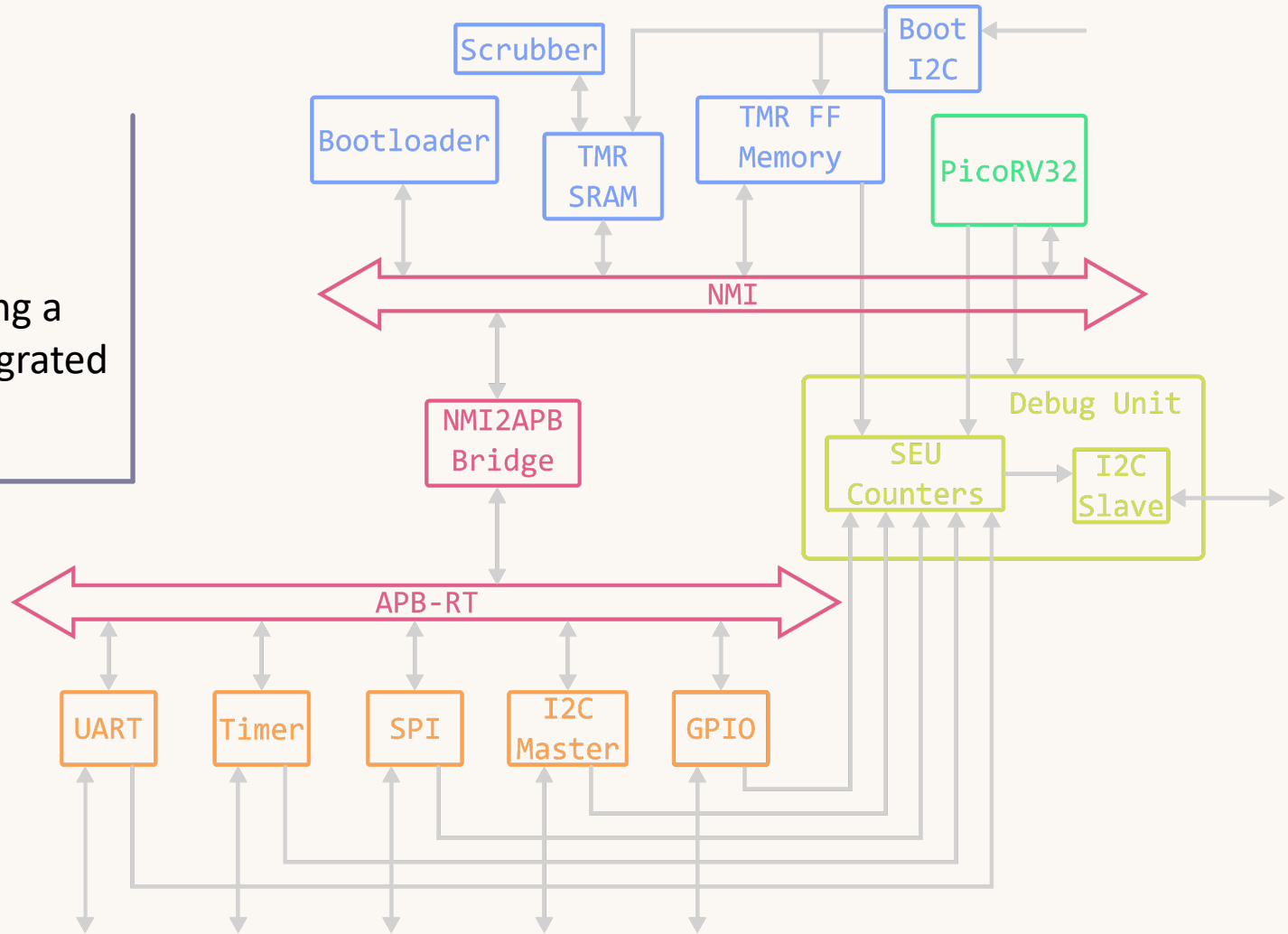
Example of SoC design build with this SoC generator platform

Many different architectures can be generated

Expect to tapeout a demonstrator chip in 28nm.

The GOAL:

- isn’t to provide a static design
- is to provide the possibility of quick generating a highly-customizable systems that can be integrated in your custom chip (as a pixel readout ASIC)



DOC: https://socmake.docs.cern.ch

GIT: https://gitlab.cern.ch/socmake

The common design platforms

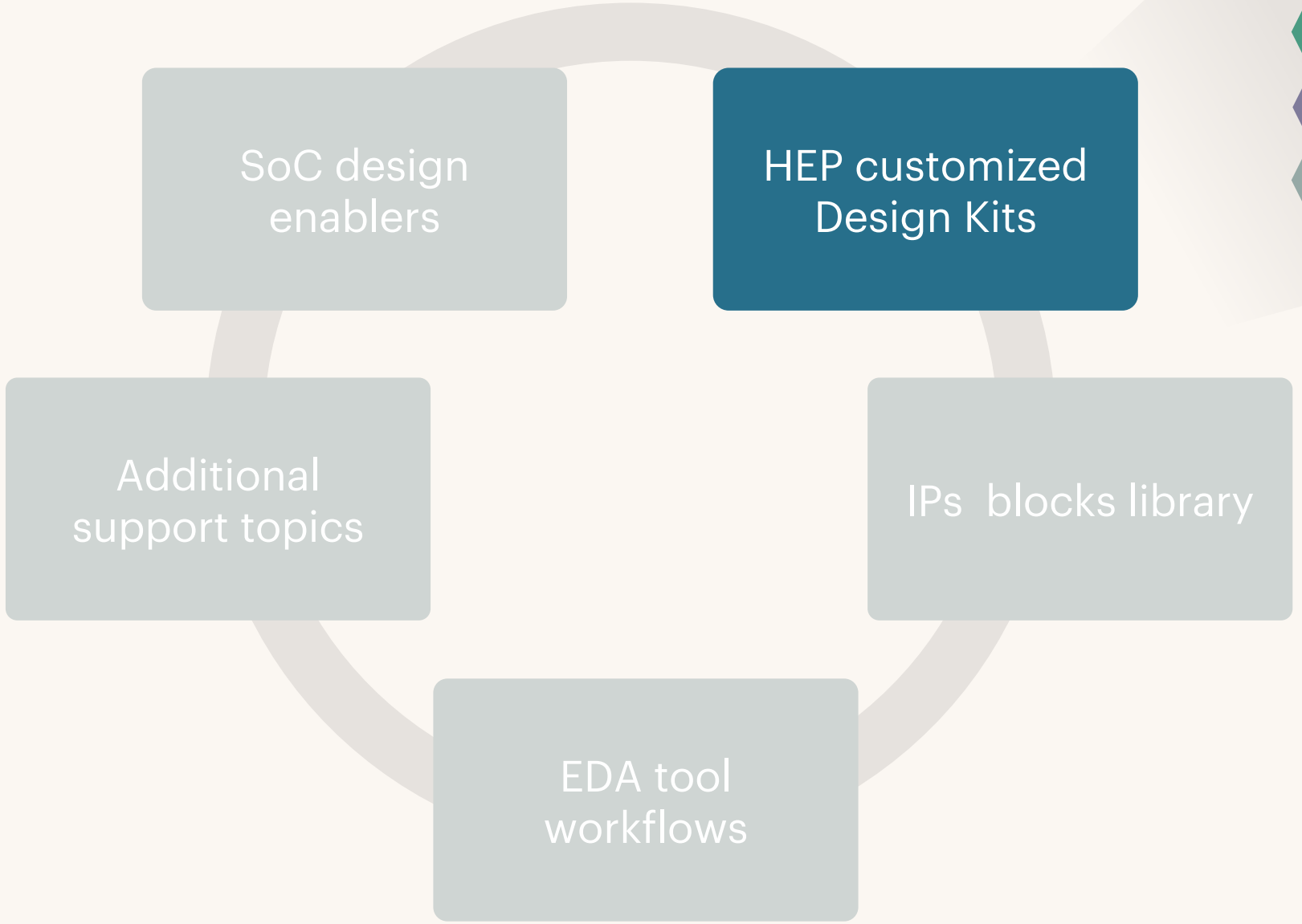
F1 130nm

F2 130nm

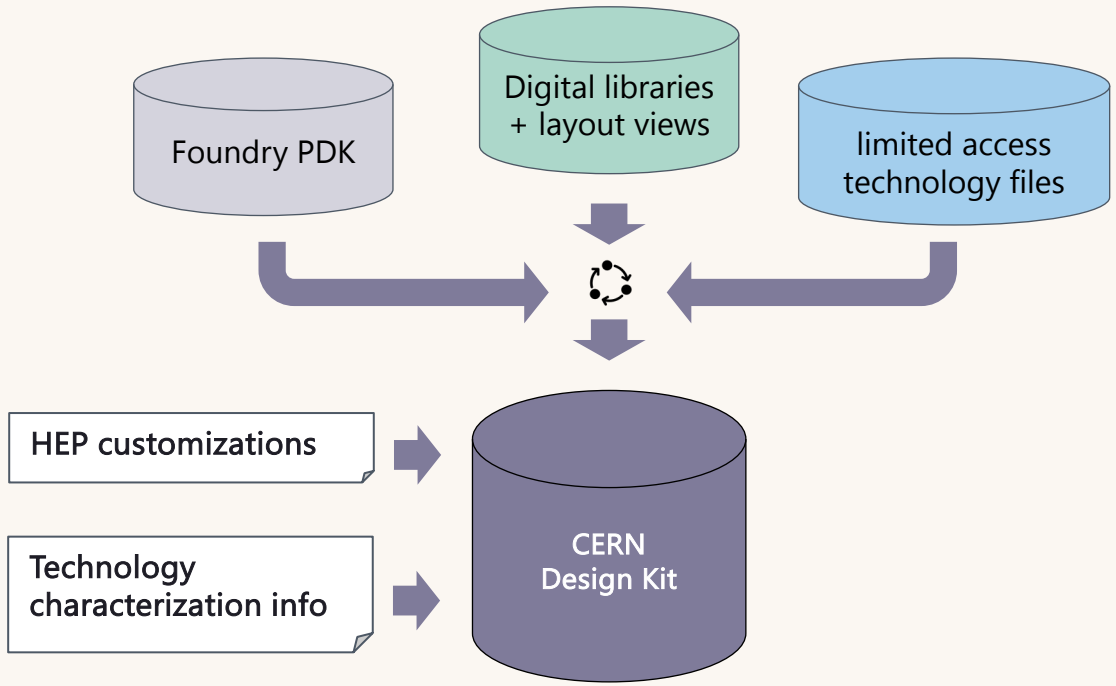
F2 65nm

F2 28nm

Advanced tech



HEP customized Design Kits



All Design Kits are restructured in the same way across all technology nodes (130nm, 65nm, 28nm)

- CERN ASIC Support refurbish, maintain and update the PDKs
- The CERN Design Kits are optimised to provide
  - a tested and reliable solution
  - Interoperability within the community avoiding incompatibilities across teams
- Optimize the efforts of integrating a design environment
- The design kits is updated following:
  - all the major foundry releases
  - HEP specific and radiation tolerance needs
  - requirements and findings from designers
- Every year the design kits are tested and adapted to support the latest EDA tools Europractice release

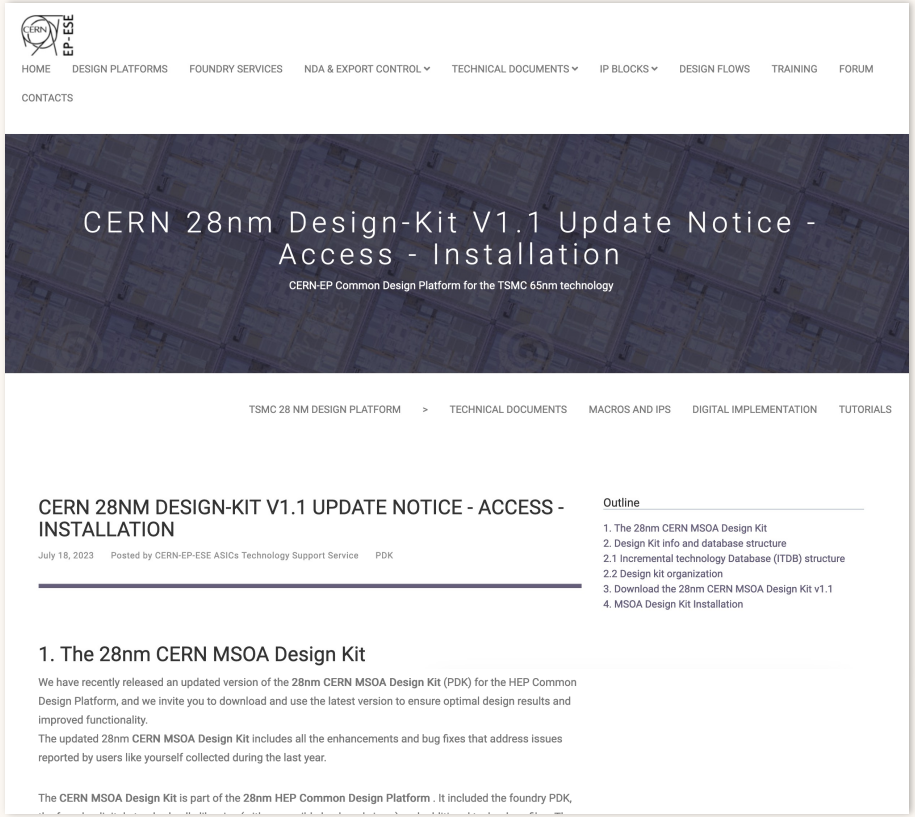
28nm design kit updates

Latest release: **v1.1.0** (18 July 2023)

UPDATE NOTICE AND DOWNLOAD DETAILS
https://asic-support-28.web.cern.ch/tech-docs/pdk_update_1.1

Request access

Download PDK



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The common design platforms

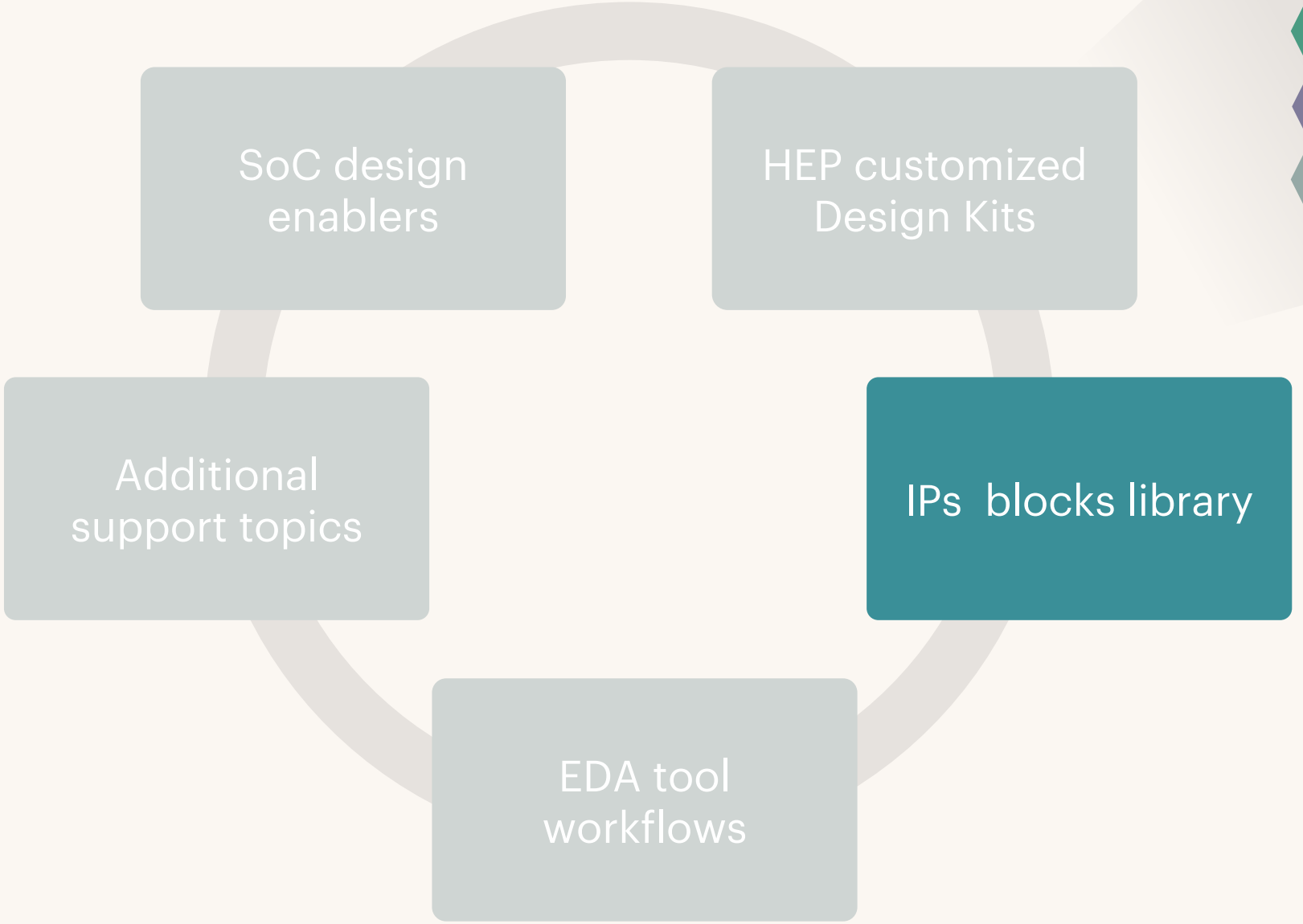
F1 130nm

F2 130nm

F2 65nm

F2 28nm

Advanced tech



IP blocks library

The CERN ASIC Support is taking care of:

- Packaging in an uniform way the IP blocks
- Maintenance of the shared repositories (Cliosoft) and institutes access and provide access upon request

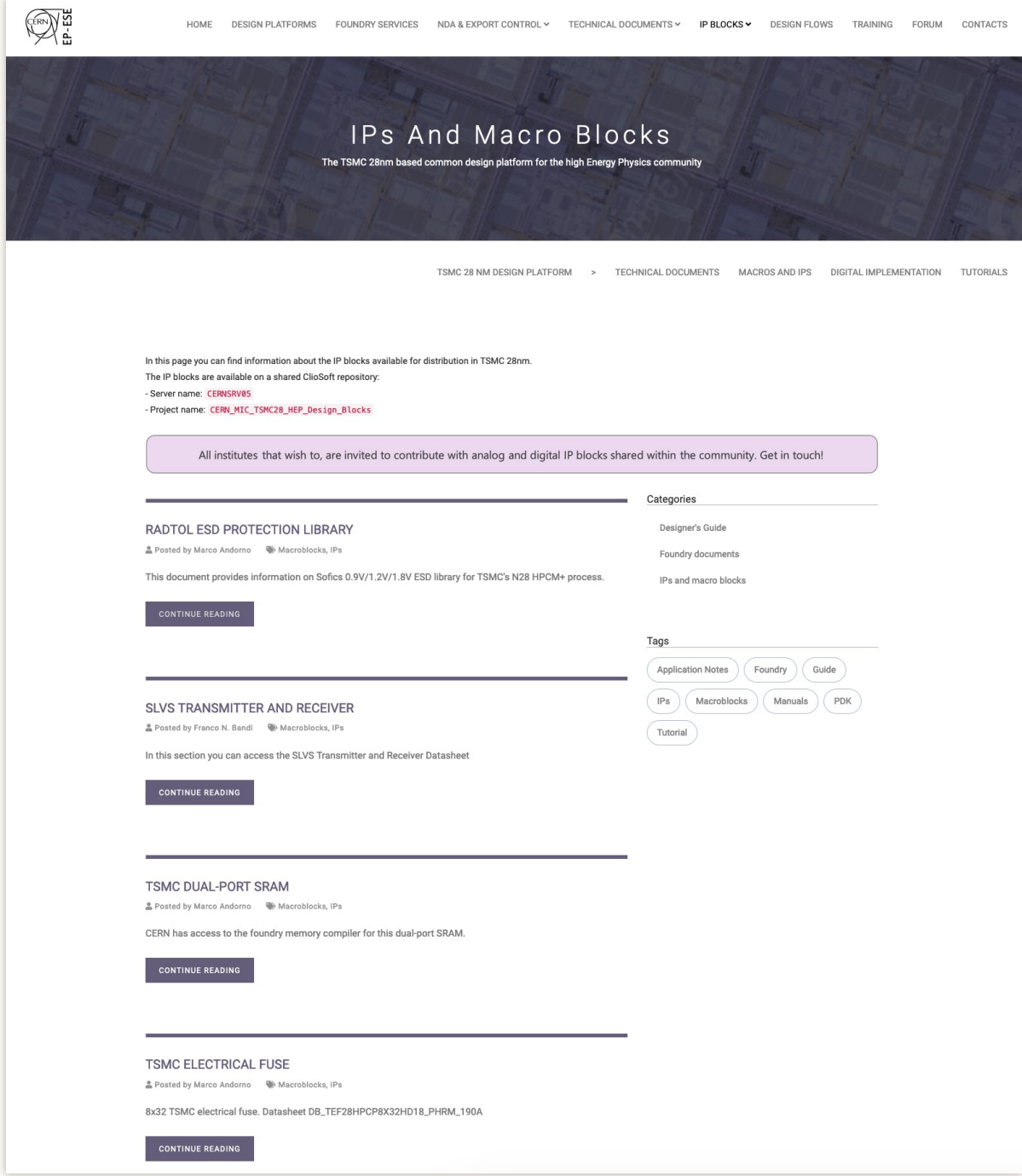
The ownership of the IP block remains with the designer. The platform allow to advertise and share the IP blocks with the community.

List of available IP blocks and datasheets:

F2 28: https://asic-support-28.web.cern.ch/ip-blocks/
F2 65: https://asic-support-65.web.cern.ch/docs2/
F2 130: https://asic-support-130.web.cern.ch/docs2/
F1 130: https://espace.cern.ch/asics-support/gf130/

And in backup slides

All institutes that wish to contribute are invited to participate to common repositories with analog and digital IP blocks, shared within the community! Get in touch!

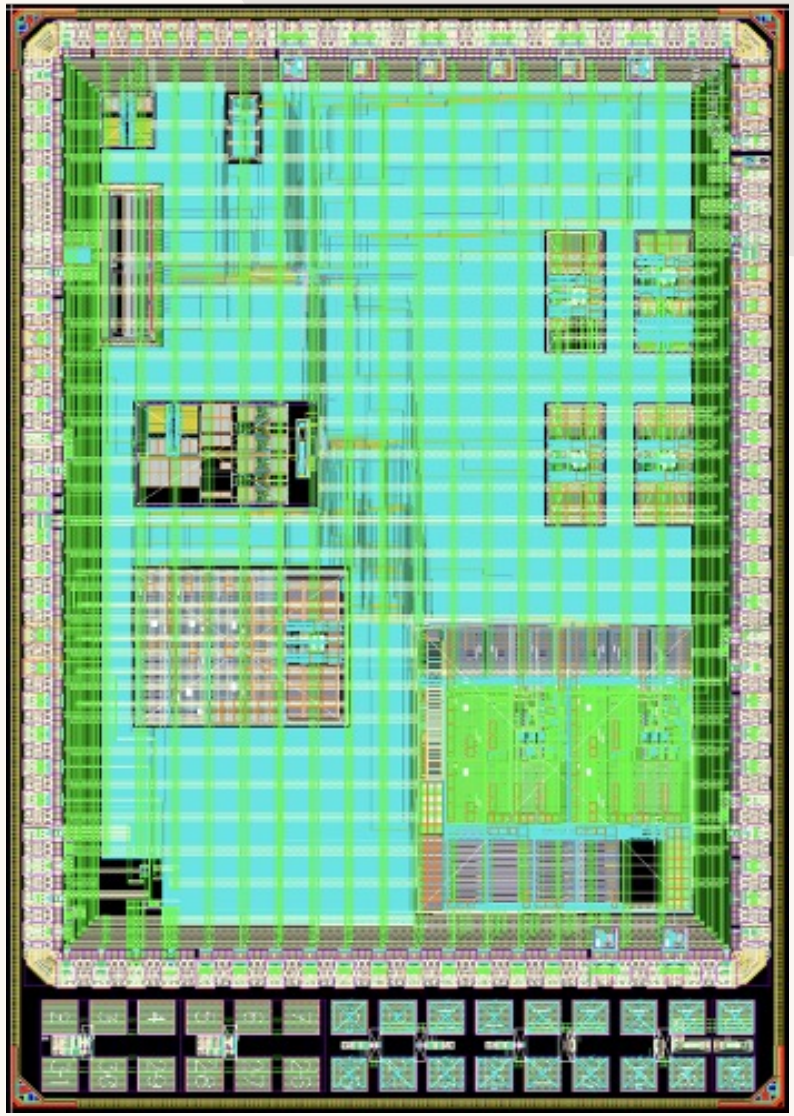


AMTest28 chip for silicon-test of common IPs

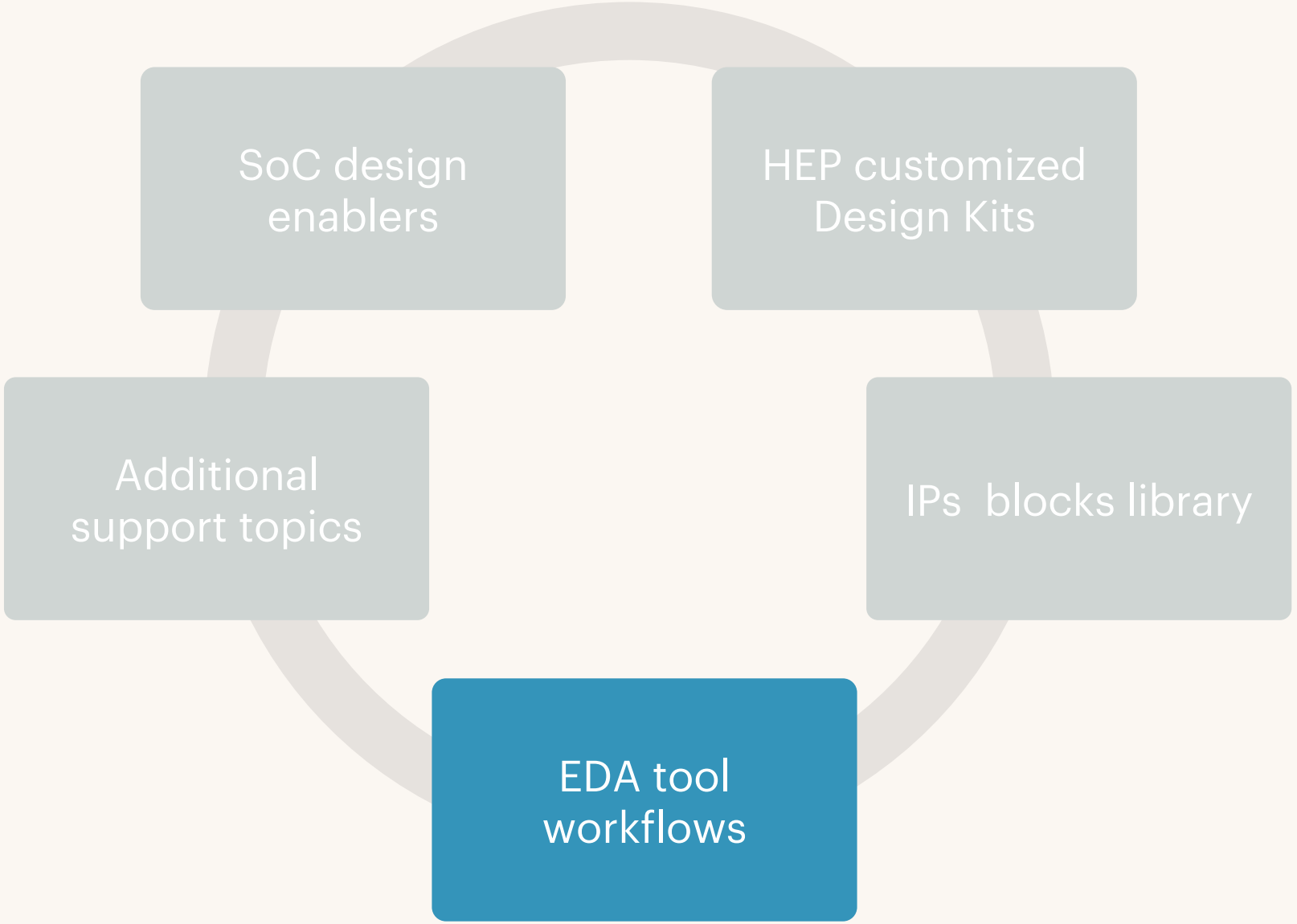
GOAL: Silicon-prove the IP blocks designed in 28nm, by functional and radiation testing

- Marco Andorno (ASIC Support) prepared a test chip that integrates several IP-blocks from CERN or form other institutes providing a single MPW run to test multiple blocks, and uniform testing requirements
- The analog and mixed-signal blocks were assembled Digital-on-Top, along with a control and configuration interface (triplicated):

IP-Block	Designer
SLVS Transmitter and Receiver	Franco Bandi (CERN)
Digital PLL	Vladimir Gromov (Nikhef)
Rail-to-rail analog buffer	Jan Kaplon (CERN)
Analog frontend	Markus Piller (TU Gratz)
Bandgap reference (4 different versions)	Grzegorz Wegrzyn, Stefano Michelis (CERN)
TIMO28 (TID response variation IP block)	Giulio Borghello (CERN)
8-bit DAC	Markus Piller (TU Gratz), Viros Sriskaran
12-bit Sigma-Delta DAC	Can Akgun (Nikhef)
Test structures (4 types)	SOFICS



The common design platforms



Digital implementation flows RTL to GDS

for 65nm and 28nm

Latest release **TAG v2.0.1** (September 2023)

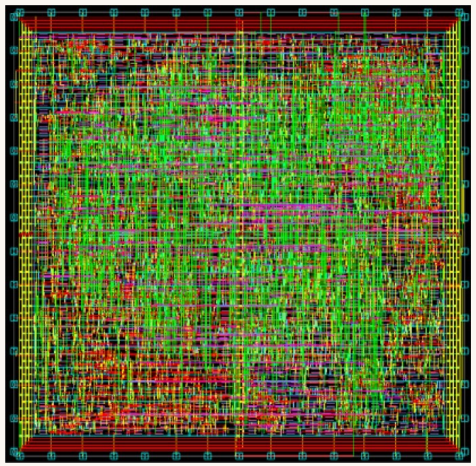
DOC: https://asicsupport.web.cern.ch/flows

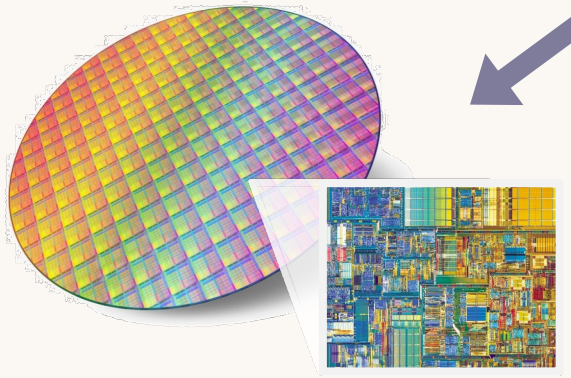
GIT: https://gitlab.cern.ch/asic-design-support/digital-design-flows

- For fast prototyping, user of the flow only need to work on the level of *.yaml configuration files (complexity is hidden behind)
- Self-contained flow steps
- Included more advanced design steps
- Support for TMR design
- Support for advanced OCVs
- Signoff STA and power analysis
- Multi power domains
- Included all Foundry recommendations
- Support for mixed-signal OA database export and sharing
- Advanced metrics reports

```
module counter #(
    parameter DATA_WIDTH   = 16,
    parameter COUNT_FROM   = 0,
    parameter COUNT_TO     = 2^(DATA_WIDTH-1),
    parameter STEP         = 1
    )(
    input  logic clk_i, en, rst,
    input  logic [DATA_WIDTH-1:0] factor,
    output logic [DATA_WIDTH*2-1:0] out
    );

    logic [DATA_WIDTH-1:0] out_m;

   // Synchronous logic
    always_ff @(posedge clk_i) begin
       if (rst && (out_m < COUNT_TO)) begin
          if (en)
             out_m <= out_m + STEP;
       end
       else
          out_m <= COUNT_FROM;
    end

    // just to generate some more logic to implement
    always_ff @(posedge clk_i) begin
        out <= out_m * factor;
    end

endmodule
```

```
wire w3;
nand g12841__6260 (n_245, w3, n_151);
or g3 (w3, n_235, n_3, wb_adr_od[7]);
wire w4;
or g12843__4319 (n_244, w4, n_241);
and g4 (w4, n_26, n_176);
wire w5, w6, w7;
nand g12844__8428 (n_243, w5, w6, w7);
or g7 (w7, n_239, n_3);
or g6 (w6, n_4, n_151);
or g5 (w5, wb_adr_od[5], n_235);
wire w8;
nand g12845__5526 (n_242, w8, n_151);
or g8 (w8, n_235, wb_adr_od[6]);
wire w9, w10;
nand g12847__6783 (n_240, w9, w10);
nand g10 (w10, wb_adr_od[3], n_237);
nand g9 (w9, wb_adr_od[4], n_236);
wire w11;
nand g12848__3680 (n_241, w11, n_239);
or g11 (w11, n_177, wb_adr_od[5]);
wire w12, w13, w14;
nand g12850__1617 (n_238, w12, w13, w14);
or g14 (w14, n_233, n_23);
or g13 (w13, n_22, n_151);
or g12 (w12, wb_adr_od[3], n_227);
wire w15;
nor g12851__2802 (n_239, w15, n_236);
and g15 (w15, n_4, n_176);
```





Digital implementation flows

for 65nm and 28nm

Latest release **TAG v2.0.1** (September 2023)

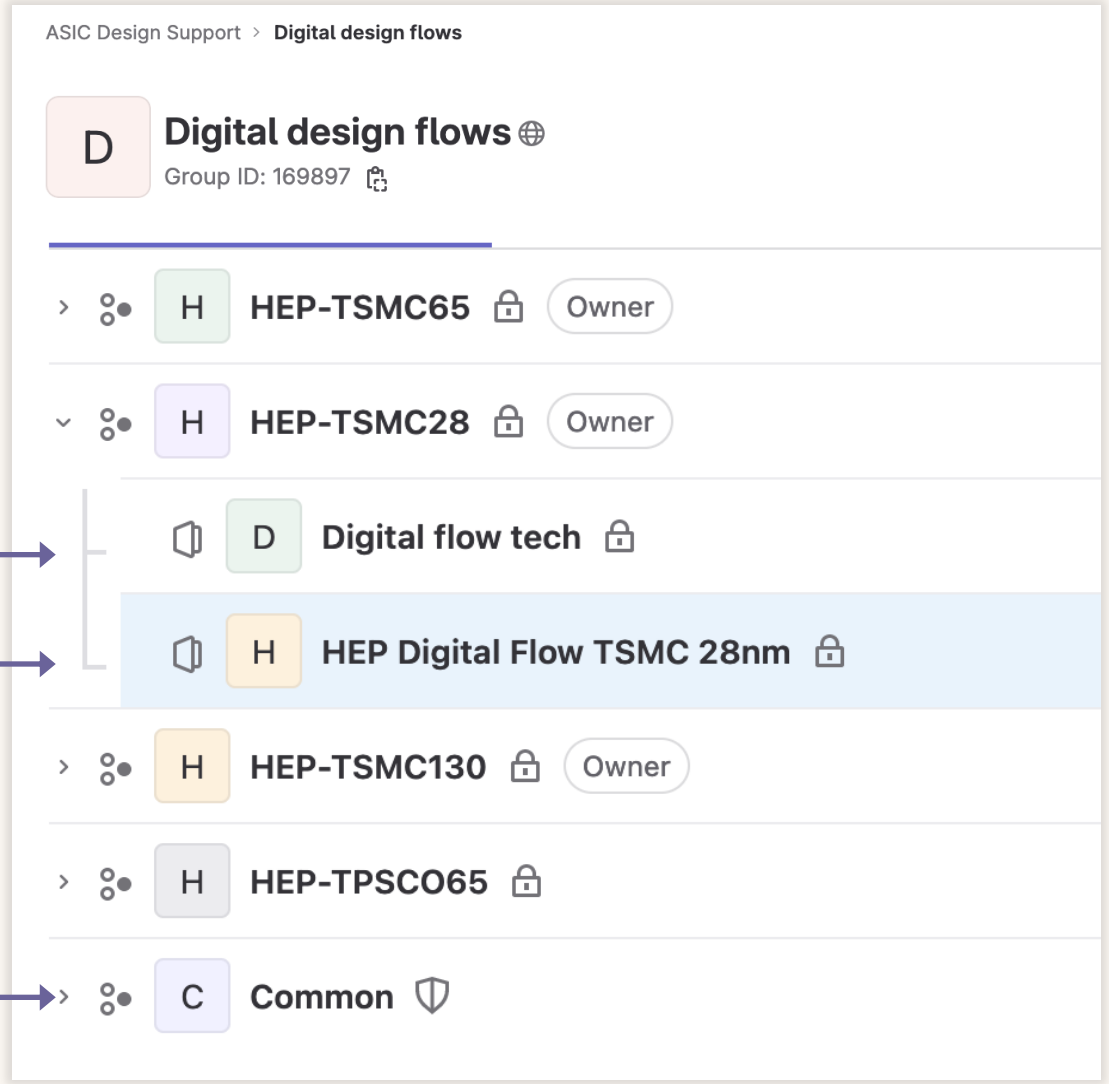
DOC: https://asicsupport.web.cern.ch/flows

GIT: https://gitlab.cern.ch/asic-design-support/digital-design-flows

Technology specific flow customization
(submodule) NDA protected

Top repository for digital design flow (TOP)
with the design specific customization files

Common library of scripts and procedures
(submodule)
● synthesis ● implementation,
● signoff STA ● power analysis
● physical verification



We would be very happy to see more participation from universities in maintaining and improving design flows and add support for other technologies!

The common design platforms

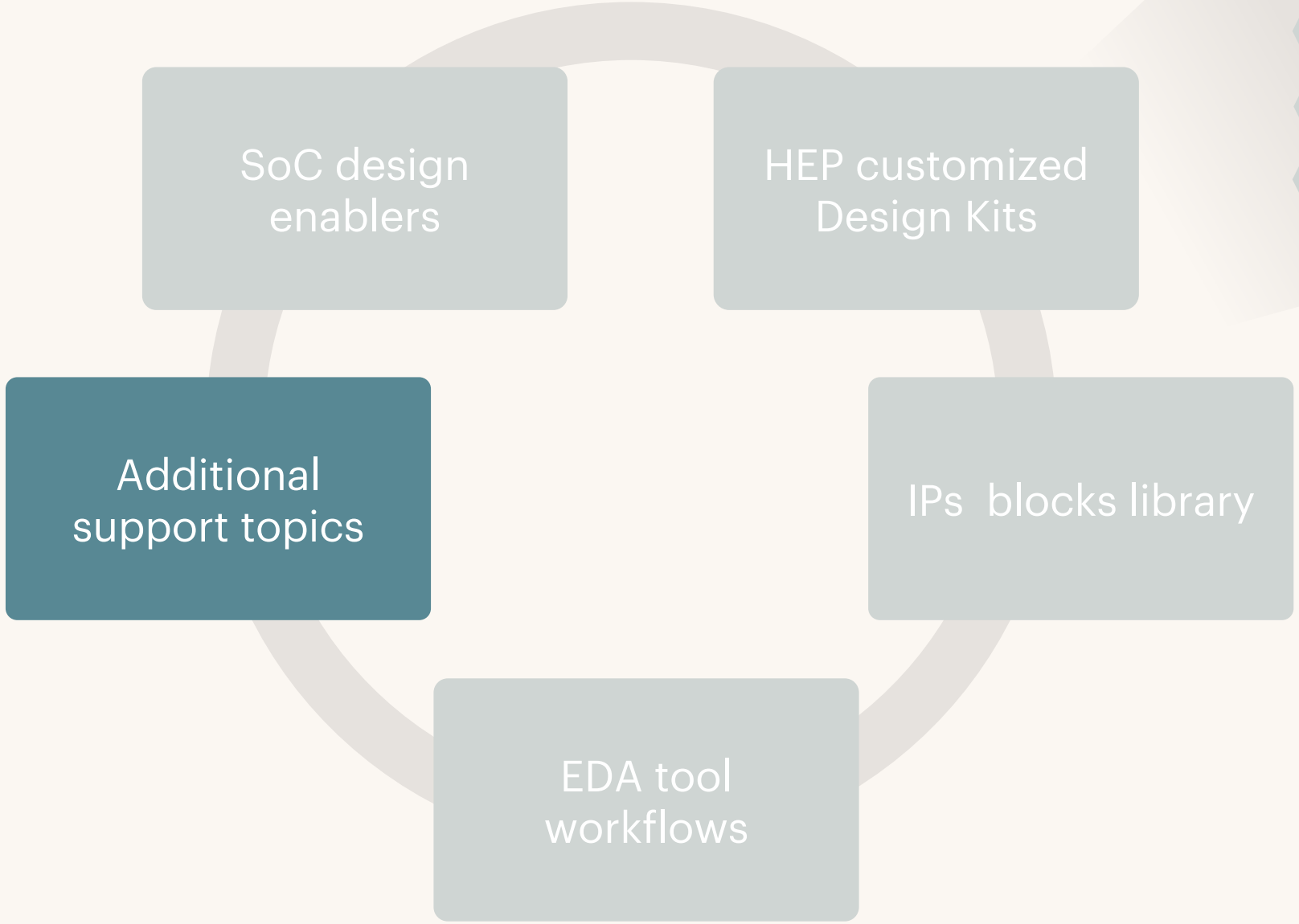
F1 130nm

F2 130nm

F2 65nm

F2 28nm

Advanced tech



Unify environment with containers

Running the EDA tools in containers?

Based on  ← Singularity fork

Also thanks for the support of Kennedy Caisley (Bonn)

The Investigations started for internal CERN EP-ESE usage was successful

↓

Possibility to provide pre-configured containers to institutes

ADVANTAGES

- Provide constant environment on any worknode places
- Provide coherent environment per each project
- Environment sharing among institutes
- Simplify system maintenance
- Be independent from OS and system dependencies

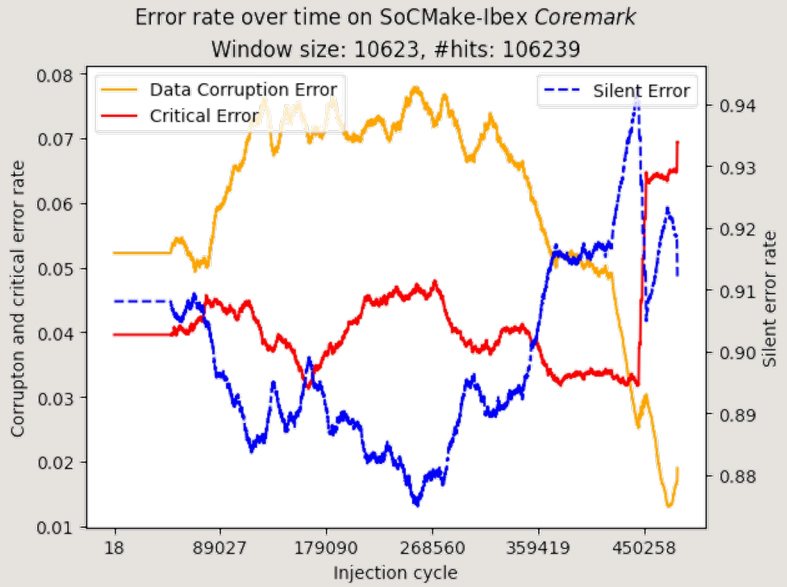
STATUS:

- Testing interactive applications in containers (Cadence/Siemens EDA tools)
- Testing direct submission of batch jobs within the interactive application (Slurm)
- EDA tool installation on mounting point in containers

Other developments

SEE hardening strategies

- Tool to study the effects of SEE on SoC designs
- Target apply redundancy and encoding techniques only where useful and accordingly to needs (hardware-software)
- Metrics analyzer - python-based data analysis of simulation results
- Compare various SoC designs or configurations (e.g. HW-Security features)
- Compare firmware workloads and benchmarks

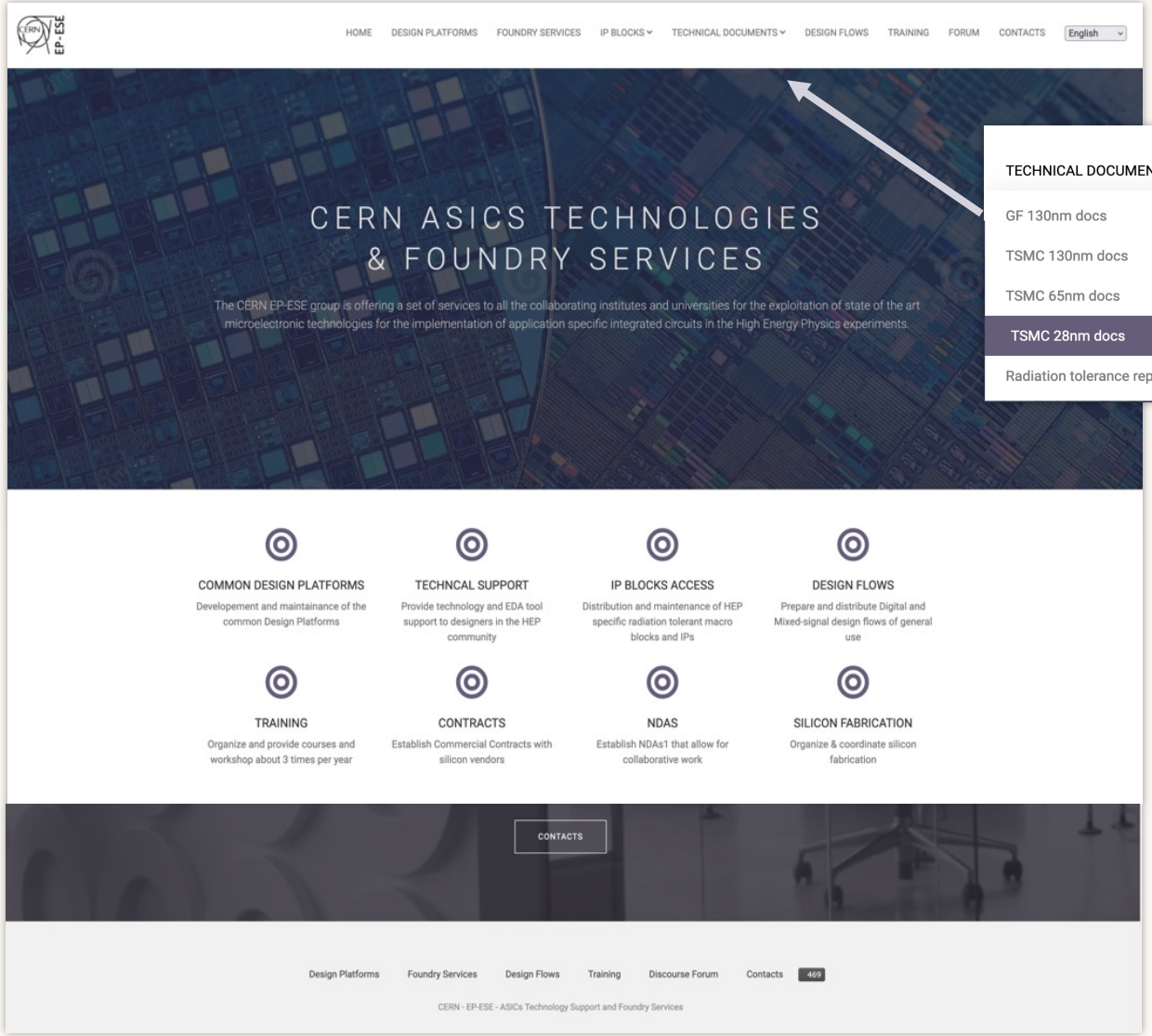


High Level Synthesis - FUTURE PLAN

- We are considering expanding the support as well to HLS topics and related tools usage
  (this may include Cadence Stratus HLS or Symens Catapult)
- We are open to collaborations!

ASIC Support documentation website

https://asicsupport.web.cern.ch



Training courses

INFO AND SUBSCRIPTION: https://asicsupport.web.cern.ch/training_courses/workshop28nm

A total of **145** Designers from HEP institutes have participated to those training workshops in the last 3 years

Digital-on-top hierarchical Implementation in workshop

DoT Workshop

- Learn the main concepts for designing in 65nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Perform synthesis, physical implementation and signoff steps
- Exercise bottom-up and top-down hierarchical design approaches
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2020 TO 2022: **6 TRAINING SESSIONS**

System Verilog Advanced Verification Environment using UVM workshop

Verification / UVM

- Learn the main concepts of functional verification for the High energy Physics
- Learn the main concepts of digital design verification
- Learn about the Universal Verification Methodology (UVM)
- In the lab sessions you will learn how to build your own UVC and verification environment
- A Cadence Training Course adapted for the High Energy Physics community requirements

SINCE 2020: **3 TRAINING SESSIONS**
NEXT SESSION TO BE SCHEDULED

Workshop on Mixed-Signal design in 28nm process

Designing in 28nm

- Learn the main concepts for designing in 28nm for the High energy Physics environment
- Learn the main concepts of the analog and Mixed-Signal design in 28nm, and analog IP characterization
- Learn main concepts about TIDs and SEUs tolerance design
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)

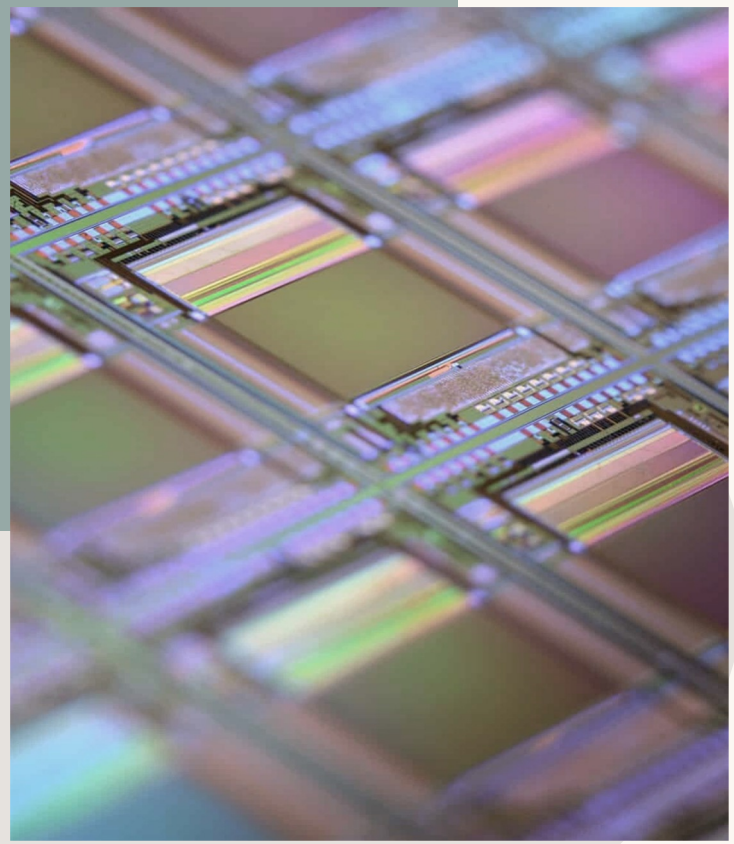
SINCE JAN 2023: **3 TRAINING SESSIONS**
NEXT SESSION END OF 2023

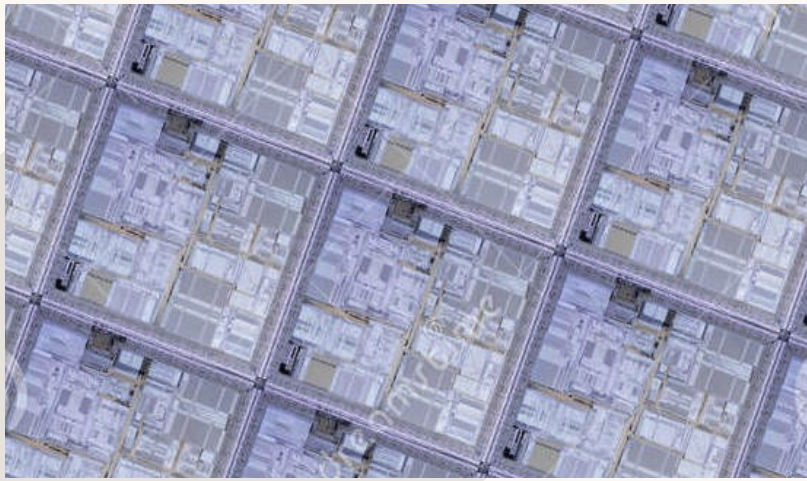
We are looking forward developing new ideas, building methodologies and to improve the support and resources for the HEP community.

Get in touch if you wish to collaborate to the future steps!

As well, we would like to improve the service provided by the CERN ASIC Support, so we need your feedback!

- Which kind of service you feel that you miss and you would like to receive from the CERN ASIC Support Service?
- Are you interested in more specialized trainings courses, tutorials, or simply material?
  For instance something dedicated to radiation tolerance or special needs of design in electronics for the HEP environment?
- Are there some other common design technologies that you would like to be supported by CERN with a common design platform?
- Do you feel enough informed or you would like a more direct communication?
- Could be useful to have dedicated meeting along the year, maybe 2/4 times per year to discuss about the needs of the community?
- Would you need additional documentation, information on the signoff process or documents of other kind?
- We usually provide support for Cadence EDA tools, would you be interested in support for other EDA tool providers?





ASIC Support & Foundry Services

Alessandro Caratelli – Kostas Kloukinas – Marco Andorno

alessandro.caratelli@cern.ch

Backup slides

Addressing the challenges

Technology Challenges

- Complex deep-submicron silicon manufacturing processes
- Powerful, Flexible but highly Complex EDA Tools
- Costly technologies

Design Challenges

- Designs in HEP are increasing in design complexity and size
- Novel designs for scientific instrumentation
- Radiation Tolerance
- Low-power requirements

Productivity Requirements

- Large, fragmented and multinational design teams
- Teams composed by designers with different levels of expertise
- Work on common design projects
- Importance of 'first-time-right' designs!

Enablers for collaborative work

Legal Framework

- Well-established commercial contracts with foundries
- 3-way NDAs with Foundries permitting technology data exchange:

  Standard NDAs allow the team to design in a specific technology but do not allow information sharing among universities or institutes
- EULAs of EDA tool providers permitting IP-blocks and libraries sharing
- IP block sharing agreements among design teams
- Export Control regulations

Technical Framework

- Access to common EDA software tools
- Common set of technology nodes
- Comprehensive “common design platforms”
  - Foundry PDKs & Foundry IP blocks
  - Rad-Tol IP blocks and IP block repositories
  - Rad-Tol SoC infrastructure
  - Design & Verification methodologies
- Maintenance, Training & Support services

The System-on-Chip generation tool summary (work in progress)

HARDWARE GENERATION

- ✓ Top-level HDL generation
- ✓ Interconnect blocks and infer crossbars and adapters
- ▪ *Generate configuration for Synthesis and Implementation*
- ✓ Documentation generation
- ▪ *IP-blocks integration generation*
- ▪ *Hardware accelerators automatic integration*

BUILD SYSTEM

- ✓ EDA tools abstraction layer
- ✓ Cross-compile application software (for RISC-V instruction set or other)
- ✓ Compile verification environment (C++, SystemC, SystemVerilog)
- ✓ Track dependencies and file changes
- ▪ *CI for testing, packaging, deployment*

SOFTWARE GENERATION

- ✓ Drivers generation C++ 17 HAL (Hardware abstraction layer)
- ✓ Linker script generation

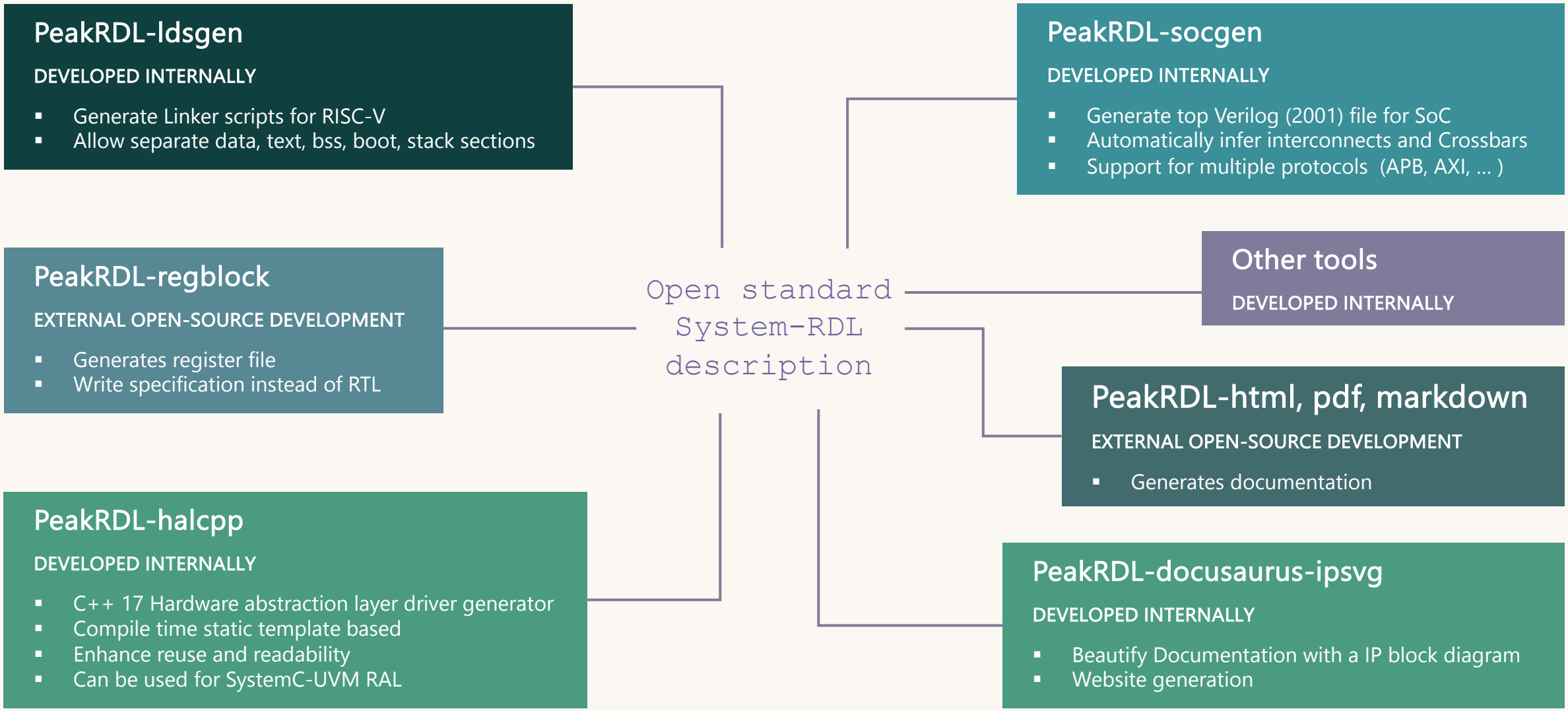
VERIFICATION

- ✓ Assemble and build Verification environment
- ▪ *SystemC-UVM environment generation*
- ✓ Support for open-source simulation tools (Verilator)
- ▪ *Support for commercial verification EDA tools*
- ▪ *FPGA Emulation*

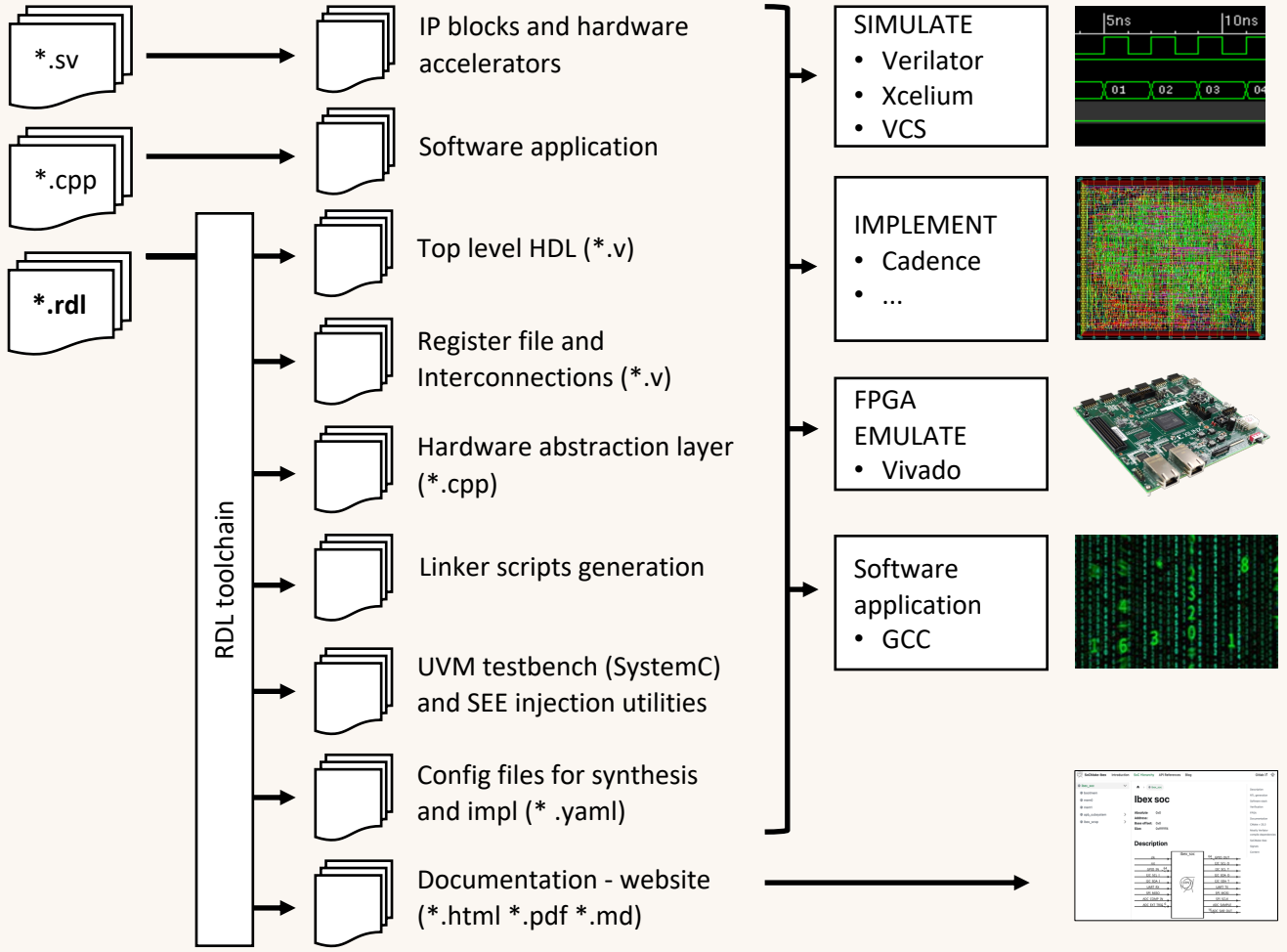
LEGEND: ✓ Development in advanced stage
▪ *Not developed yet*

The peakRDL toolchain https://gitlab.cern.ch/socmake

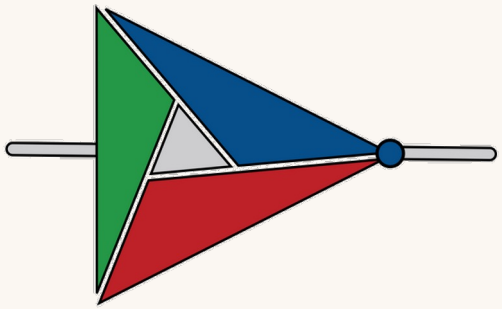
SoCMake support the peakRDL toolchain (work in progress - more components needs to be added)



Hardware generation Software generation



The SoC generator build system



DOC: https://socmake.docs.cern.ch

GIT: https://gitlab.cern.ch/socmake

The SoCMake **build system for Hardware** and SoC designers.

It aims to provide a complete workflow for simulating, implementing and developing System on Chip designs.

SoCMake is an **extension of CMake** build system.
CMake is a mature and widely used build system, and it can easily cover the **requirements needed for hardware design**.

Having a native C++ support, gives ability to compile **SystemC testbenches** and C or **C++ application codes** for simulated processors.

This makes SoCMake especially good for SoC designs and eliminates the need for yet another build system for simulation and software stack.

✓ The SoC generator verification environment

- Based on the Accellera UVM libraries for SystemC
  - Open-source simulators, compile with GCC
  - Write C++ instead of SystemVerilog
  - Reuse target CPU Application in verification (simulate hardware with actual application software)
  - Possibility to use C++ and Python libraries
  - Possibility for constraint randomization and functional coverage with external libraries
- For the moment support only for Verilator.
  Support for commercial verification tools (Xcelium, VCS) will be introduced in the future
- Includes a tool to study the effects of SEE on SoC designs
  - Compare various SoC designs or configurations (e.g. HW-Security features)
  - Target redundancy and encoding techniques according to the effect on the system (hardware-software codesign)

28nm RadTol IP blocks library

https://asic-support-28.web.cern.ch/ip-blocks/

- RADIATION TOLERANT ESD PROTECTIONS
  - Outsourced to SOFICS by the CERN ASIC Support
- SRAM MEMORIES
  - Compilers purchased from the Foundry by the CERN
- RADIATION TOLERANT CMOS IO PAD
  - Outsourced to SOFICS by the CERN ASIC Support
- EFUSES
  - IP block purchased from the Foundry by the CERN
- BANDGAP VOLTAGE REFERENCE & TEMP MONITOR
  - **G. Traversi** (Bergamo/Pavia) / INFN Falaphel project
- SLVS DIFFERENTIAL LINE DRIVERS AND RECEIVERS
  - **Franco Bandi** (CERN EP-R&D WP5)
- RAIL TO RAIL OPERATIONAL AMPLIFIER
  - **Jan Kaplon** (CERN EP-ESE)
- DIGITAL TO ANALOG CONVERTER (8-BIT)
  - **Markus Piller** (DOCT, CERN EP-R&D WP5)
- RAIL-TO-RAIL DIGITAL TO ANALOG CONVERTER (8-BIT)
  - **V. Sriskaran** (CERN EP-ESE)
- ΣΔ ADC for monitoring (12b incremental/16b free running)
  - **Tobias Hoffman** (CERN EP-ESE)
- ΣΔ ADC for monitoring (12b)
  - **O. C. Akgun**
- TID MONITORING CIRCUIT
  - **Giulio Borghello** (CERN EP-ESE)
- Multichannel TDC
  - **C. Rudorf** (University of Ulm)

65nm RadTol IP blocks library

https://asic-support-65.web.cern.ch/ip-blocks/

- RAD-TOLERANT AND SEU TOLERANT SRAMs
  - CERN - IMEC
- SINGLE PORT FUNDRY SRAMs
  - Compilers purchased from the Foundry by the CERN
- DUAL PORT FUNDRY SRAMs
  - Compilers purchased from the Foundry by the CERN
- RAD-TOL BANDGAP REFERENCE VOLTAGE DIODE BASED
  - Stefano Michelis (CERN)
- RAD-TOL REFERENCE VOLTAGE DTNMOS BASED
  - **Stefano Michelis (CERN)**
- EFUSES
  - IP block purchased from the Foundry by the CERN
- RAD-TOLERANT ESD STRUCTURES
  - **Outsourced to SOFICS by CERN**
- Rad-Tolerant CERN IO pads
  - **Iraklis Klemastiotis (CERN)**