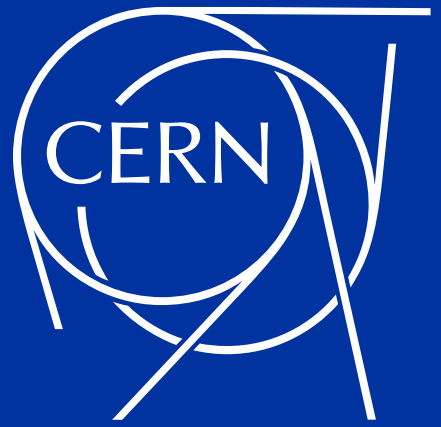


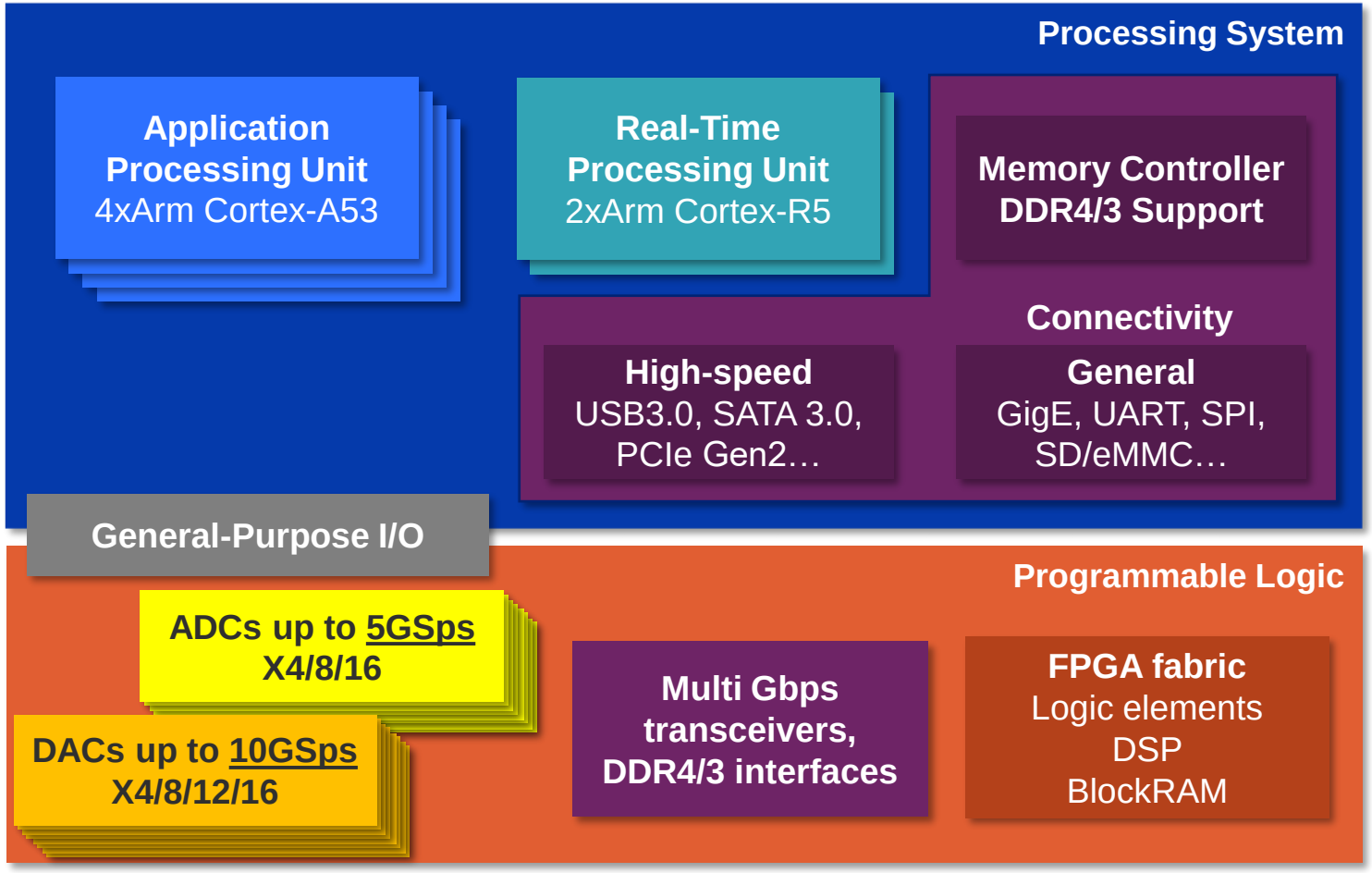
RF System-on-Chip use in the CERN Beam Instrumentation group

Andrea Boccardi, **slides from Irene Degl'Innocenti's presentation to the CERN 3rd SoC workshop** – CERN SY-BI-BP

TWEPP 2023 - FPGA user group

The RF-SoC: what is it?

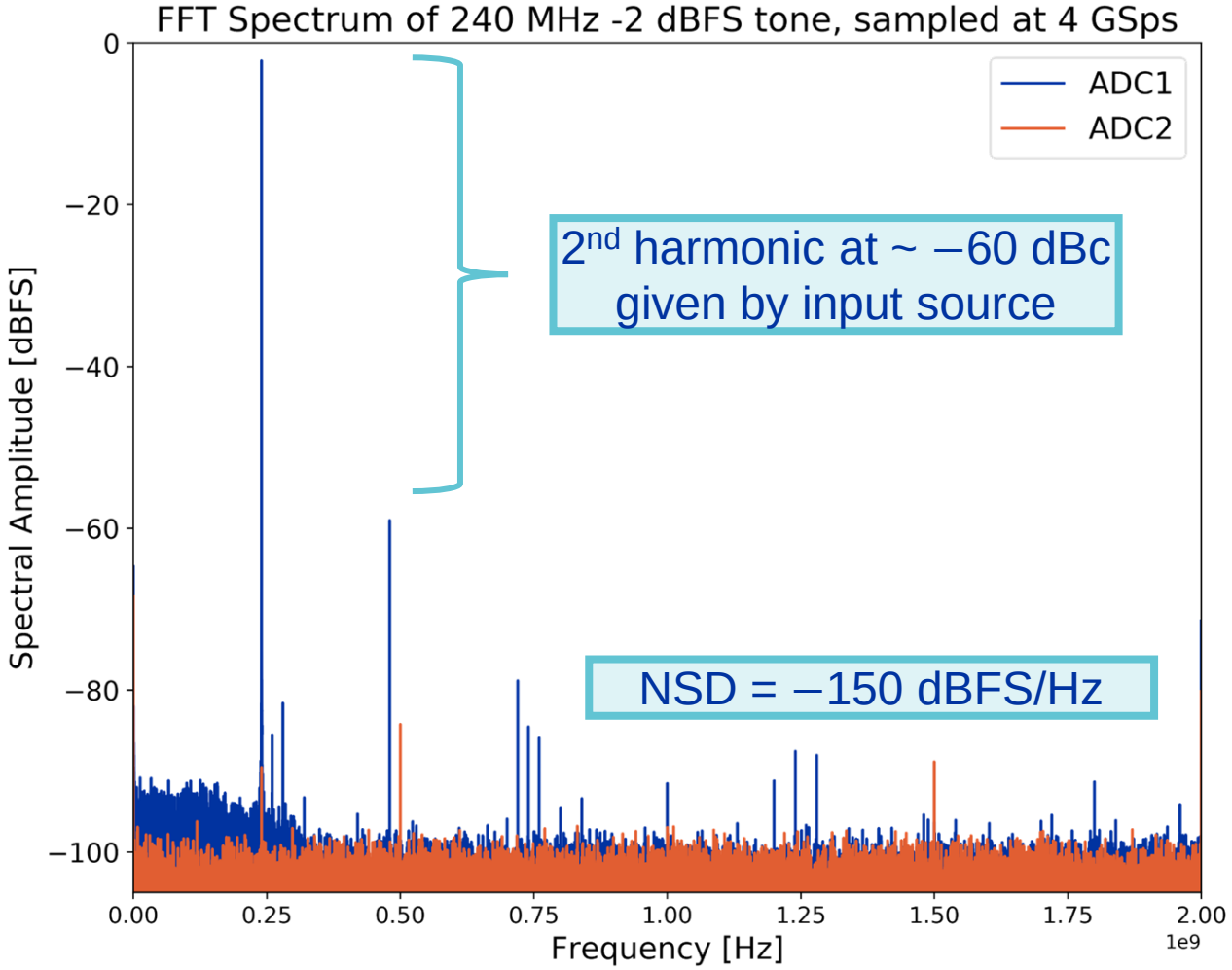
The RF System-on-Chip Technology



The RF-SoC: performance and cost comparison

The RF System-on-Chip Technology

ADC Performance

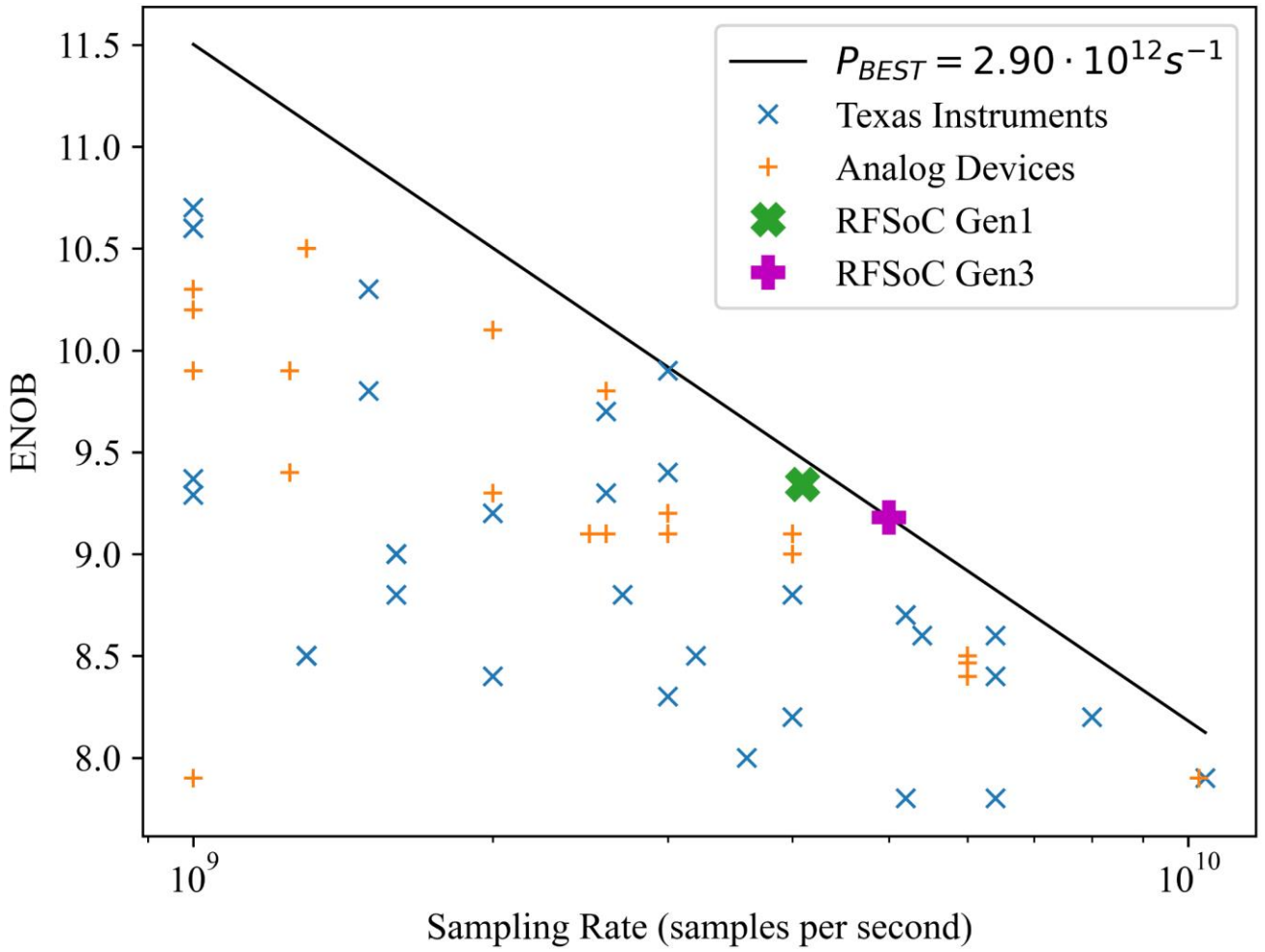


	SNR (dBFS)	SFDR (dBFS)	ENOB
AD9208[1] (14b, 3 GSps)	60.2	78	9.7
RFSoC (12b, 4 GSps)	*58*	74[3]	*9.3*
TI 12DJ4000RF[2] (12b, 4 GSps)	57	67	9.0

1. Analog Devices, AD9208 Data Sheet link
2. Texas Instrument, ADC12DJ4000RF Data Sheet, link
3. J.E. Dusatko, “Evaluation of the Xilinx RFSoC for Accelerator Applications”, in *Proc. NAPAC'19*, Lansing, MI, USA, Sep. 2019, pp. 483-486. link

The RF System-on-Chip Technology

ADC Performance

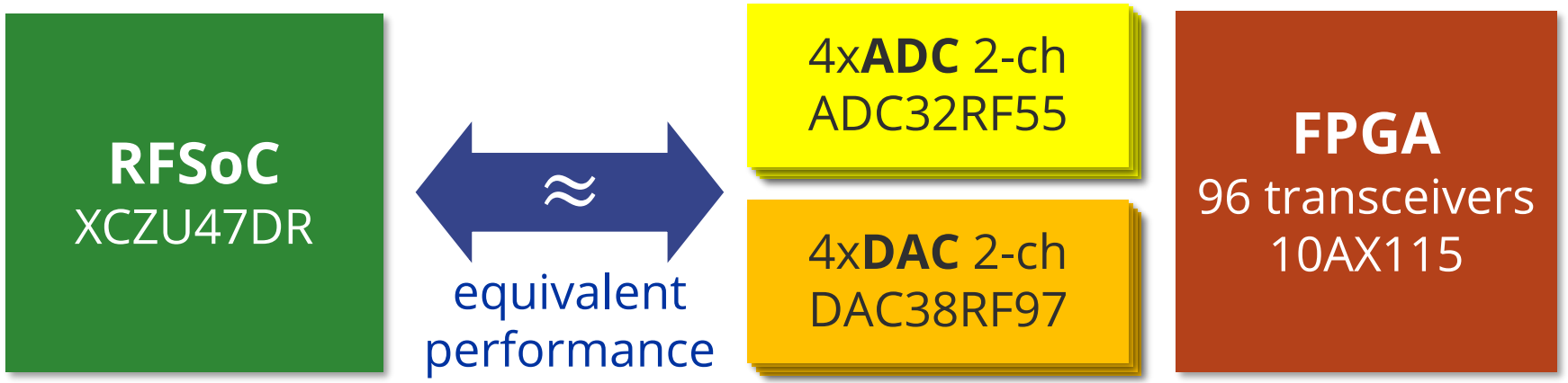


Measurement of performance

$$P = 2^{\mathrm{ENOB}} \times F_s$$

RFSoC Gen3 ADCs have **excellent P**

The RF System-on-Chip Technology
Comparison with discrete solution



	Discrete	RFSoC
Cost (k$)	18.0	20.3
IC count	9	1

Total cost per architecture for IC, indicative prices for small quantities found online.

Summary

Cost
RF-SoC ~10% pricier

Integration
Less PCB area
Less power

Development
Less interfaces
OS and CPU

The HL-LHC BPM development as a case study

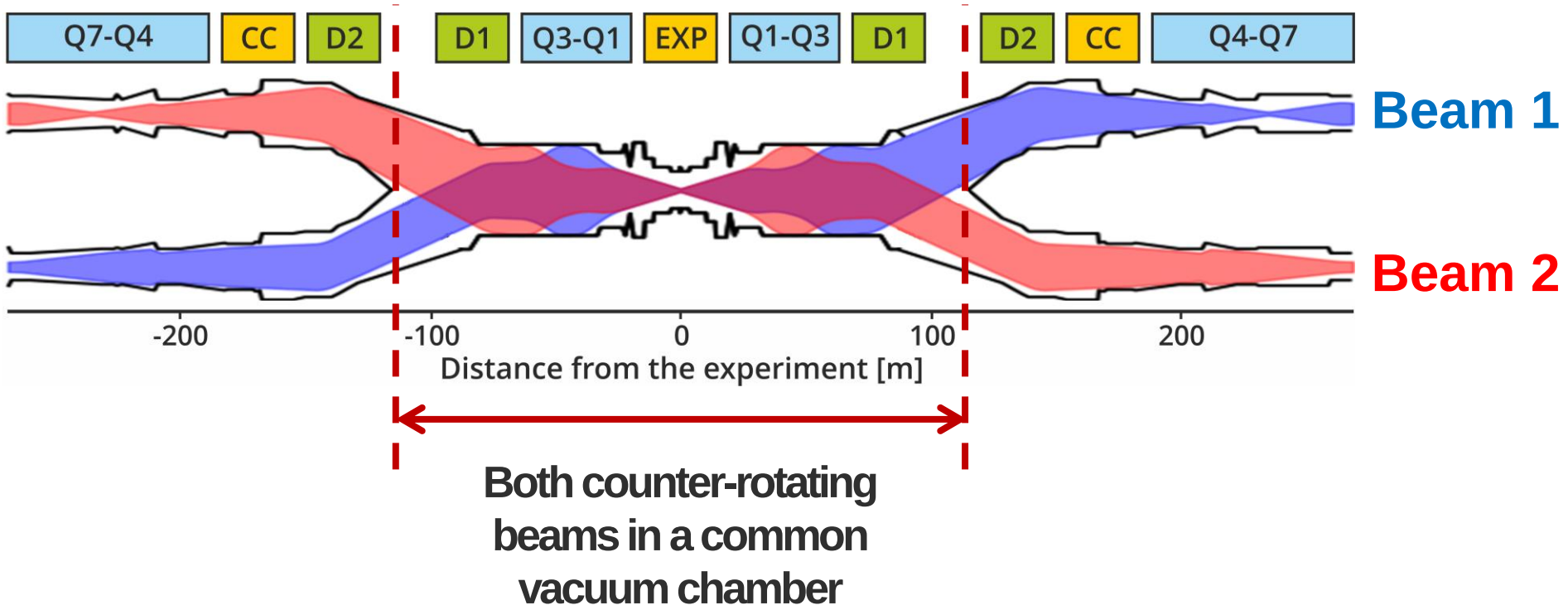
HL-LHC Beam Position Monitor Upgrade

What is a Beam Position Monitor?

HL-LHC Beam Position Monitor Upgrade

New BPMs close to interaction regions

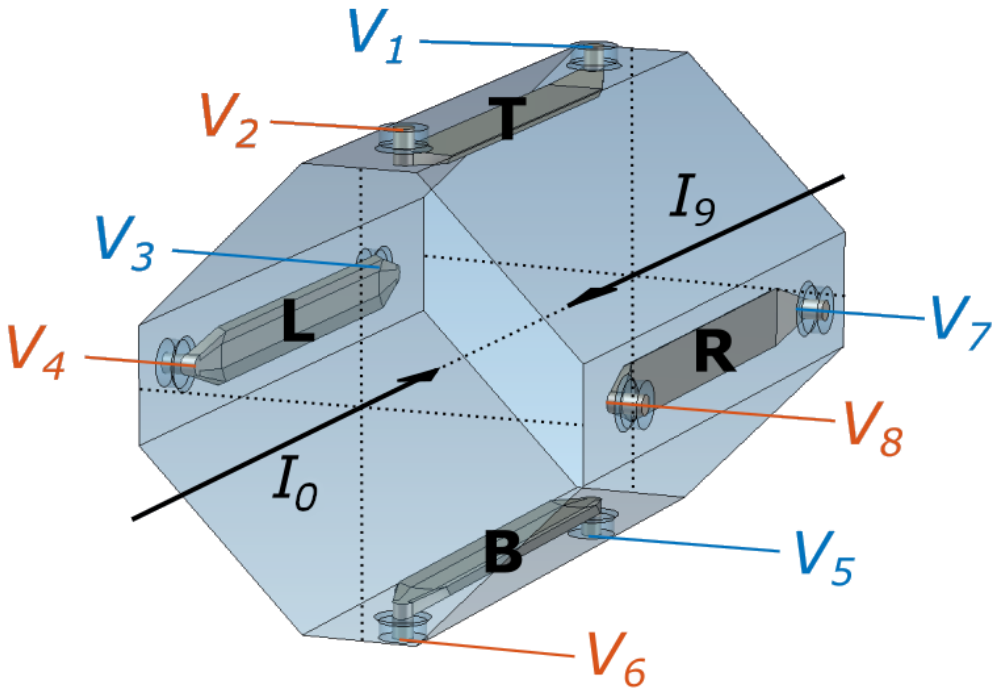
New BPMs in the immediate vicinity of interaction regions 1 (ATLAS) and 5 (CMS), where the two beams coexist within a single pipe

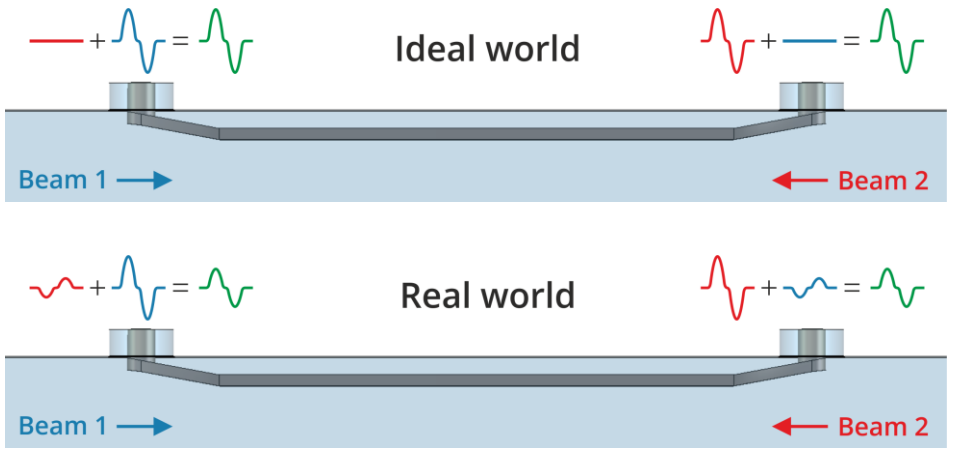


HL-LHC Beam Position Monitor Upgrade

Directional Couplers

In a good directional coupler a signal is seen mostly at the upstream ports





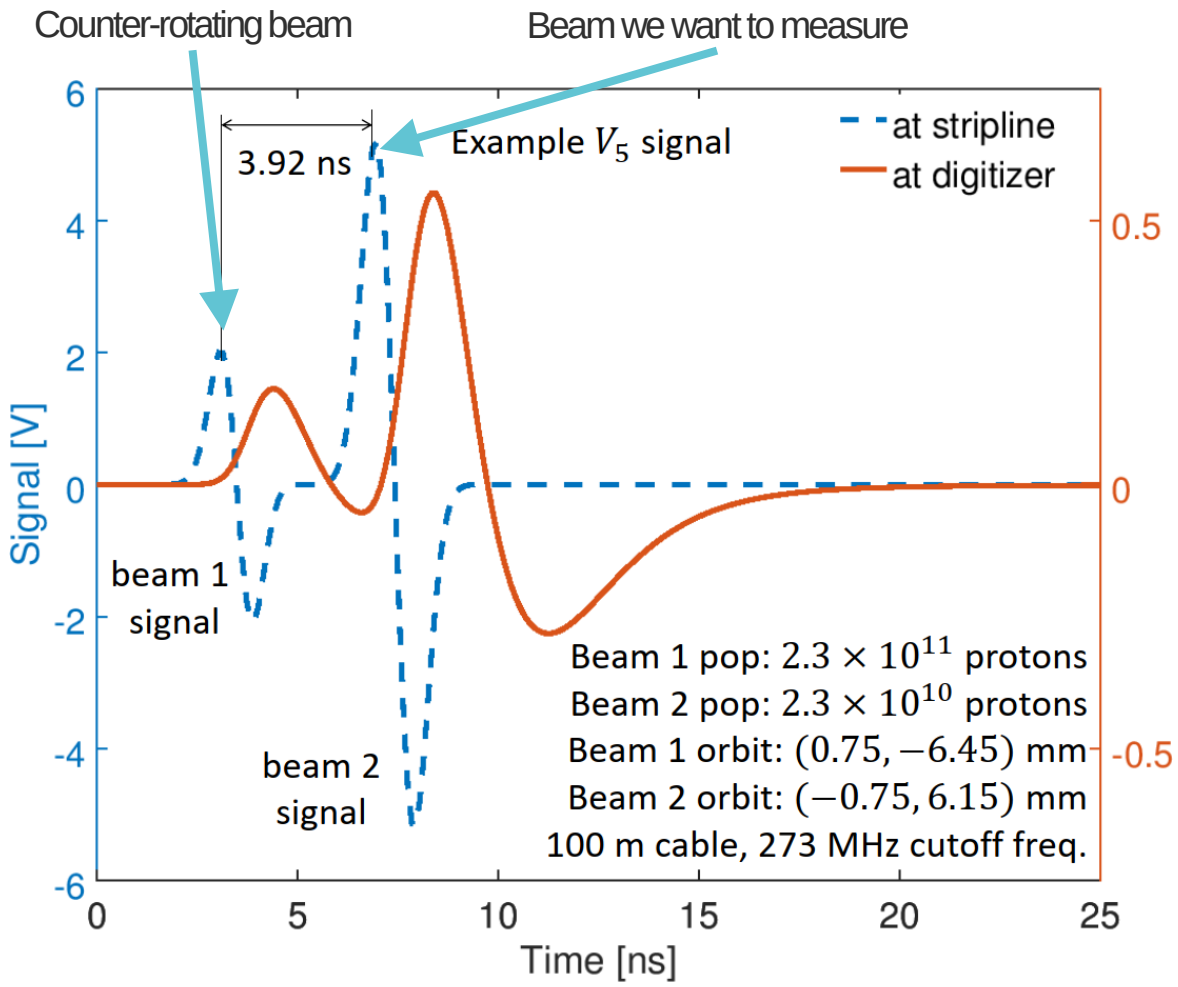
HL-LHC Beam Position Monitor Upgrade

Beam to beam distortion

The presence of the other beam affects the measurement when:

- Short bunch crossing time
- Intensity of the other beam significantly higher

The distortion of the beam signals due to the presence of the other beam must be compensated for



Resources Estimation for HL-LHC BPM
Digital Acquisition Requirements per Stripline

- **Fast digital acquisition of 8 waveforms** → 8 ADCs: > 2 GSps, > 8.5 ENOB
- **Digital Signal Processing implementation**
  - **Power** computation
  - **Power Compensation algorithm** (each waveform: 4 multiplications + 1 division + 2 square root) [IBIC21]
  - **Beam Position Monitor** functionality
    - **Continuous log of averaged low-volume data**
    - **On demand storage of high-volume data**
    - Calibration → 8 DACs

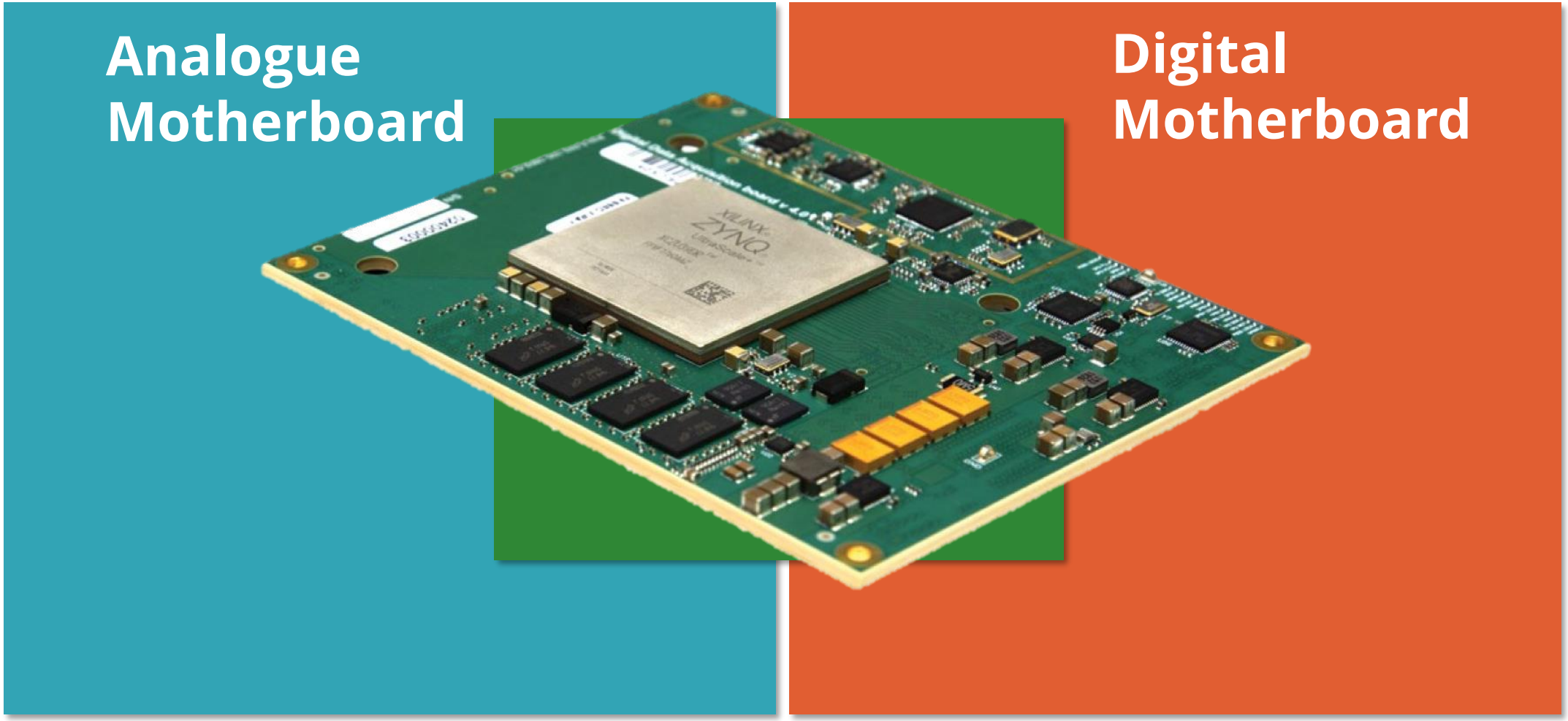
→
- Logic
- Memory Size
- Memory Bandwidth
- Transmission Bandwidth

Resources Estimation for HL-LHC BPM

Resources estimation

Resources	Required qty.	% RFSoC
ADCs	8	100 %
DACs	8	100 %
Internal memory	30 Mb	48 %
DSP	172	4 %
LUT	20521	5 %
FF	50644	6 %
DDR	768 Mb	3 %
DDR WR peak BW	22 Gbps	24 %
Read-out BW	54 Mbps	~10 %

Quick overview of the DAQ architecture (to be…)

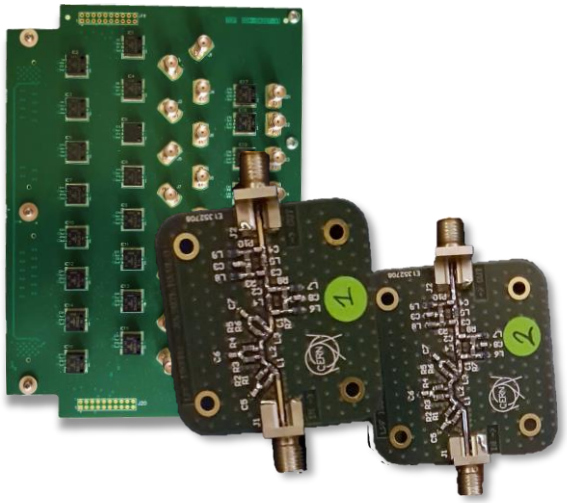


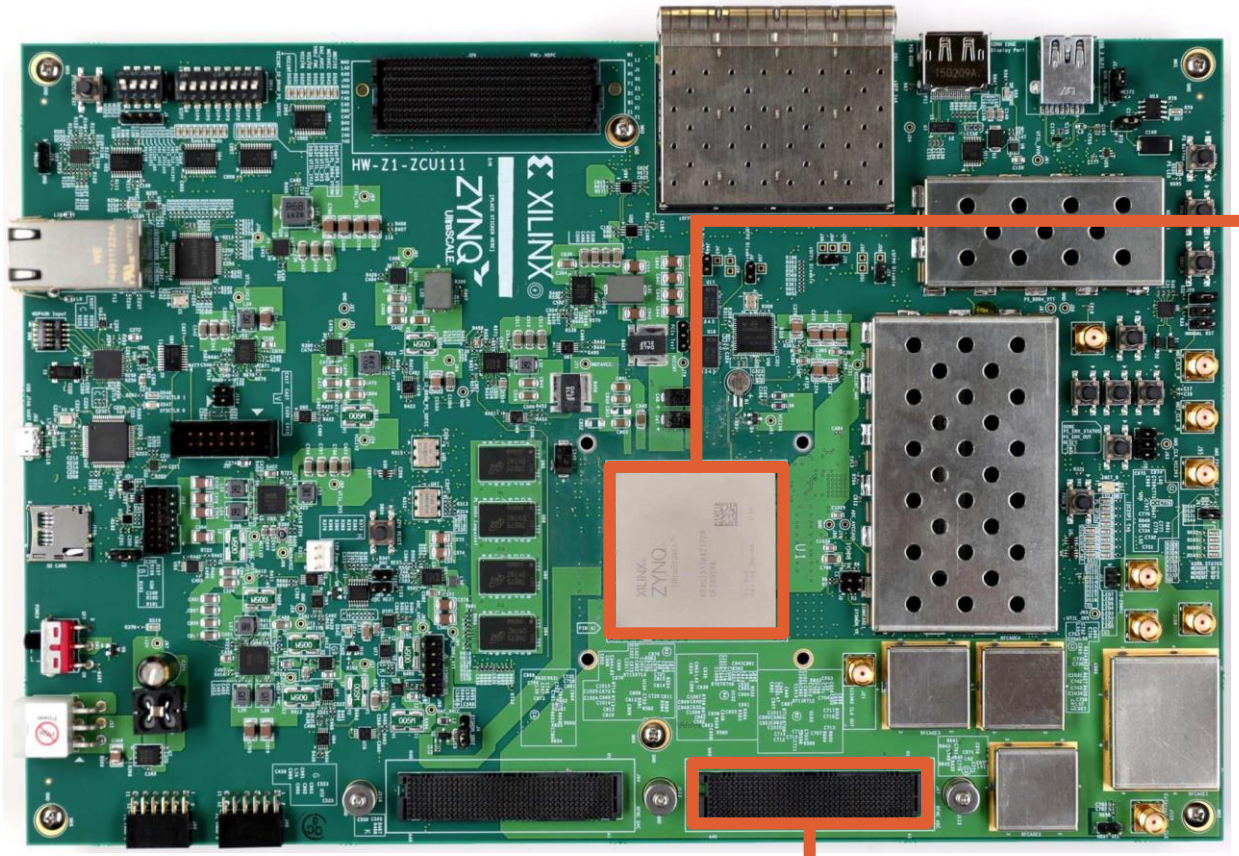
RF-SoC learning curve and development time
Zero to hero journey example

Example

RFSoC 4-channel scope on ZCU111 evaluation board

Price ~11 k$

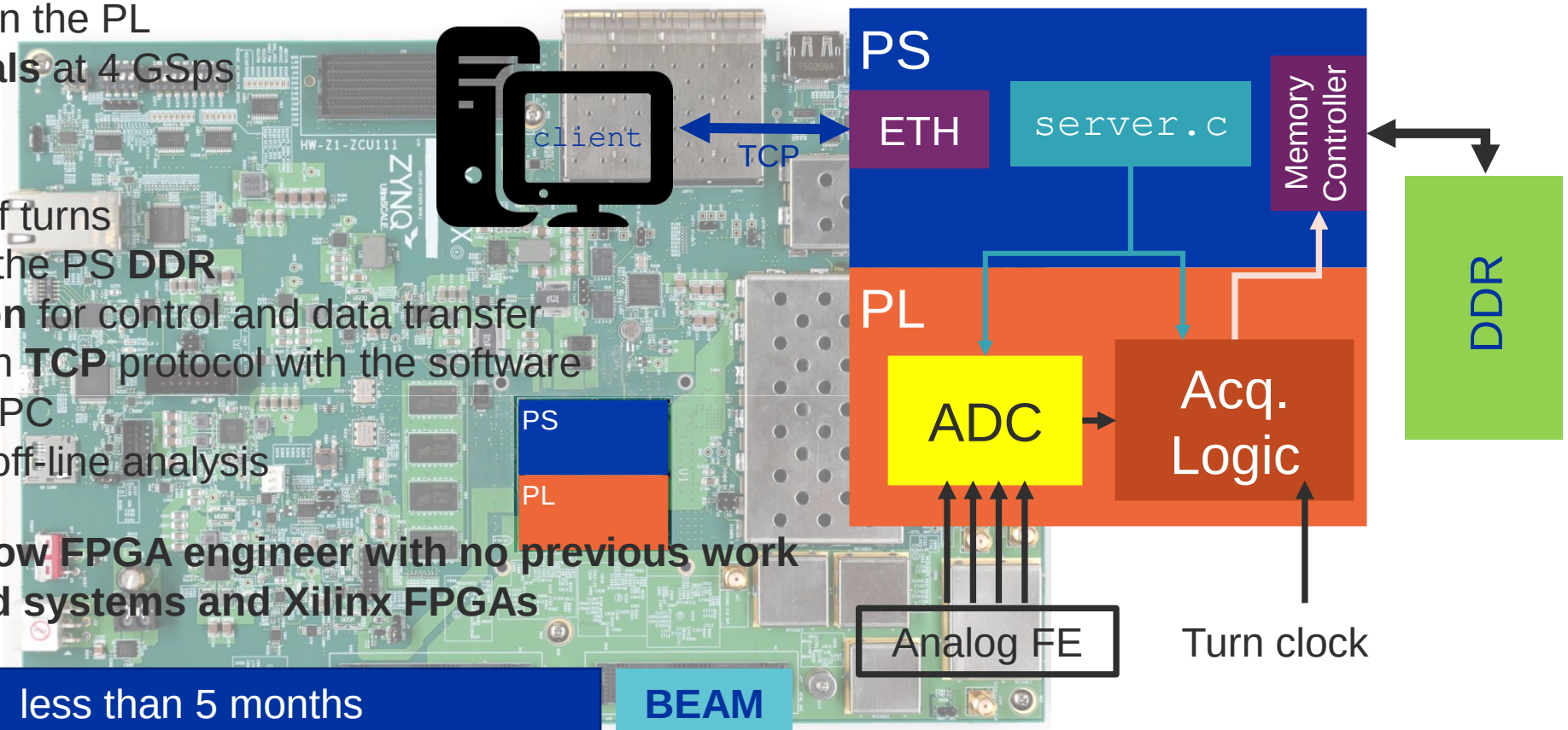




Example

RFSoC 4-channel scope on ZCU111 evaluation board

- **FPGA logic** and **ADC** in the PL
  - digitization **4 signals** at 4 GSps
  - selected window
  - turn clock
  - selected number of turns
- Storage of raw-data in the PS **DDR**
- **APU server application** for control and data transfer
- Communication through **TCP** protocol with the software running on an external PC
- Raw-data read-out for off-line analysis

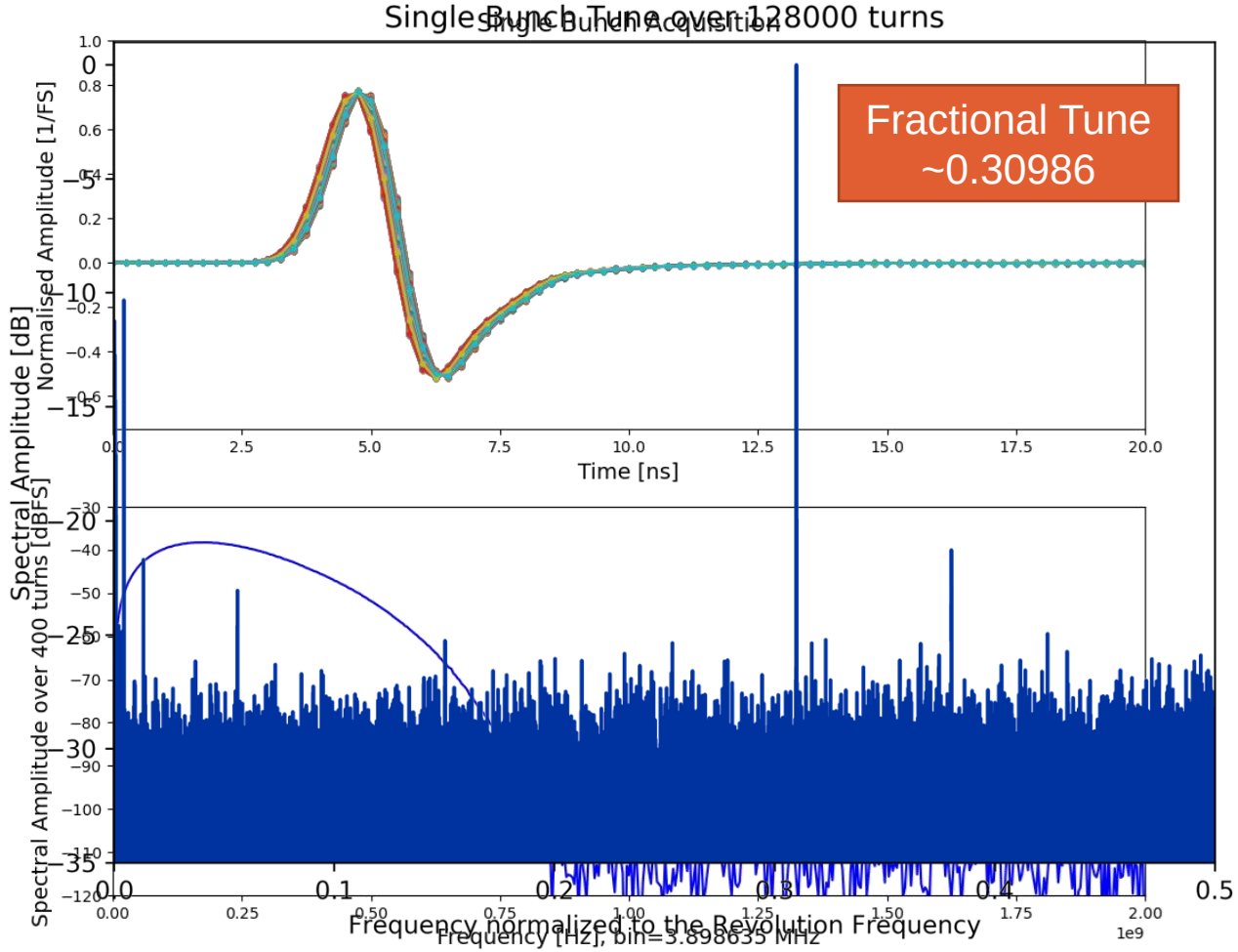


Development by one fellow FPGA engineer with no previous work experience on embedded systems and Xilinx FPGAs

6 weeks courses	less than 5 months actual development (GW+FW+SW)	**BEAM TEST**

RFSoC Scope: Beam Raw Data Acquisition

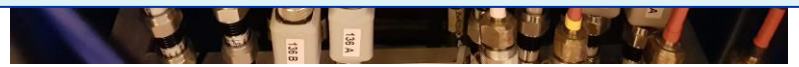
Measurements of LHC Stripline



Several raw data acquisitions for the HL-LHC BPM studies

- 4 channels at 4 GSps
- Memory per acquisition: ~**2 GB**
- Longest acquisition (<400 MB) single bunch for **128000 consecutive turns** (more than 11s of observation)

- **First Results: IPAC23-THPL119**

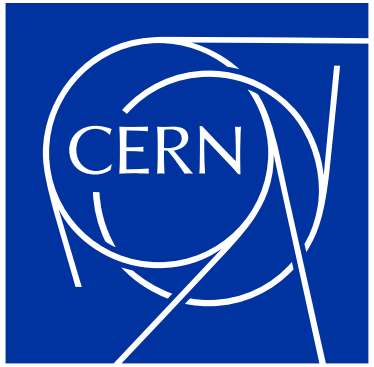


Conclusions…

I would like to say “none really: this was meant to be an excuse to start a conversation in this user group, and maybe a collaboration?”

But looks weird a presentation without conclusions, so:

- **RF-SoC is a very promising technology**
- **The RF-SoC will be the core of the HL-LHC IR BPM system**
  - It is estimated that for this relatively complex system we will not go beyond 50% of the available resources in the FPGA logic
- **There are many resources online to get up to speed with designing for RF-SoC, still is a quite complex flow**
  - As a reference 6 months to take a young digital engineer from virtually 0 to beam-tests (with a dev-kit!)



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