

## **Session Program**

**1-6 Oct 2023**



# **TWEPP 2023 Topical Workshop on Electronics for Particle Physics**

***ASIC***

Geremeas, Sardinia, Italy  
Calaserena Village, Geremeas, Quartu S.Elena, Sardinia (Italy)

# Monday 2 October

14:45

## ASIC

**Session** | **Location:** Mistral Room | **Convener:** Angelo Rivetti

14:45–15:05

**Performance of H2GCROC3, the readout ASIC of SiPMs for the back hadronic sections of the CMS High Granularity Calorimeter.**

**Speaker**

Jose David Gonzalez Martinez

15:05–15:25

**First test results for ECON-T and ECON-D ASICs for CMS HGCAL**

**Speaker**

Cristina Ana Mantilla Suarez

15:25–15:45

**Testing and characterisation of the prototype readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker**

**Speaker**

Michael Grippo

15:45

16:15

## ASIC

**Session** | **Location:** Mistral Room | **Convener:** Ping Gui

16:15–16:35

**Design and characterization of RD53C production chips for ATLAS and CMS pixel upgrades at HL-LHC**

**Speaker**

Luca Pacher

16:35–16:55

**Performance of the COLUTA ADC ASIC for the ATLAS HL-LHC Liquid Argon Calorimeter Readout**

**Speakers**

Michael Himmelsbach, Michael Himmelsbach

16:55–17:15

**Chips for calibration of the ATLAS LAr calorimeter**

**Speaker**

Mr Ludovic Raux

17:15

## Tuesday 3 October

09:00

### ASIC

**Session** | **Location:** Mistral Room | **Convener:** Marcus Julian French

09:00–09:20

#### The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results

**Speaker**

Gianluca Aglieri Rinella

09:20–09:40

#### Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

**Speaker**

Chiara Ferrero

09:40–10:00

#### Development of monolithic pixel sensor prototypes for the CEPC vertex detector

**Speaker**

Wei Wei

10:00

11:20

### ASIC

**Session** | **Location:** Mistral Room | **Convener:** David Gascon

11:20–11:40

#### Characterization of the ATLAS Liquid Argon Front-End ASIC ALFE2 for the HL-LHC upgrade

**Speaker**

Dimitrios Matakias

11:40–12:00

#### Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers

**Speaker**

Larry Lou Jr Ruckman

12:00–12:20

#### Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology

**Speaker**

Sandro Cadeddu

12:20

15:20

### ASIC

**Session** | **Location:** Mistral Room | **Convener:** Angelo Rivetti

15:20–15:40

#### Digital on Top methodology for Monolithic Active Pixel Sensor, feedback from MIMOSIS sensors for CBM Micro-Vertex Detector

**Speaker**

Frederic Morel

15:40-16:00

**Tri-axis 5 $\mu$ m hexagon pixel-strip matrix combining 3\*852 current comparator in a 180nm node**

**Speaker**

Edouard Bechetoille

16:00-16:20

**Lab measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype detector with a large breakdown voltage**

**Speaker**

Chenfan Zhang

16:20

17:40

**ASIC**

**Session** | **Location:** Mistral Room | **Convener:** Ping Gui

17:40-18:00

**3D-integrated pixel circuit for a low power and small pitch SOI sensor**

**Speaker**

Yunpeng Lu

18:00-18:20

**NAPA-P1: NANOSECOND TIMING PIXEL FOR LARGE AREA SENSORS**

**Speaker**

Alexandre Habib

18:20

## Wednesday 4 October

09:00

### ASIC

**Session** | **Location:** Mistral Room | **Convener:** Adriano Lai

09:00–09:20

**A low crosstalk 768-channel of 14-bit analog to digital converters for high resolution array of detectors.**

**Speaker**

Dr Daniel Dzahini

09:20–09:40

**Dual use driver for high speed links transmitters in the future high energy physics experiments**

**Speaker**

Mateusz Karol Baszczyk

09:40–10:00

**SET sensitivity study of a VCRO-based PLL for HL-LHC ATLAS HGTD**

**Speaker**

Mr Maxime Morenas

10:00

11:20

### ASIC

**Session** | **Location:** Mistral Room | **Convener:** Christine Guo Hu

11:20–11:40

**Design and Characterization of a precision tunable time delay integrated circuit.**

**Speaker**

Yahya Tousi

11:40–12:00

**In-pixel AI for lossy data compression at source for X-ray detectors**

**Speaker**

Danny Noonan

12:00–12:20

**A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs.**

**Speaker**

Gianmario Bergamin

12:20