Status of the mTCA LLRF development

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Setup: AWAKE run2C

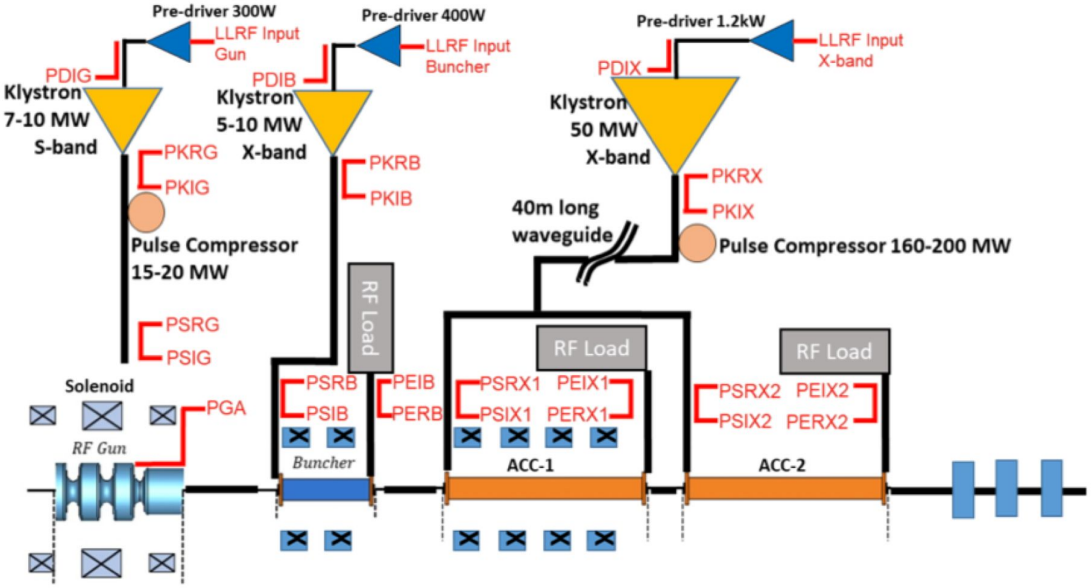
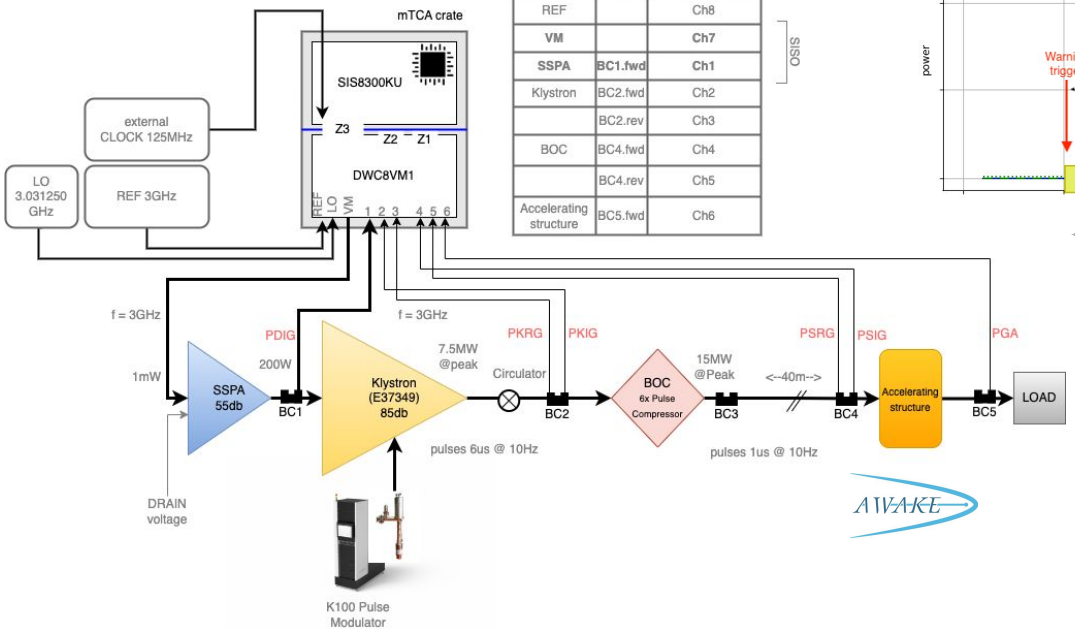
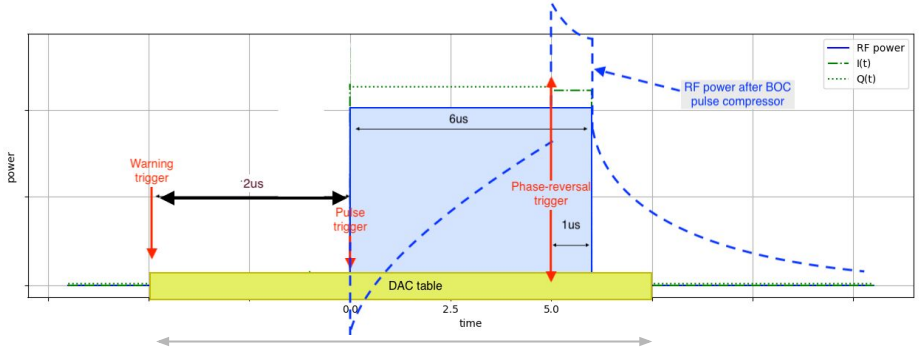


Figure 2 Shows the new electron linac needed for run 2c. The directional couplers and signals that to be treated by the LLRF system are marked in red.

Setup: LLRF



Group	Device	mTCA channel
REF		Ch8
VM		Ch7
SSPA	BC1.fwd	Ch1
Klystron	BC2.fwd	Ch2
	BC2.rev	Ch3
BOC	BC4.fwd	Ch4
	BC4.rev	Ch5
Accelerating structure	BC5.fwd	Ch6



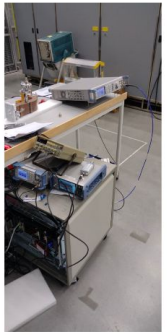
1024 samples (8ns * 1024)

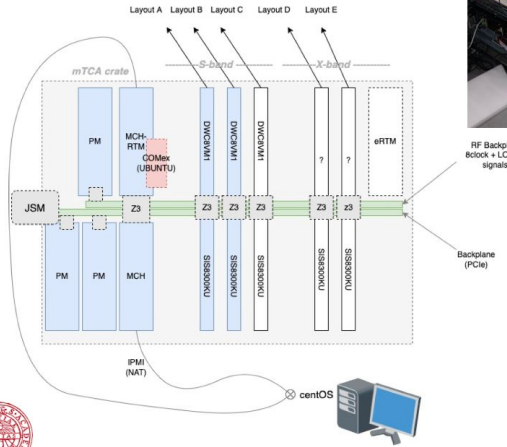
	S-band	X-band
Operating frequency	2.997899068 GHz	11.991596272 GHz
Pulse length	1-10 µs	100-1500 ns
Bandwidth	> 20 MHz	> 20 MHz
Pulse repetition rate	9.97 Hz	9.97 Hz
Number of signals to be acquired	14 + Reference	18 + Reference
Number of signals to be generated	2	2
Jitter	<30 fs	< 30 fs
Amplitude stability	10^{-4}	10^{-4}

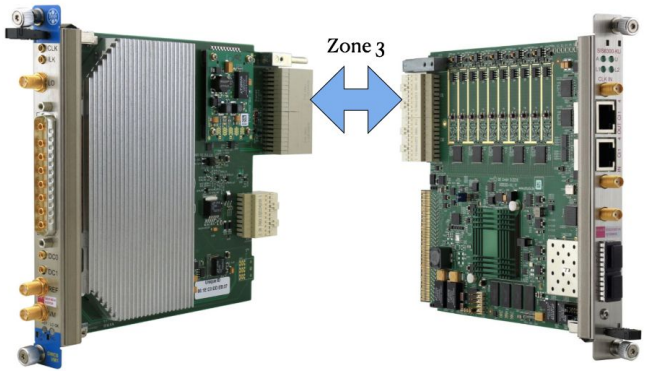
AWAKE 2C specification - prepared by Ben Woolley

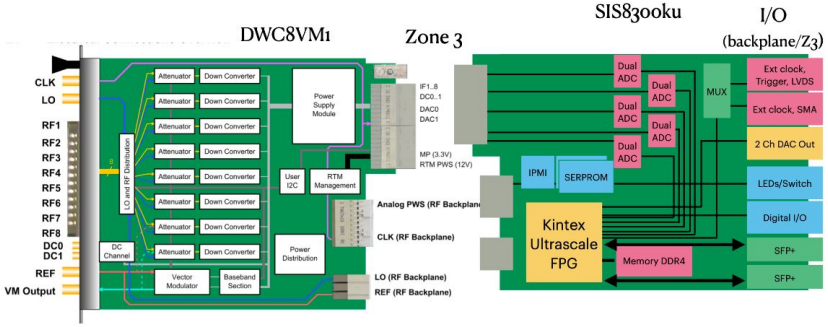
Setup: mTCA LLRF

MTCA crate in UU:









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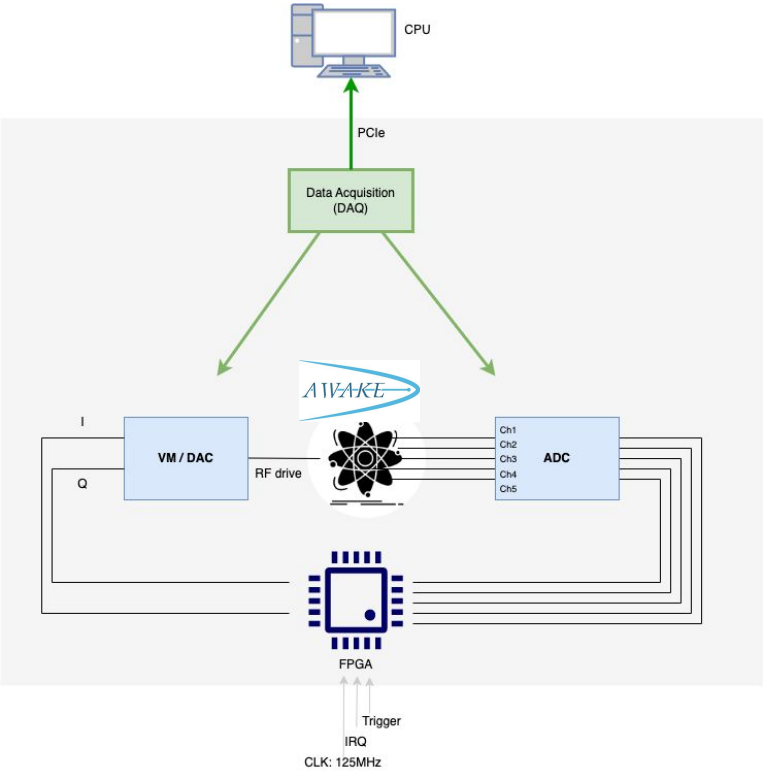
Setup: firmware

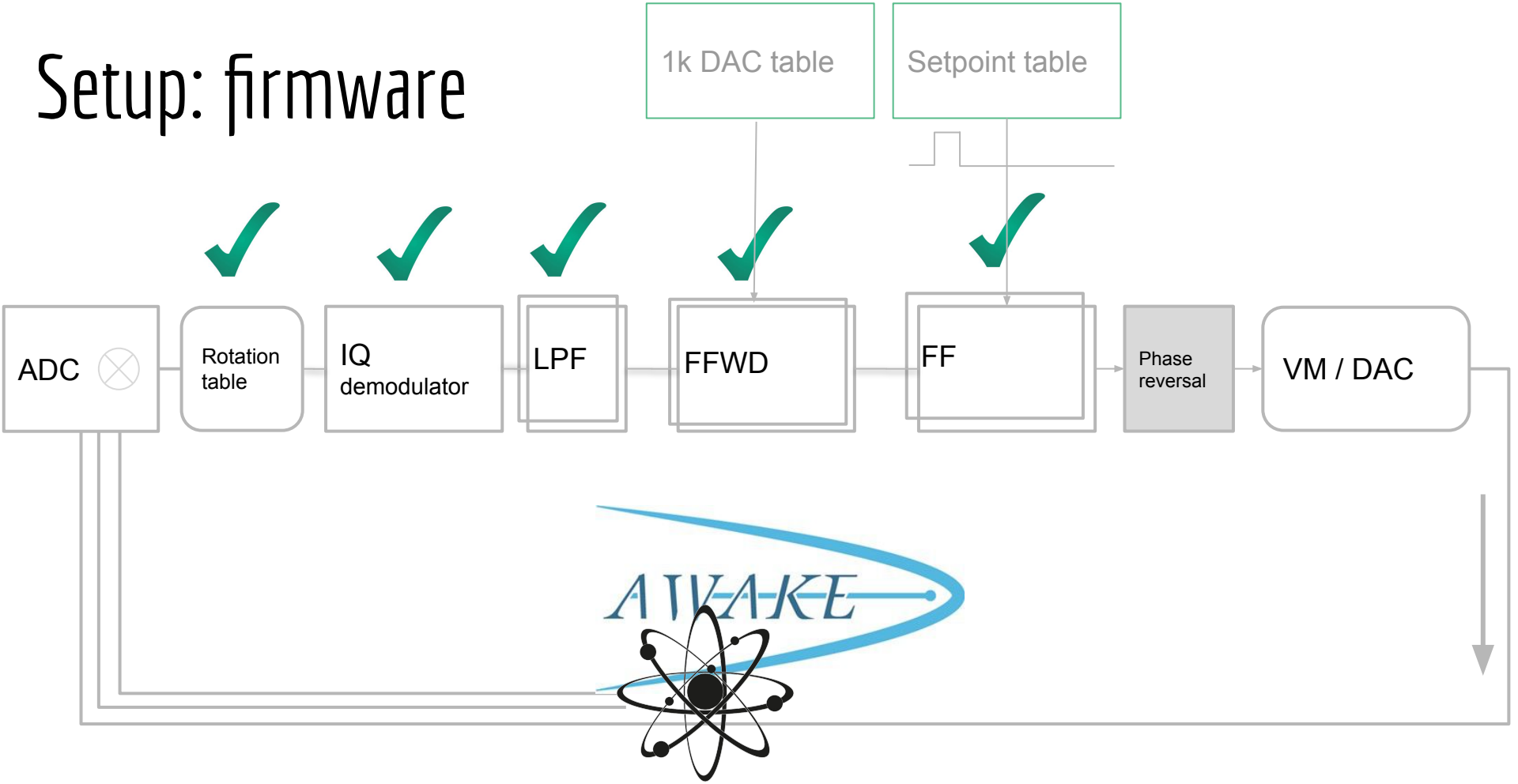


- Building on DESYs open source project (CG).
- DesyRDL (±=FESA).
- AXI4 and AXI4L.
- Xilinx IP: xDMA.
- Added IRQ.
- Augmented by PSI_fix.

Components:

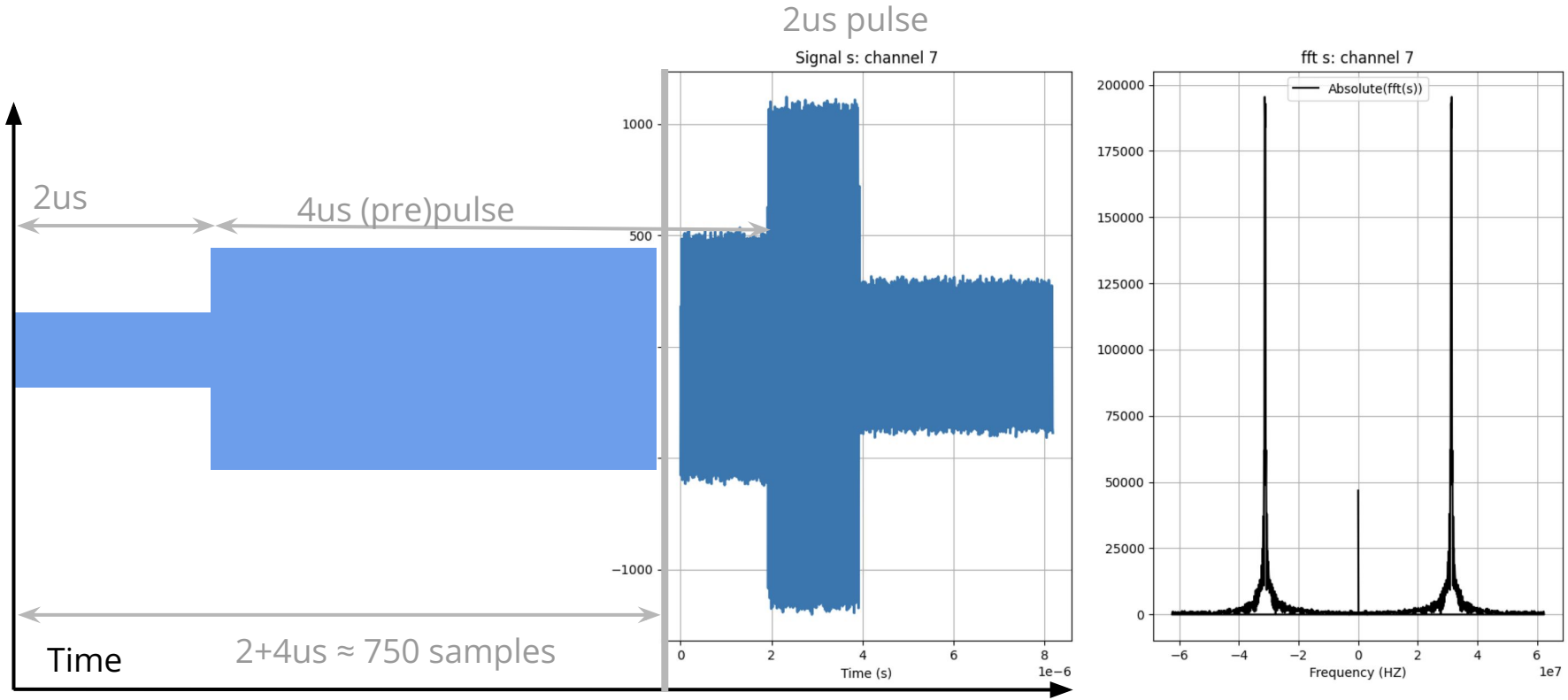
1. Feed forward table.
2. Feedback (PID).
3. IQ demodulator.
4. Rotation table.

Setup: firmware

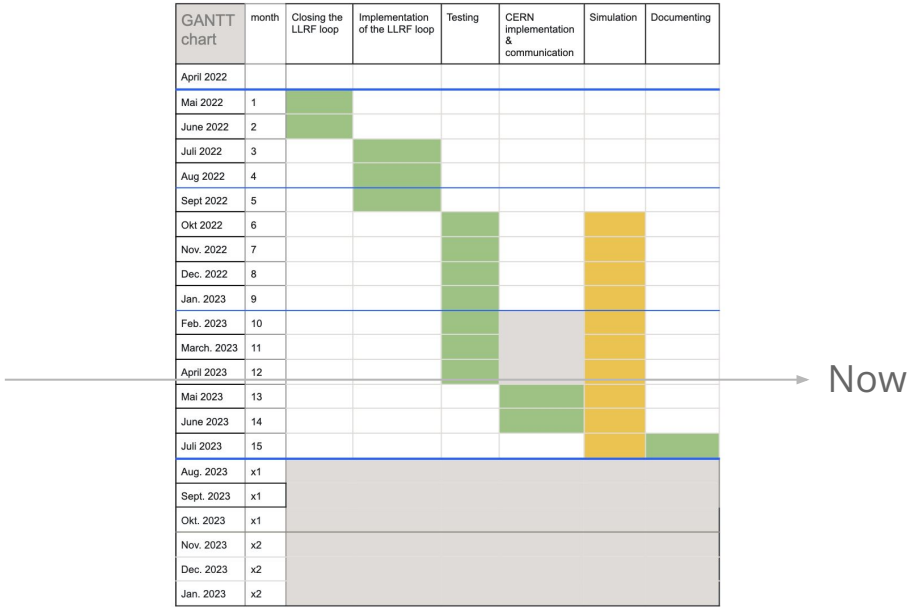


LLRF: Result

IF = 31.25MHz



Timeline & integration



Fast ADC sampling

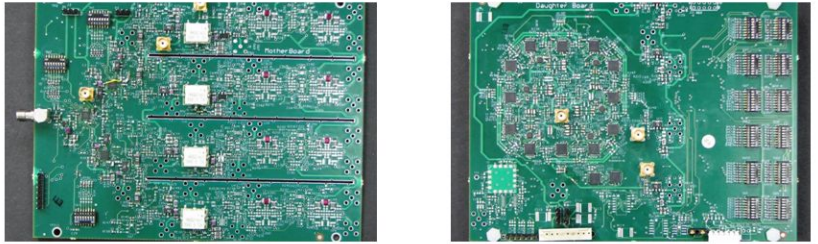
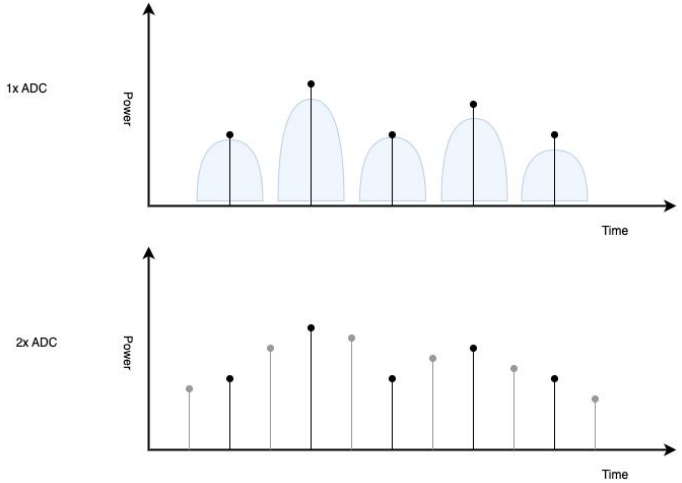


Figure 3. Circuit implementation. The left board realizes the analog mixing and filtering. A sign waveform alternating at 2 GHz is implemented in the right board.

Interleaving ADC:



125 MSPS

250 MSPS

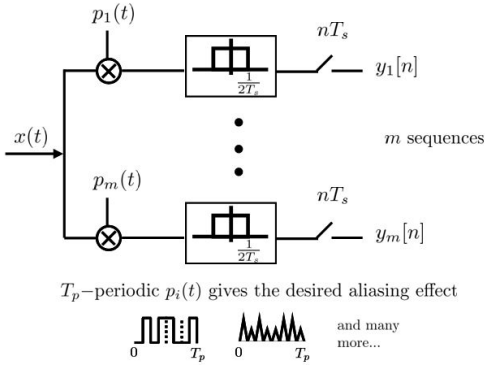


Figure 2. The modulated wideband converter

Conclusions

Questions:

- LLRF setup?
- Results?
- Fast ADCs?