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TOF-enabled Dual-polarity Charge-to-Time Converter based on FPGA for SiPM detector applications

A novel compact charge readout method based on Field Programmable Gate Array (FPGA) voltage-referenced receiver was proposed. In the highly integrated charge readout method, it consists of a dual-polarity Charge-to-Time Converter (dQTC) and digital FPGA. We refer to this new FPGA-based charge measurement method as FPGA-dQTC. In the FPGA-dQTC method, an FPGA input receiver serves as a voltage comparator. To achieve a compact charge readout, the FPGA I/O port was configured as a voltage-referenced receiver instead of a LVDS receiver. The single-ended voltage-referenced receivers share a common reference voltage in each I/O Bank of the FPGA, which maximizes the capability of multi-channel and multi-functionality in our proposed charge measurement method. Experiments in terms of channel linearity and timing performance for the FPGA-dQTC method were carried out. A Coincidence Timing Resolution (CTR) evaluation setup including two PET detectors was built. Each PET detector comprises a $3\times3\times10$ mm³ LYSO crystal coupled with a SiPM detector. The energy resolutions were 10.53% and 10.57% for the two PET detectors. The CTR values between the two detectors were ~ 330 ps for cathode output signal of the SiPM. Experiment results show that the FPGA-dQTC scheme provides a promising method for a compact, multi-channel front end readout electronics for nuclear imaging applications.

Collaboration(s)

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