A 16-Channel Fast-timing ASIC for TRIDENT Large-area SiPM Arrays Readout

Mingxin Wang[a,*] and Weihao Wu[a] for the TRIDENT collaboration

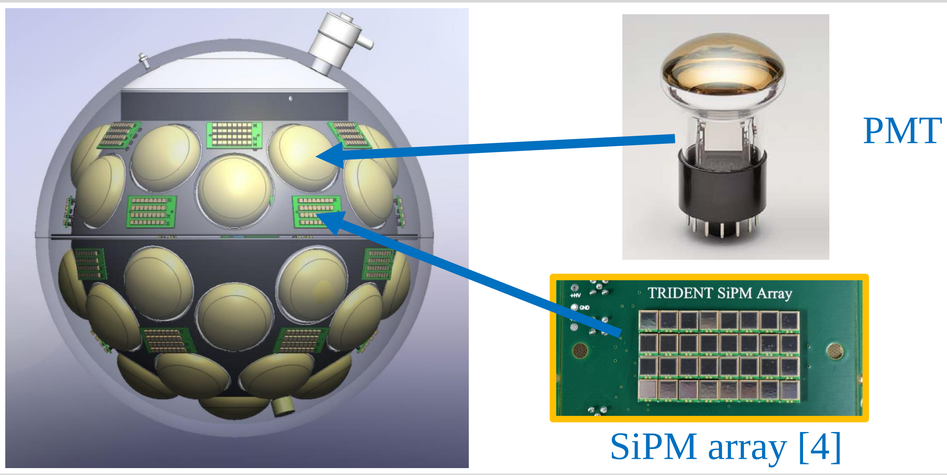
Contact: starkshai@sjtu.edu.cn, wuweihao@sjtu.edu.cn

a. State Key Laboratory of Dark Matter Physics, School of Physics and Astronomy & Tsung-Dao Lee Institute, Shanghai Jiao Tong University, Shanghai 200240, China

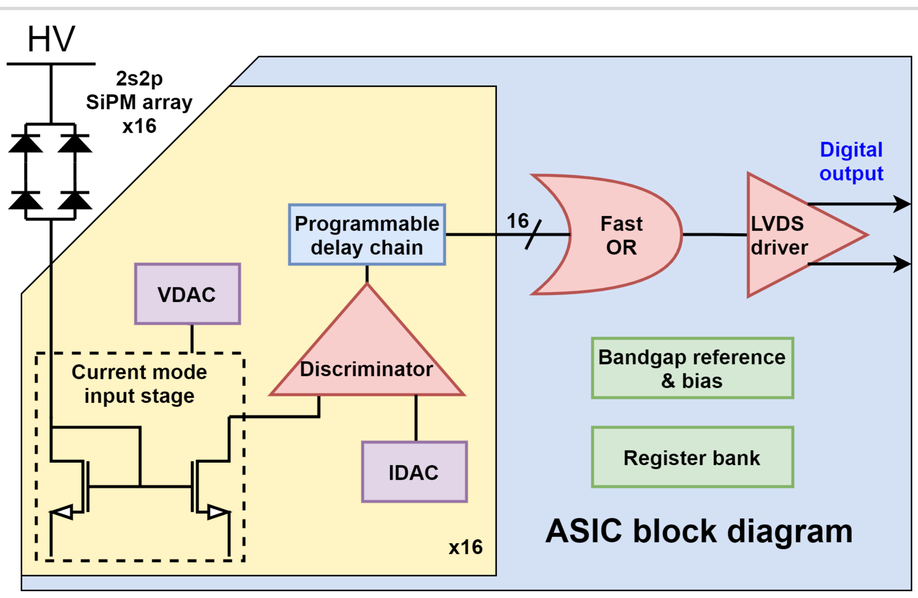
Abstract

TRopIcal DEep-sea Neutrino Telescope (TRIDENT) [1] features the hybrid digital optical module (hDOM) as the detector unit. The hDOM integrates large-area silicon photomultiplier (SiPM) arrays combined with photomultiplier tubes (PMTs) to enhance photon detection efficiency and timing capability, which is crucial for improving the angular resolution of TRIDENT. We are developing a 16-channel fast-timing application-specific integrated circuit (ASIC) for high-precision time measurements to cope with the large input capacitor. In the first version of the prototype ASIC, we designed and compared four different architectures [2]. We ultimately chose the most appropriate front-end circuit, which consisted of a negative feedback common gate stage (NFBCG) and a current discriminator. The outputs of 16 discriminators are merged into one channel by fast OR gates and then transmitted to the off-chip time-to-digital converter. The latency inconsistency between channels is reduced by programmable delay chains. The post-simulation shows that the timing jitter of 16 channels combined with 64 $3 \times 3\ mm^2$ SiPMs is around 500 ps with a single photo-electron signal input. The total power consumption is about 60 mW, which is three times lower than that of the non-ASIC solution.

Conceptual design of an hDOM [3]



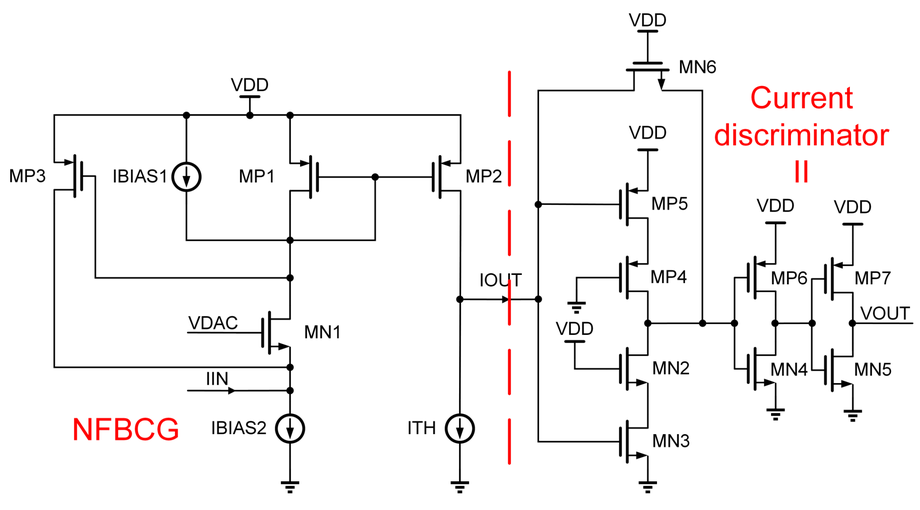
The functional block diagram of the ASIC



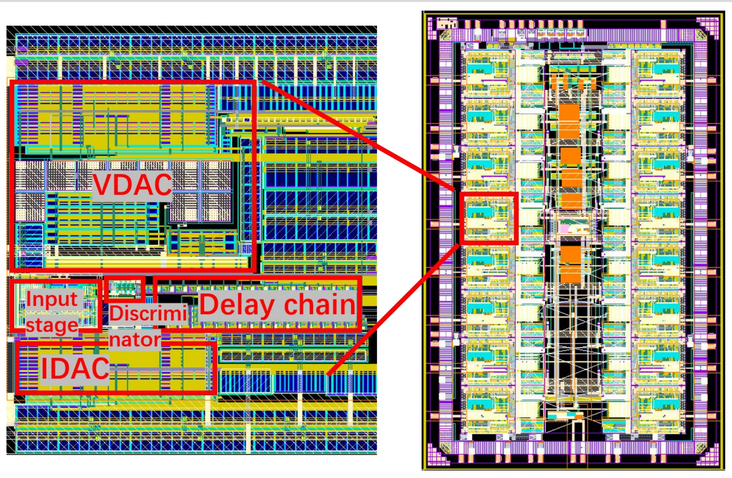
Parameter	Specification
Input impedance	≤ 50 Ω
Input connection	Connecting the anode of a 2s2p SiPM array*
Anode voltage control per channel	About 1 V dynamic range adjustment
Timing jitter	≤ 500 ps FWHM
Power consumption	≤ 10 mW/channel

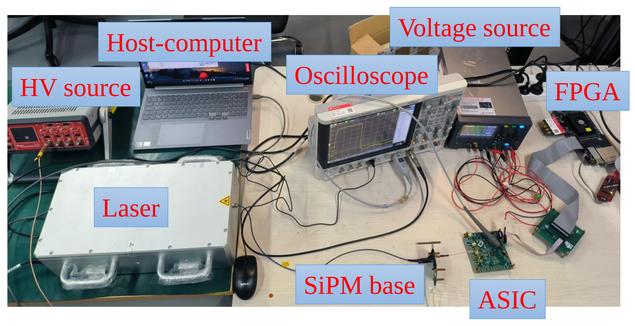
* 2s2p is a configuration with two S13360-3050PE in series and two series in parallel.

The schematic of core modules of the timing channel



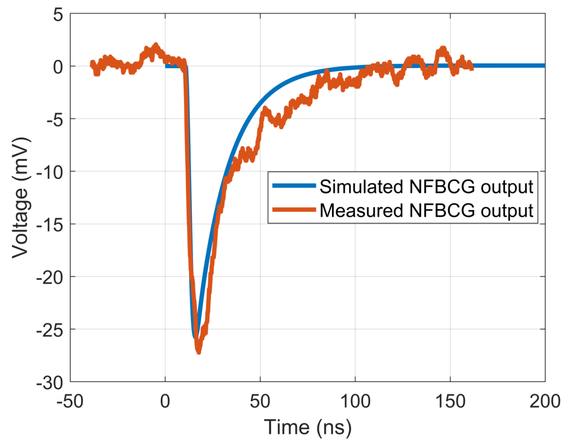
Layout & setup



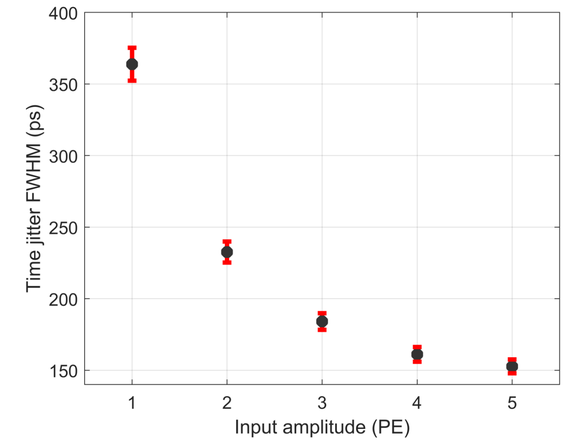


Left: layout of the 16-channel ASIC with a dimension of 2749 $\mu m \times 4200\ \mu m$.
Right: test setup for the prototype ASIC.

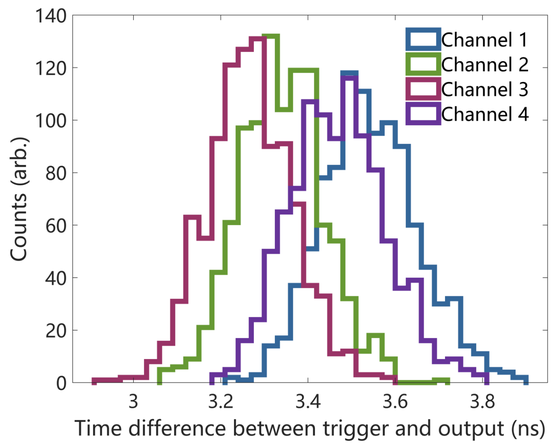
Performance



Simulated and measured SPE waveforms of the input stage readout with an S13360-3050PE SiPM, where the over-voltage of the SiPM is 4 V.

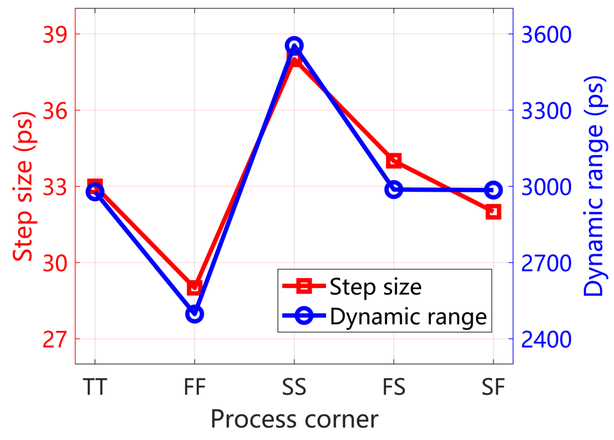


The measured electronic jitter of a timing channel with a 2s2p SiPM array.



Channel No.	1	2	3	4
Time jitter FWHM (ps)	257	224	229	253
Timing offset (ps)	275	73	0	202

The measured ToA distribution of four timing channels in the prototype ASIC.



The post-simulation result of the two-stage delay chain.

- Coarse delay chain: logic gates
- Fine delay chain: capacitor interpolation

To mitigate latency inconsistencies between channels.

Conclusion

We have designed a 16-channel fast-timing ASIC for TRIDENT large-area SiPM arrays readout. Based on the post-simulation results and the test results of the prototype ASICs, the timing jitter of this ASIC with 64 $3 \times 3\ mm^2$ SiPMs is expected to be around 500 ps. The total power consumption of the ASIC, obtained through the post-simulation, is 57.75 mW, which is three times lower than that of the non-ASIC solution [4]. The ASIC was scheduled for tape-out in June 2025. The corresponding tests will be conducted in the second half of 2025.

[1] Ye Z.P. et al. "*A multi-cubic-kilometre neutrino telescope in the western Pacific Ocean*", Nature Astronomy, 7 (2023) 1497. [2] M.X. Wang et al. "*Exploration of optimized front-end readout circuit for time measurement of large-area SiPM arrays*", arXiv:2502.02999 (2025). [3] Fan Hu et al. "*Exploring a PMT + SiPM hybrid optical module for next generation neutrino telescopes*", PoS ICRC2021, 1043. [4] Wei Zhi and Weihao Wu, these proceedings, PoS ICRC2025, 1055.