SLAC xTCA Program

2nd xTCA Interest Group Meeting
CERN

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March 7, 2011
TOPICS

1. PICMG Specifications Development Status
2. ILC Standards R&D Program
3. RF and Controls Upgrade Developments
1. PICMG Specifications Development

• Three Technical Subcommittees
  – Coordinating Committee
  – Hardware WG (I/O, Timing & Synchronization)
  – Software WG (Software and Protocols)
1. PICMG Specifications Development

• HWG Main Activities
  – Specification for interface to ATCA RTM (PICMG3.8) (Done, out for PICMG-wide vote)
  – Specification for double-wide MicroTCA with IO and Timing (MTCA.4) (Done, Committee vote March 8, 2011)
  – Clock & Timing Protocol for ATCA backplane
1. PICMG Specifications Development

• Software WG Main Activities
  – Aimed at Guidelines, not Specifications
  – Aimed at high level interoperability of modules developed in labs and industry
  – Developed comprehensive Roadmap
  – Progress slow due to lack of people and targeted projects to provide focus
Software & Protocols Roadmap

Existing Working Groups and Status

• Data Transport Protocol
  – Initial Protocol set selected and under evaluation
• Synchronization Protocol
  – Pending final hardware distribution scheme
• Command/Control Protocol
  – At discussion/proposal stage
• Component Management/Failover/Update
  – At discussion/proposal stage
• Common Hardware API
  – Technical proposal accepted in principle; guideline in work
• Common Process/Thread Model
  – Technical proposal accepted in principle; guideline in work
• Common I/O Device Model
  – Technical proposal accepted in principle; guideline in work
• Common Communication Model
  – Combined with Common I/O Device Model
1. PICMG Specifications Development

**AdvancedTCA®**

PICMG® 3.8  
R1.0 D0.7j

AdvancedTCA Rear Transition Module  
Zone 3A

3 February 2011

**Open Modular Computing Specifications**

**xTCA™**

PICMG® Specification MTCA.4  
R 1.0 Draft 0.9w

Enhancements for Rear I/O and Precision Timing

21 January 2011

**Open Modular Computing Specifications**
1. PICMG Specifications Development

- ARTM Module: PICMG3.8
- Features Added
  - Alignment/Keying
  - Power & System Management
  - User Data I/O
E.g. RTM Usage: Generic MPP Module

Generic Massively Parallel Processor & Hub Switcher 0.5 Tb/s Throughput System
10 Gbps Channels — Courtesy M. Huffer, SLAC (See also IPFN Lisbon Poster)
ATCA Timing over Fabric on Hub Slots

• Use current backplanes – compatibility with PICMG 3.x.
• Timing signals from hub are not bussed and are bidirectional.
  – The Hub can route any timing signal from any node card
• Can be used on dual-dual star and full-mesh.
• Support the ‘multicast’ ‘binary state timing’ (BST) signals.
  – Distribution of clock, trigger and gate type signals
  – BST1, BST2, BST3 diff pairs proposed.
• Support the ‘multicast’ of ‘encoded event and timing’ (EET) signals.
  – One EET diff pair proposed.
  – This signal contains a carrier clock and carries deterministic timing messages allowing clock skew correction, absolute time setting and trigger transport.

-J. Sousa, IPFN Lisbon 2010 xTCA Workshop

• HWG Project: Document Proposal as PICMG Guideline
1. PICMG Specifications Development

AMC & µRTM Modules – MTCA.4

Keying
User I/O
Power System Mgmt
Standard AMC Connector and Backplane

AMC
µRTM
MTCA.4 Prototypes: 6-Payload Shelf

- Development Shelf 6-Slot
- Physics Backplane
- Non-Redundant MCH, Fans, Power Module

Front Panels

µRTM RTM I/O Connector

Rear I/O Panels

2 µRTM RTM

2-wide AMC

Backplane Edge Connector

Courtesy K. Rehlich DESY & Schroff GMBH
MTCA.4 12-Slot Shelf & Modules

12 Slot Crate & Front-Rear Fan Tray (Schroff)

6 Slot Crate w/ AMC & RTM (Schroff)

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2. ILC Standards R&D Program

• Goals
  – Develop xTCA infrastructure for lab programs
  – Develop Reference Designs for Modules
  – Develop IPMI & N+1 Software Support
  – *Develop Industry Support for Generic Apps*

• Target Test Applications
  – FY11: 10MW L-Band klystron interlocks
  – FY12: 10MW L-Band LLRF demonstration
MTCA.4 Infrastructure Development Platform

- SLAC Linac controls upgrade
- 6-Slot Prototype Shelf w/ MCH, Processor, Interim Timing System, power module, built-in fans
- PMC Event Receiver (EVR) on double MTCA Adapter
- Shelf non-redundant
- All rear I/O access
MTCA Backplane Timing Distribution

- 2 radial clocks per AMC, low jitter
- 8 bussed lines, M-LVDS for Clocks, triggers, interlocks

Central Timing

ENC Clock
Trigger

AMC Timing

ENC Clock
Trigger

AMC ADC

Interlock

AMC ADC

Interlock

MCH
Cross Point Switch

Backplane

- K. Rehlich, DESY

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Timing Tx-Rx Module – Stockholm U.

- Fiber optic links w/ drift compensation
- ps stability
- AMC module is receiver and transmitter
- Clock, trigger and event distribution
- New design for Rx-only MTCA.4 version starting for SLAC requirements (Mico-Research EVR Compatible)
MTCA.4 Engineering Reference Design

- Double-wide plus RTM provides excellent analog space, ground noise control, crosstalk
- AMC space fully backward compatible with industry single-wide designs

- Reference Design complete w/ supporting FW-SW environment enables engineers to focus on payload design w/ power, IPMI basic infrastructure standardized

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MTCA RF Infrastructure, ADC-DAC, RTM

Courtesy R. Akre
3. LLRF and Controls Upgrade Projects

- RF Upgrade demo unit funded, completion due end FY11
  - MTCA.4 used for processor, ADC-DAC, IPMI to peripheral RF, interlock chassis

- Controls Upgrade Sector Node demo unit
  - Proposed, under review to optimize conversion
  - Funding restrictions require phased approach to CAMAC replacement
  - Initial target BPM & Similar diagnostics
  - Same ADC-DAC as for LLRF, new RTM
Planned RF Chassis & RTM

RF Chassis

RF Frequency Generation

119MHz Clock

119MHz Clock

2856MHz Ref

2856MHz Ref

2830.5MHz LO

2856MHz Ref

119MHz CLK

Diode Out

2856MHz In

RF Up Converter

RF Signal

Down Mixing

Local Oscillator

RF Reference

RF Ref Monitor

LO 2830.5MHz

KLY Out

ACC RF

ACC Beam

KLY BV

KLY BV

Klystron Beam V

Klystron Drive

SLED Output

Accelerator Out

Klystron Out

LO Monitor

Clock Monitor

RF Ref Monitor

2856MHz Ref

2856MHz In

119MHz Clock

LO Distribution

Klystron Beam Voltage Processing

Klystron Beam

Klystron Out

RF Chassis

LO Monitor

Clock Monitor

RF Ref Monitor

2856MHz Ref

RF Out to SSSB

Klystron Drive

SLED Output

Accelerator Out

Klystron Out

KLY BV

KLY BV

I

Q

RF Out

Drive

SLED

ACC RF

ACC Beam

KLY Out

AC Power

TRIG

AC Power

TRIG

DACs

ADCs

LO Monitor

Clock

RF Ref Monitor

2856MHz Ref

2830.5MHz LO

2856MHz Ref

119MHz CLK

Diode Out

2856MHz In

RF Up Converter

RF Signal

Down Mixing

Local Oscillator

RF Reference

RF Ref Monitor

LO 2830.5MHz

KLY Out

ACC RF

ACC Beam

KLY BV

KLY BV

I

Q

RF Out

Drive

SLED

ACC RF

ACC Beam

KLY Out

AC Power

TRIG

AC Power

TRIG

DACs

ADCs

To/from

MTCA.4

ADC-DAC

Courtesy R. Akre
Test Station BD – RF & Accelerator

MAIN DRIVE LINE

SYNC CLOCKS & LO GENERATION

KLYSTRON SLED WAVEGUIDE

MODULATOR

40ft ACCEL.SECTION INSTRUMENTS & CNTRLS

Protection Interlocks

DOWN-CONVERTER RF->IF

MKSU II

MTCA CHASSIS INFRASTRUCTURE & MODULES

BPMs Toroids Wire Scan Profile Mon. Vacuum Power Supplies BCS Temperature

MTCA.4

SLAC
NATIONAL ACCELERATOR LABORATORY
Station Crate Layout (Typ.)

Infrastructure
Pwr, MCH, IOC, Timing

RF Fdbk

Controls Modules (Typ.)

Redundant MCH, Pwr Options

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Note – All I/O in Rear; both AMC, RTM Hot Swappable
Upgraded Station Rack Profile

AC POWER PANEL

MTCA CONTROLS

HEAT EXCHANGER

CROSS-CONNECT

RF GENERATION & DOWNMIX

MKSUII

SOLENOID POWER SUPPLY

CONTROLS IN-OUT

RF IN-OUT

PLUG-IN COOLING UNIT (BOTTOM IN – TOP OUT)

PLUG-IN COOLING UNIT (FRONT IN – TOP OUT)
In-Rack Crate Enclosure

RF GENERATION & DOWNMIX
MKSUII
SOLENOID POWER SUPPLY

SOLENOID POWER SUPPLY

RF CABLES TO/FROM TRAYS
REAR I/O CABLES TO/FROM RTM’S
WATER COOLED ENCLOSURE
CABLES TO/FROM TUNNEL
PENETRATION
• FPGA Based interlocks on-board
• Cables interface to existing plant
• Self-contained, delivers fault trips to modulator
• Communicates to MTCA.4 control processor by Ethernet

Courtesy S. Zheng & J. Olsen
Design & Industrial Support Goals

- Work with Industry to provide key generic FPGA AMC modules
  - Develop 2 or more sources
  - Encourage multiple lab-supported specifications

- AMC 1
  - FAST ADC
  - 4 CH 16 BIT 119 MSPS (180 MSPS MAX)

- RTM 1
  - STRIPLINE BPM (2 TYPES)
  - SIGNAL CONDITIONING, FILTERING & CALIBRATION

- RTM 2
  - TOROID (2 TYPES)
  - SIGNAL CONDITIONING & CALIBRATION

- RTM 2 GATED ADC SIGNAL CONDITIONING (GADC)

(Struck, Vadatech)

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Beamline Instruments via IP Adapter

RTM 4
BLEN BROFILE MONITOR
GENERIC 3 IP 1/0
ADAPTER, SCSI PORT,
IPMI PASSTHOUGH

AMC 3
3-INDUSTRY PACK (IP)
ADAPTER FOR PHYSICS
BACKPLANE

1-3 
INDUSTRY 
PACKS

RTM 4
VACUUM GUAGE
READOUT, REMOTE
WAKEUP

RTM 4
VAC-I-ION PUMP
CONTROLLER
INTERFACE

RTM 4
WIRE SCANNER MOVERS
HYTEK IP DESIGN
PORT FW, SW FROM
XSTG DESIGN

(TEWS, 
Vadatech)

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LLRF System, Feedback Apps

AMC 2
FAST ADC
10 CH 16 BIT 119 MSPS
2 CH DAC 238 MSPS

2 CH DAC 238 MSPS

RF FREQUENCY GENERATION
LOCAL OSCILLATOR (LO)
SAMPLING CLOCKS

2856 MHZ REF IN

IF SIGS
DAC OUT

RTM-3
25 MHZ IF SIGNAL PASSTHROUGH
DAC OUTPUT TO RF AMP

I/O CNTRL

RTM-3
GENERIC FAST
SIGNAL CONDITIONING UP TO 10
CH ANALOG IN, 2 CH DAC OUT

(Struck, Vadatech)

IF SIGS
DAC OUT

RTM-3

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Conclusions 1

• Standards
  – HWG completed specs
    • MTCA.4, submitted to PICMG, comments due March 4th
    • PICMG3.8, Committee vote March 8th, send to PICMG for approval (~3 mo process)
    • Started work on ATCA fabric timing Guideline
  – SWG roadmap in progress
    • No work for past 2 months, limited personnel, need new members involved in relevant apps
Conclusions 2

• Infrastructure
  – Operational on 6-slot including EVR timing on PMC adapter; IPMI for MTCA.4 progressing
  – 6 & 12 slot crates hand
  – Timing module in hand; new Rx unit starting design (Stockholm); vendor development planned

• Test stand Demos
  – FPGA Interlocks on industry FPGA, in-house RTM underway for FY 11
  – RF demo planned FY 12
Conclusions 3

• RF and Controls Upgrades using MTCA.4
  – RF approved for demo station, due end FY11
  – Controls proposal for scaled down demo to include BPMs, conversion plan for later additions underway
  – Common shared platform based in MTCA.4 is ultimate goal to optimize cost performance
Acknowledgments

• The entire SLAC program is enabled by:
  – PICMG HWG and SWG leaders and members
  – LLRF and Controls teams at SLAC
  – Collaboration with Lab partners especially DESY XFEL project personnel
  – Industry support especially Schroff, ELMA, TEWS, Struck, Kontron, NAT, PT and Vadatech
  – Interest of broader lab community especially PICMG members CERN, DESY, FNAL, IHEP, IPFN and ITER, and University of Stockholm