CMOS SPAD

M. Nicola Mazziotta
mazziotta@ba.infn.it
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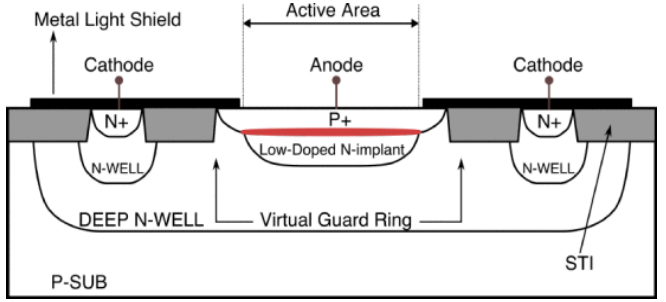
Introduction

- The increasing requirements for sub-mm/mm photon sensor cells made of array of single photon avalanche diodes (SPAD) with low time jitter imply higher levels of integration
- Standard CMOS processes provide a mature and reliable technology, which allows the co-integration of SPADs and electronics at low costs
- Advantages of CMOS SPADs are:
  - Light detection and readout on a single chip (simple mechanics, lower cost suitable for mass production)
  - Active pixel quenching
  - Each SPAD can read out individual cells and bad SPADs can be turned off to reduce overall noise (trade-off between active area and noise)
  - Back-side illumination possible
  - Timing resolution < 100 ps
  - Fast tracker devices
- CMOS SPAD developments for high-energy physics could find applications for large instrumented surfaces highly segmented (e.g., RICH)
- The aim of this talk is not to review the status of art of CMOS-SPADs, but to trigger a discussion toward a possible new development of CMOS-SPADs in the contest of DRD4
  - I am just presenting a few of examples
    - My personal selection, apologies for not mentioning many other interesting works

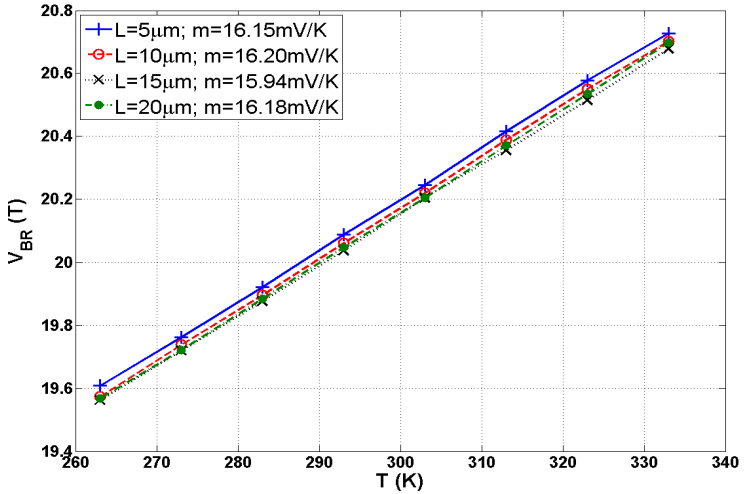
FBK CMOS-SPAD in 110 nm process node

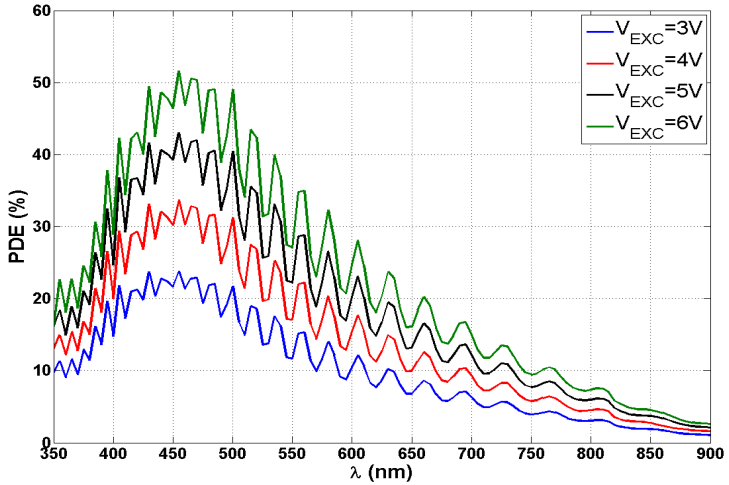
- CMOS Image Sensor (CIS) technologies used to design Single Photon Avalanche Diodes (SPADs)
  - SPAD integrated in the LFoundry CMOS process design kits (PDK) in 150/110 nm nodes
- Active area defined by the side length (L) of the high electric field region
  - L is few tens of microns
- Breakdown voltage of about 20 Volt
- Photon Detection Efficiency (PDE) peak around 450 nm
- Timing resolution of about 86-99 ps FWHM @ 468 nm

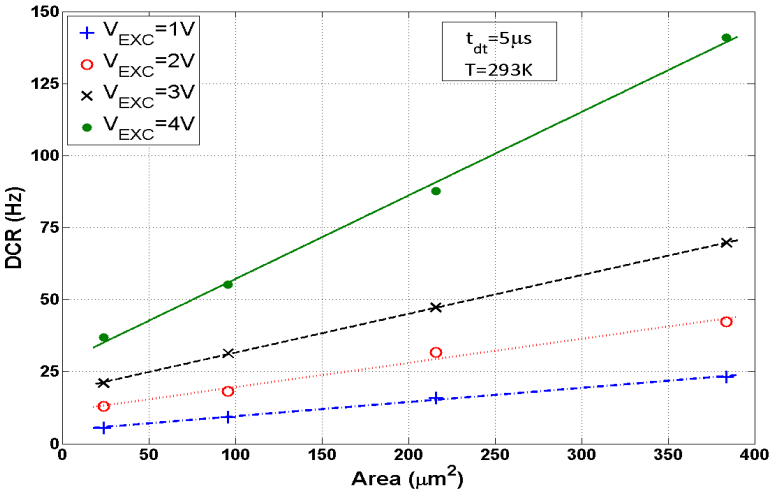


Cross-section of a p+/n-implant SPAD implemented in a 110 nm CIS technology with virtual deep n-well guard ring. The avalanche region is highlighted in red.

	Timing Resolution (ps); @V_{EXC}=4V	
	Laser λ: 468nm	Laser λ: 831nm
L=5μm	86.5	69
L=10μm	90	71
L=15μm	97.5	76
L=20μm	99	80



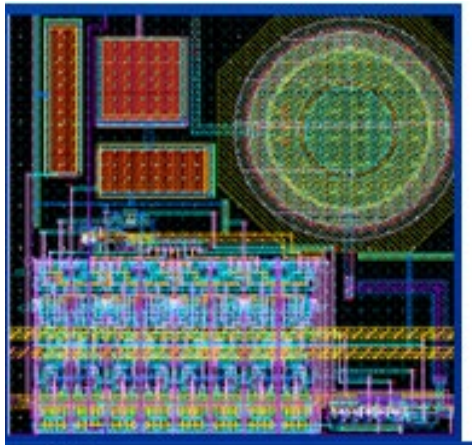


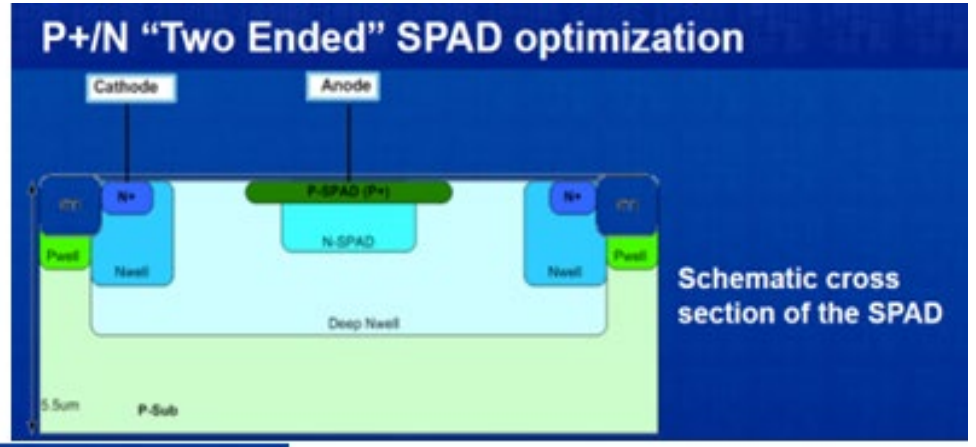


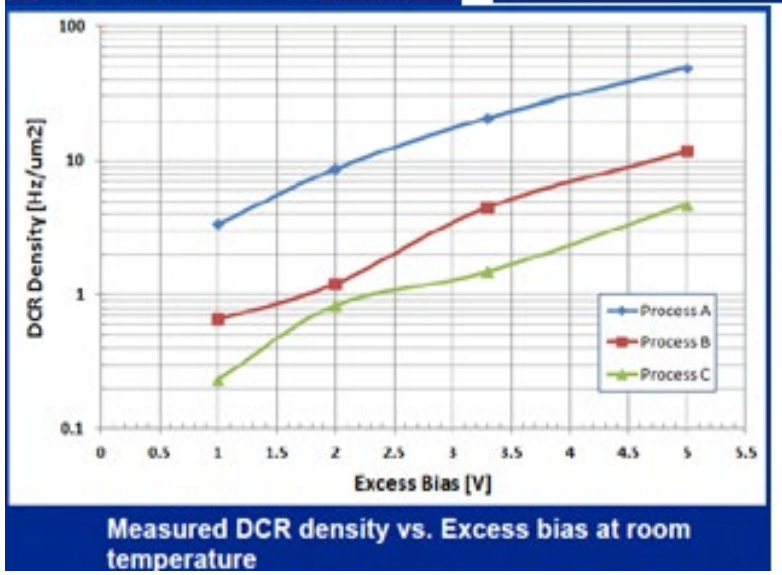
https://ieeexplore.ieee.org/document/8486883

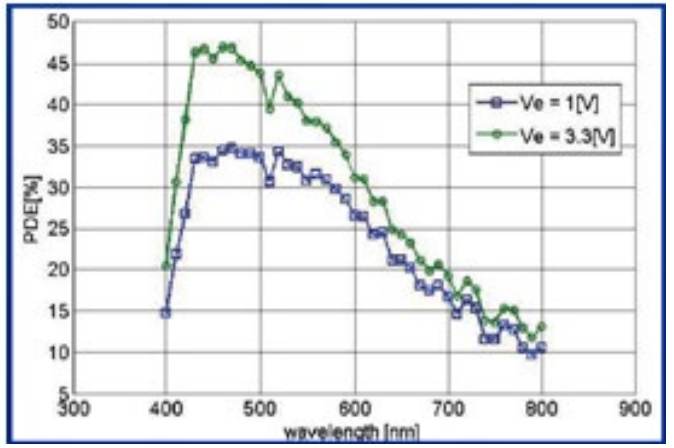
Tower Jazz (TOWER Semiconductor) SPAD technology

- Technology: 180 nm CMOS (1.8V/3.3V or 1.8V/ 5.0V) and CIS state of the art pixels
- Breakdown voltages: 12 V, 14 V and 20 V
- PDE peak around 450 nm







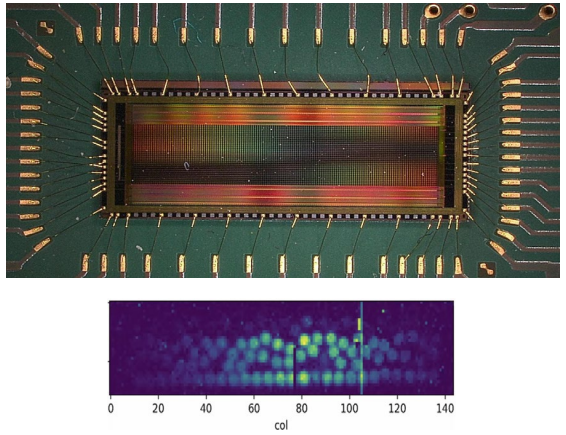


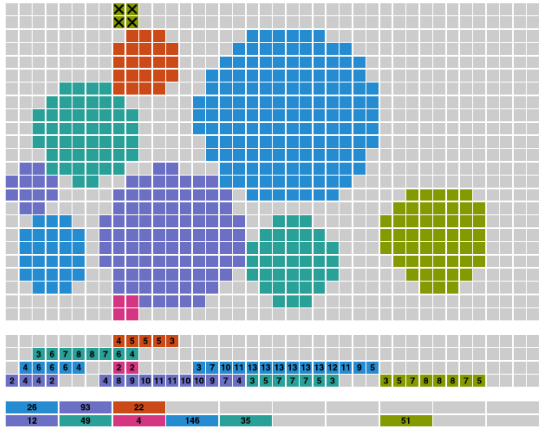
Dr. Amos Fenigstein, TowerJazz February, 2018 https://imagesensors.org/wp-content/uploads/2019/05/Amos_Fenigstein.pdf

CMOS SPAD for the readout of scintillating fibers

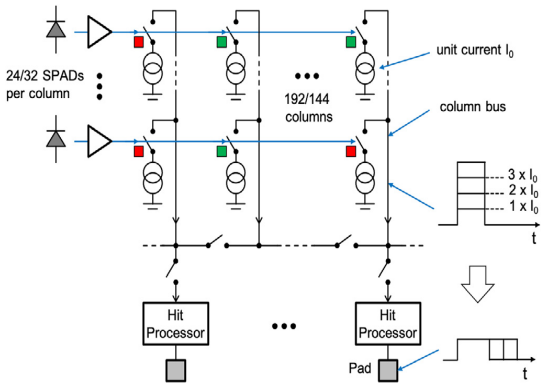
- Detection of light from optical fibers for particle fiber trackers
- SPAD pitches of 42/56 µm to accommodate large or small fibers
  - 350 nm CMOS technology with 4 metal layers (IMS in Duisburg, Germany)
- Each SPAD can be associated to a group by enabling a programmable switches
  - The total current is $N \times I_0$ when N (enabled) SPADs have fired and I_0 the unit current

Sensitive area: 8064 × 1792 µm2
Pixel size: 56 x 56 µm2

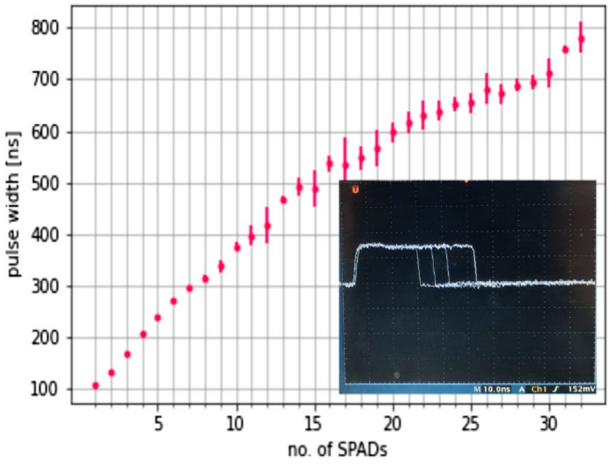


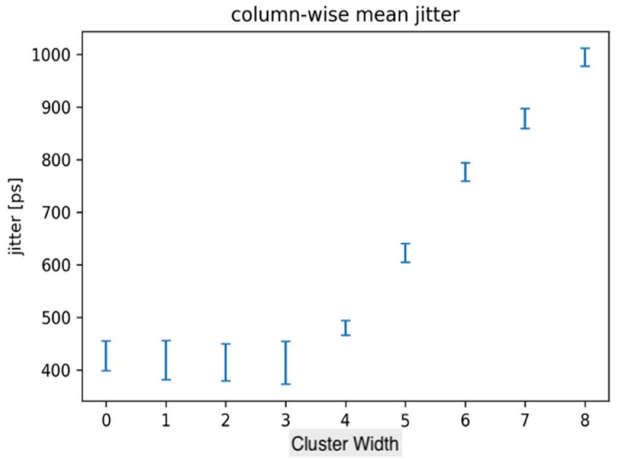


Example of SPAD groupings and limitation of the architecture



Principle of SPAD counting in a column group.





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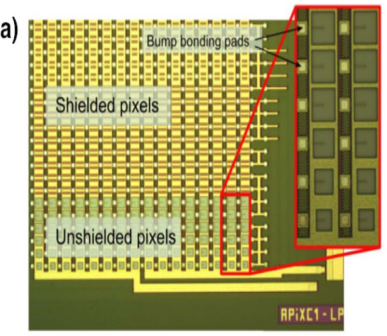
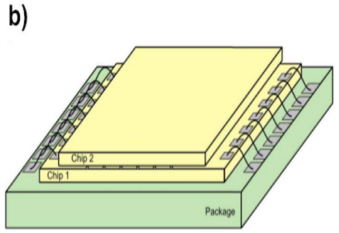
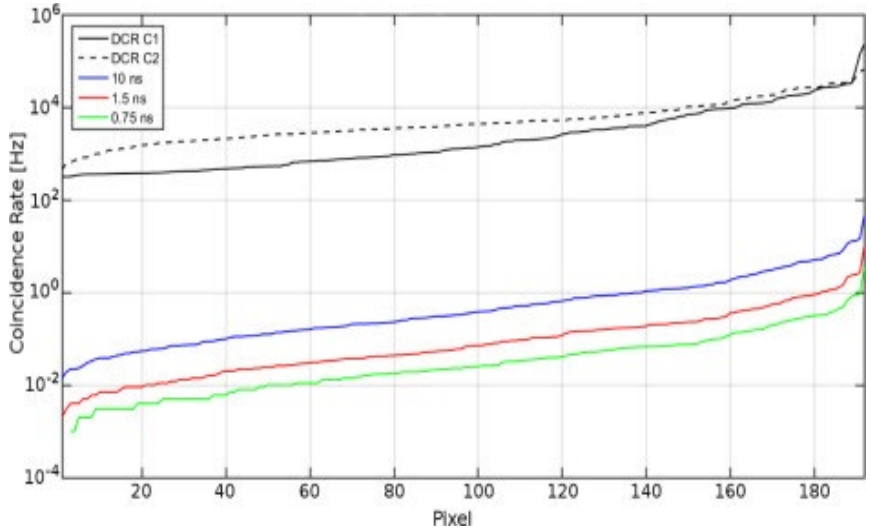
Avalanche Pixel Sensor for tracking applications

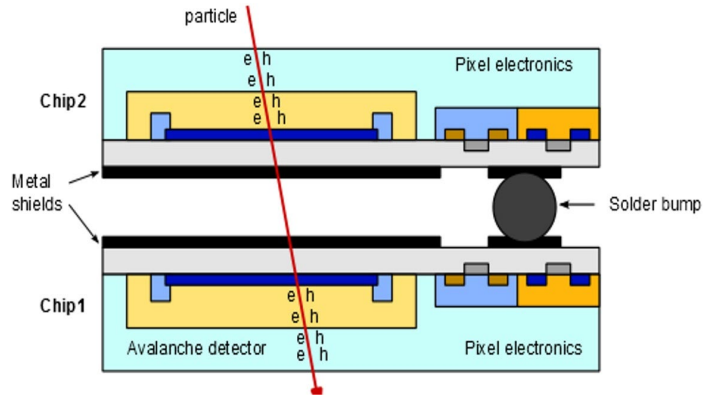
- A position-sensitive detector based on the vertical integration of pairs of aligned pixels operating in Geiger-mode regime and designed for charged particle detection
  - This device exploits the coincidence between two simultaneous avalanche events to discriminate between particle-triggered detections and dark counts
  - A proof-of-principle prototype was designed and fabricated in a 150 nm CMOS process and vertically integrated through bump bonding

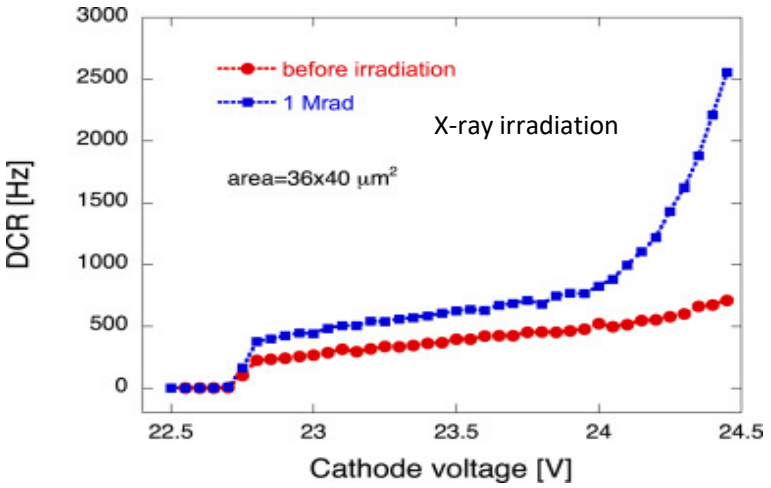






Cumulative DCR is plotted as a function of the number of pixels included in the sum, as measured separately in each chip and in coincidence





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Further works and references (selection)

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- P. Brog et al. “APiX, a two-tier avalanche pixel sensor for digital charged particle detection” NIM A 958 (2020) 162546
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- M. Musacci et al. “Radiation tolerance characterization of Geiger-mode CMOS avalanche diodes for a dual-layer particle detector” NIM A936, pp. 695-696, 2019.
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- E. Manuzzato et al., "A 16×8 Digital-SiPM Array With Distributed Trigger Generator for Low SNR Particle Tracking," in IEEE Solid-State Circuits Letters, vol. 2, no. 9, pp. 75-78, Sept. 2019
- A. Ficorella et al. “Crosstalk Characterization of a Two-tier Pixelated Avalanche Sensor for Charged Particle Detection”,IEEE Journal of Selected Topics in Quantum Electronics, vol. 24, no. 2, pp. 1-8, March-April 2018
- M. Moreno-García, H. Xu, L. Gasparini and M. Perenzoni, "Low-Noise Single Photon Avalanche Diodes in a 110nm CIS Technology," 2018 48th European Solid-State Device Research Conference (ESSDERC), Dresden, Germany, 2018, pp. 94-97
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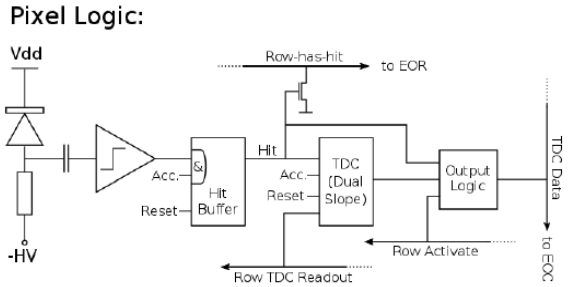
- L. H. C. Braga et al., "A Fully Digital 8×16 SiPM Array for PET Applications With Per-Pixel TDCs and Real-Time Energy Output," in IEEE Journal of Solid-State Circuits, vol. 49, no. 1, pp. 301-314, Jan. 2014, doi: 10.1109/JSSC.2013.2284351

Conclusions

- Combining SPAD and CMOS readout electronics on a single chip with tailor-made readout architectures can provide digitized output signals with low power consumption
  - By combining detection and processing, systems get greatly simplified and cheaper
  - New development of CMOS-SPAD could also be of interest of other DRDs
- Timeline: 3-5 years (depending on the application)
- Possible working plan:
  - SPAD optimization (if needed), starting from the current CIS SPAD
  - Analog blocks design
  - Digital blocks design
  - Floor-plan and chip assembly
  - Test and radiation hardness qualification
  - …



https://indico.cern.ch/event/837899/contributions/3570849/attachments/1916472/3168565/Bergen_LW_CMOSSPAD_Talk_MKeller.pdf

Thanks to Francesco Licciulli, Lucio Pancheri, Lodovico Ratti, Leonardo Gasparini for input and discussion

Backup

A Fully Digital 8 x 16 SiPM Array for PET Applications With Per-Pixel TDCs and Real-Time Energy Output

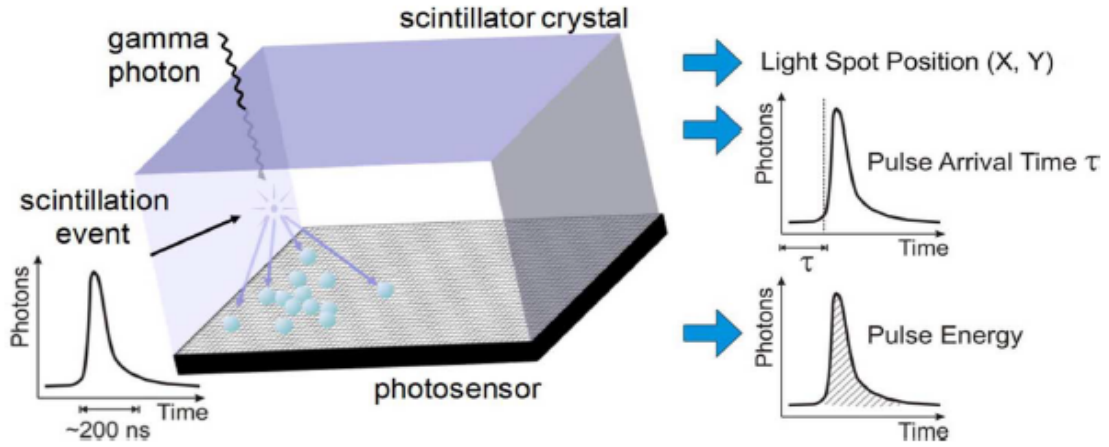


Fig. 2. Scintillation light pulse hitting the photosensor and its respective outputs.

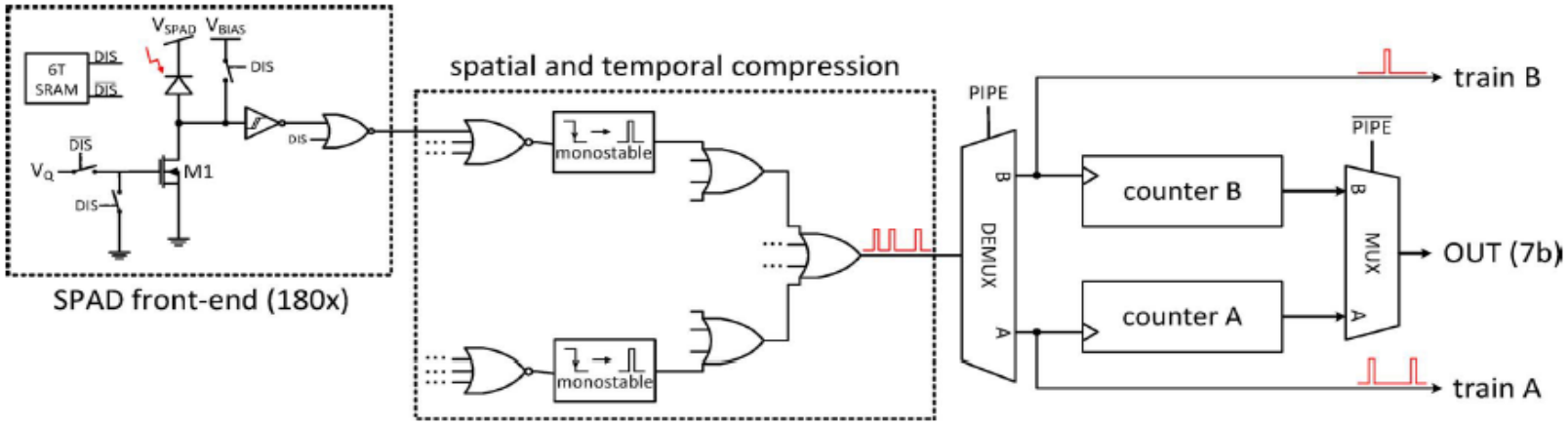


Fig. 3. Mini-SiPM (detector cell) complete schematic.

https://ieeexplore.ieee.org/document/6642135