CMOS SPAD

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Introduction

- The increasing requirements for sub-mm/mm photon sensor cells made of array of single photon avalanche diodes (SPAD) with low time jitter imply higher levels of integration
- Standard CMOS processes provide a mature and reliable technology, which allows the co-integration of SPADs and electronics at low costs
- Advantages of CMOS SPADs are:
  - Light detection and readout on a single chip (simple mechanics, lower cost suitable for mass production)
  - Active pixel quenching
  - Each SPAD can read out individual cells and bad SPADs can be turned off to reduce overall noise (trade-off between active area and noise)
  - Back-side illumination possible
  - Timing resolution < 100 ps
  - Fast tracker devices
- CMOS SPAD developments for high-energy physics could find applications for large instrumented surfaces highly segmented (e.g., RICH)
- The aim of this talk is not to review the status of art of CMOS-SPADs, but to trigger a discussion toward a possible new development of CMOS-SPADs in the contest of DRD4
  - I am just presenting a few of examples
    - My personal selection, apologies for not mentioning many other interesting works
FBK CMOS-SPAD in 110 nm process node

- CMOS Image Sensor (CIS) technologies used to design Single Photon Avalanche Diodes (SPADs)
  - SPAD integrated in the LFoundry CMOS process design kits (PDK) in 150/110 nm nodes
- Active area defined by the side length (L) of the high electric field region
  - L is few tens of microns
- Breakdown voltage of about 20 Volt
- Photon Detection Efficiency (PDE) peak around 450 nm
- Timing resolution of about 86-99 ps FWHM @ 468 nm
Tower Jazz (TOWER Semiconductor) SPAD technology

- Technology: 180 nm CMOS (1.8V/3.3V or 1.8V/5.0V) and CIS state of the art pixels
- Breakdown voltages: 12 V, 14 V and 20 V
- PDE peak around 450 nm
CMOS SPAD for the readout of scintillating fibers

• Detection of light from optical fibers for particle fiber trackers
• SPAD pitches of 42/56 μm to accommodate large or small fibers
  • 350 nm CMOS technology with 4 metal layers (IMS in Duisburg, Germany)
• Each SPAD can be associated to a group by enabling a programmable switches
  • The total current is $N \times I_0$ when $N$ (enabled) SPADs have fired and $I_0$ the unit current

Sensitive area: 8064 × 1792 μm²
Pixel size: 56 x 56 μm²

Example of SPAD groupings and limitation of the architecture

Principle of SPAD counting in a column group.

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Avalanche Pixel Sensor for tracking applications

- A position-sensitive detector based on the vertical integration of pairs of aligned pixels operating in Geiger-mode regime and designed for charged particle detection
  - This device exploits the coincidence between two simultaneous avalanche events to discriminate between particle-triggered detections and dark counts
  - A proof-of-principle prototype was designed and fabricated in a 150 nm CMOS process and vertically integrated through bump bonding

Cumulative DCR is plotted as a function of the number of pixels included in the sum, as measured separately in each chip and in coincidence

https://doi.org/10.3389/fphy.2020.607319
Further works and references (selection)

• G. Torilla et al. “DCR and crosstalk characterization of a bi-layered 24×72 CMOS SPAD array for charged particle detection”, NIM A 1046 (2023) 167693
• P. Fischer, R. K. Zimmermann and B. Maisano “CMOS SPAD sensor chip for the readout of scintillating fibers” NIM A 1040 (2022) 167033
• P. Brog et al. “APIX, a two-tier avalanche pixel sensor for digital charged particle detection” NIM A 958 (2020) 162546
• L. Pancheri “First prototypes of two-tier avalanche pixel sensors for particle detection”, NIM A 845 (2017) 143
• N. D'Ascenzo et al. “Silicon avalanche pixel sensor for high precision tracking” Journal of Instrumentation, 9-, C03027 (2014)
Conclusions

• Combining SPAD and CMOS readout electronics on a single chip with tailor-made readout architectures can provide digitized output signals with low power consumption
  • By combining detection and processing, systems get greatly simplified and cheaper
  • New development of CMOS-SPAD could also be of interest of other DRDs

• Timeline: 3-5 years (depending on the application)

• Possible working plan:
  • SPAD optimization (if needed), starting from the current CIS SPAD
  • Analog blocks design
  • Digital blocks design
  • Floor-plan and chip assembly
  • Test and radiation hardness qualification
  • ...

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Backup
A Fully Digital 8 x 16 SiPM Array for PET Applications With Per-Pixel TDCs and Real-Time Energy Output

Fig. 2. Scintillation light pulse hitting the photosensor and its respective outputs.

Fig. 3. Mini-SiPM (detector cell) complete schematic.