Test and performance of the CMS ECAL barrel data conversion and digital processing ASIC for HL-LHC

Abstract

The demanding requirements of the high luminosity upgrade of LHC (HL-LHC) necessitated a complete redesign of the front-end electronics for the CMS electromagnetic calorimeter (ECAL).

The Very-Front-End cards will incorporate two new ASICs: a fast amplifier (CATIA) and a data conversion and compression ASIC (LiTE-DTU). The CATIA serves as a transimpedance amplifier to read signals from the APD sensors connected to the ECAL crystals. It features two differential outputs with two different gains, $\times 10$ and $\times 1$, to ensure optimal resolution for signals up to 2 TeV. The LiTE-DTU ASIC, designed in a commercial 65 nm CMOS technology, integrates two 12-bit 160 MS/s SAR ADCs to sample the CATIA outputs. A gain selection mechanism and a lossless data compression algorithm enable data transmission using a single 1.28 Gb/s serializer. An on-chip PLL generates a low-jitter 1.28 GHz clock required by the ADCs and by the serializer. This upgrade will guarantee high-precision energy measurements for the HL-LHC phase: the improved time resolution of approximately 30 ps for photons and electrons above 50 GeV addresses the increased event pileup and enhances the rejection of spike signals, anomalous signals resulting from direct APD interactions.

The LiTE-DTU ASIC has undergone extensive testing in both laboratory and beam tests, demonstrating excellent performance in the pre-production version. An ADC effective number of bits (ENOB) of 9.4 was measured at a 50 MHz input frequency using the internal PLL clock, slightly lower than the design value of 10.2. However, measurements using an external clock source yielded an ENOB of 10.2, suggesting that the degradation was due to PLL clock jitter. While the overall performance already meets system requirements, efforts will be made to improve the PLL clock jitter in the next version of the ASIC.

Radiation tests were conducted to evaluate the LiTE-DTU's tolerance to total ionizing dose (TID) damage using 10-keV X-rays up to 50 kGy, showing no performance variation in the ASIC after irradiation. The LiTE-DTU was also tested for single event upsets (SEU) tolerance, revealing a measured cross-section of approximately $6.8 \times 10^{-18}\,\mathrm{cm}^2$/bit for the I2C registers, protected by TMR, and $9.4 \times 10^{-13}\,\mathrm{cm}^2$/chip for the unprotected data path. These results surpass the requirements for the CMS experiment.

A total of 600 pre-production dies was delivered. They were used to equip a 400-channel spare ECAL module for large-scale integration tests, stability tests and beam tests. These chips underwent testing and validation using an automated procedure and the achieved a yield of approximately 97%. The test setup consists of a test board with a ZIF socket, a commercial FPGA board, a low-jitter clock generator, and arbitrary waveform generators. All modules were remotely controlled through a custom DAQ test interface written in Python. This system will be integrated into the automatic test equipment for the testing and validation of the LiTE-DTU mass production, expected to deliver approximately 100k chips by the beginning of 2024.