Test and Performance of the CMS ECAL Barrel Data Conversion and Digital Processing ASIC for HL-LHC
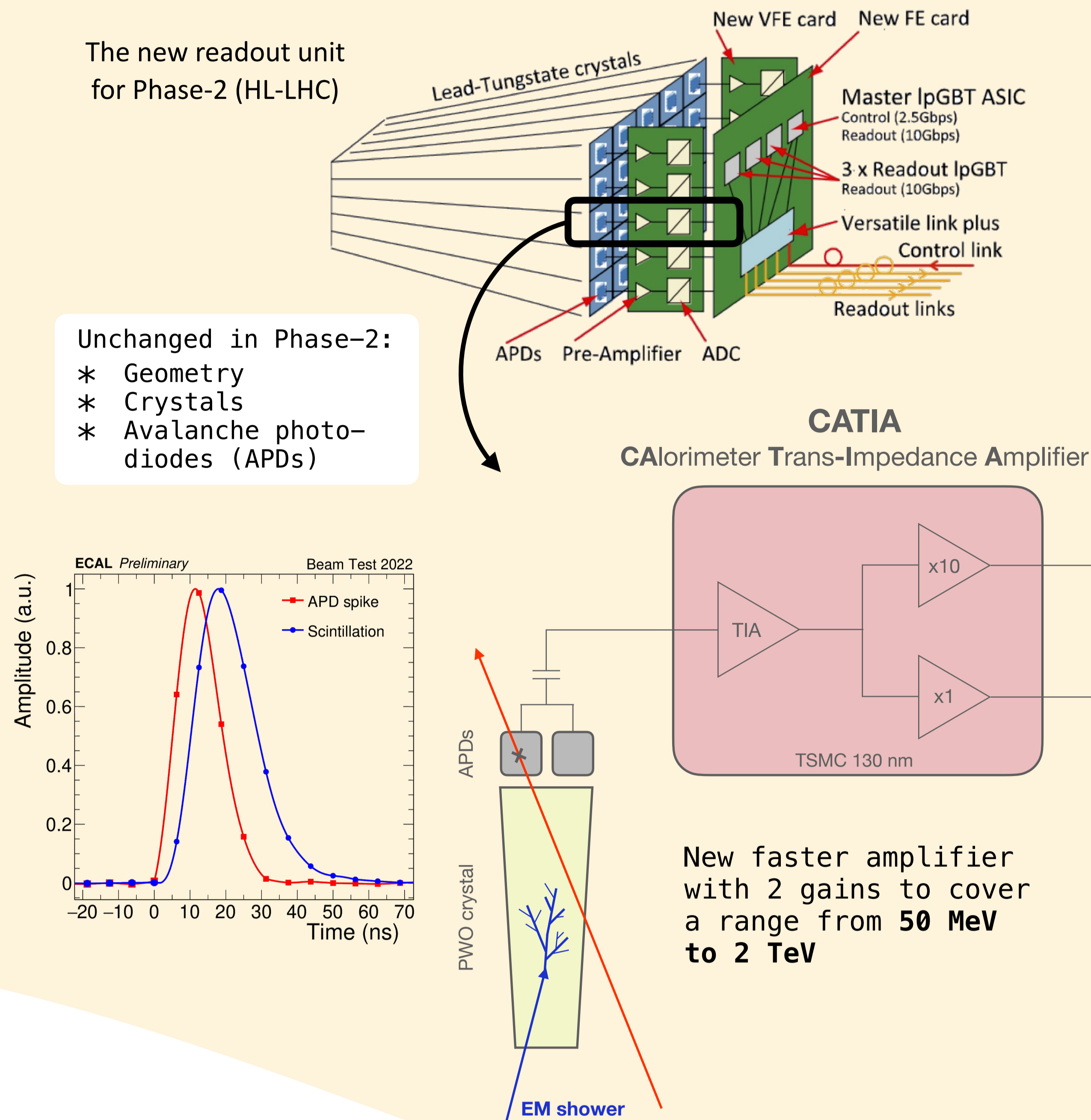
25-29 September 2023, Siena (Italy)

Context and front-end upgrade

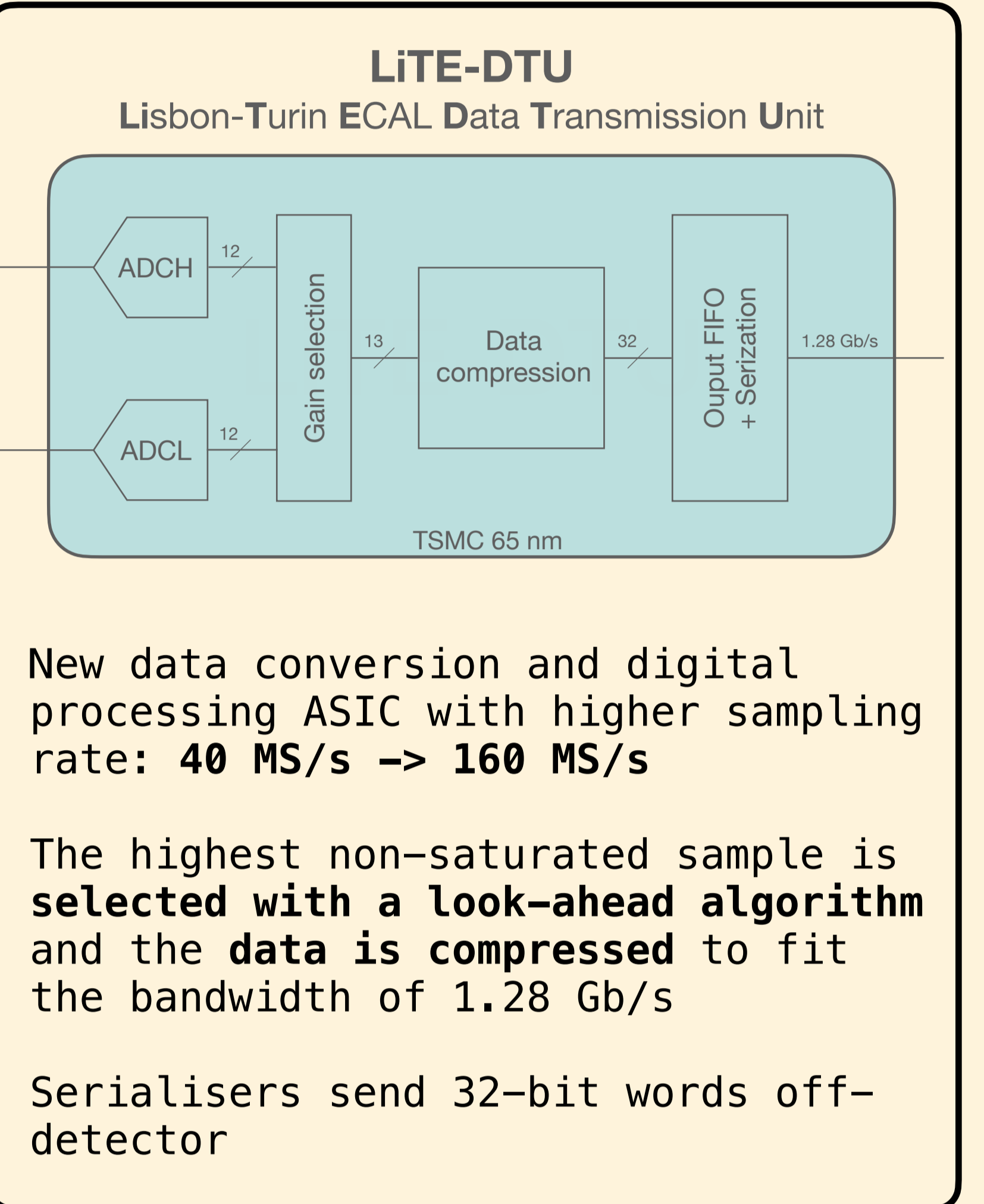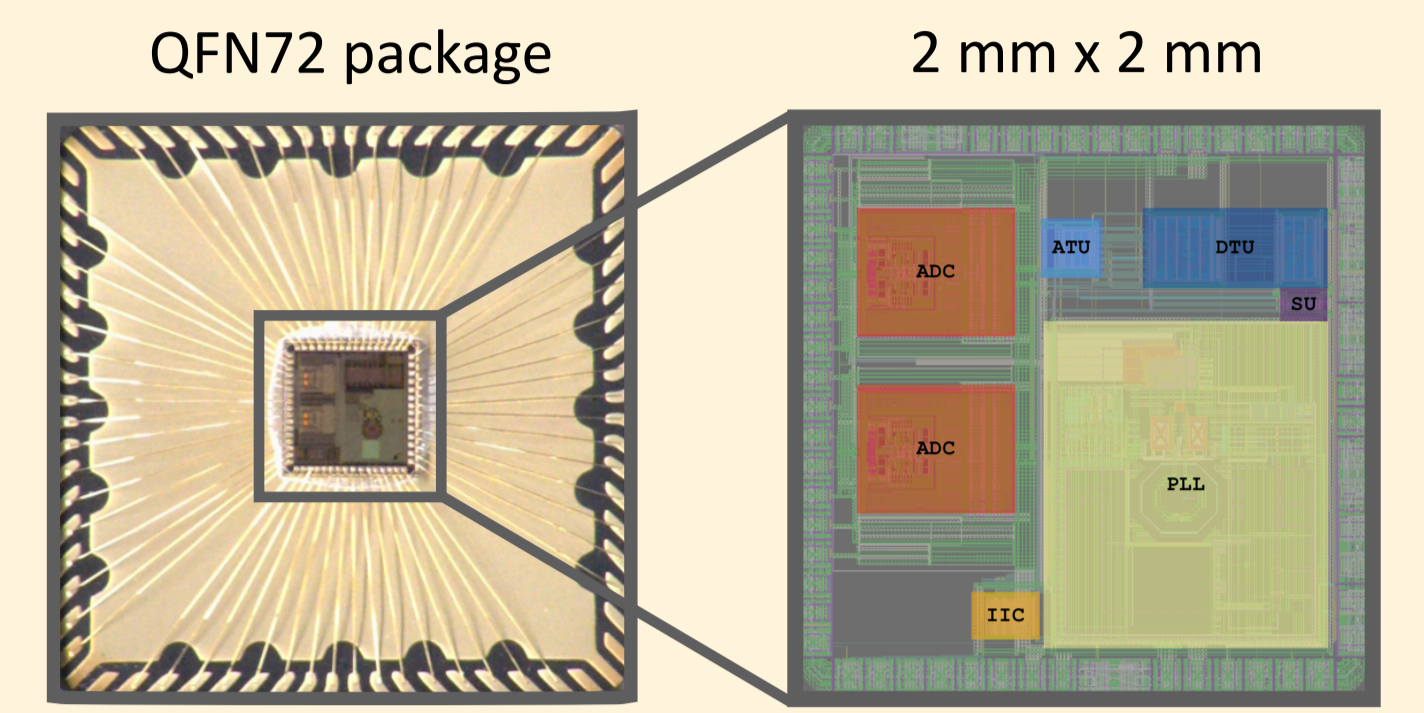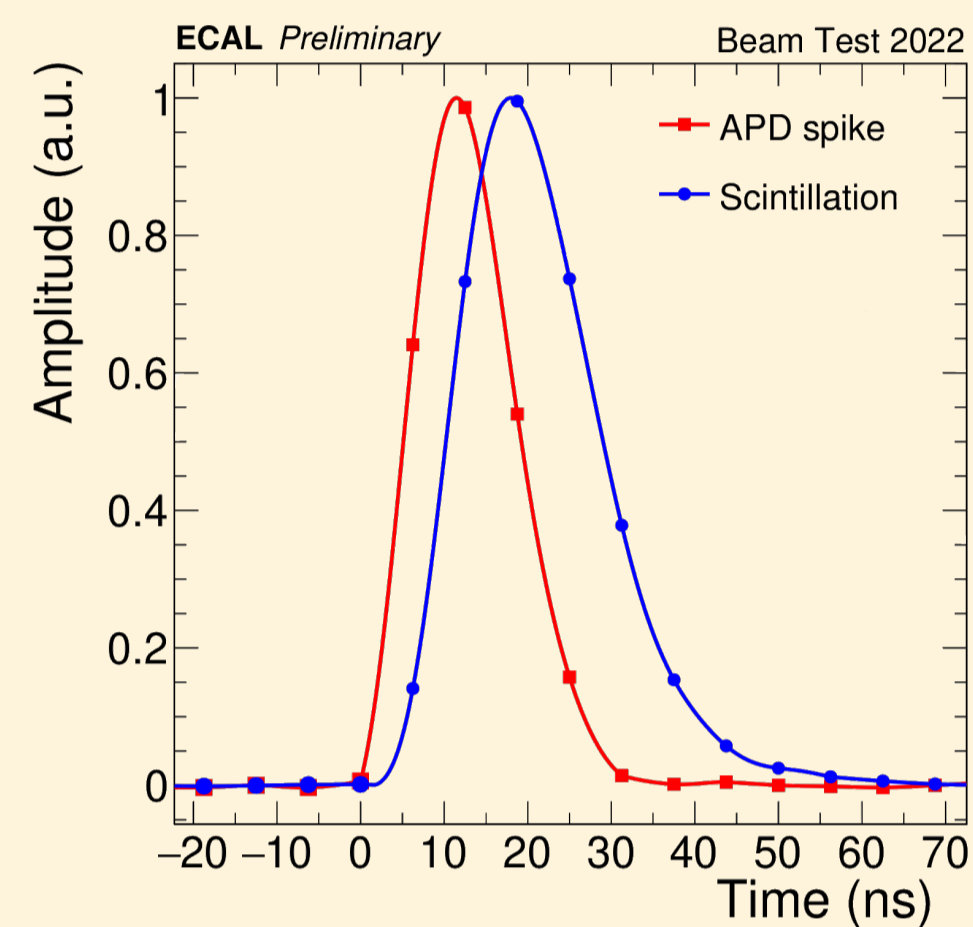### HL-LHC upgrade challenges for the ECAL barrel

* Increased **pileup** from 40~60 up to 200

* Increased **noise** caused by detector and sensor **ageing**

Faster front-end (FE) electronics to

* **Improve time resolution** for better primary vertex reconstruction –> **≤30 ps for E>50 GeV**

* **Discern scintillation signals** from **APD spikes** (signals from direct ionization of the APDs)

The new readout unit for Phase-2 (HL-LHC)

New VFE card   New FE card
Lead-Tungstate crystals
Master lpGBT ASIC
Control (2.5Gbps)
Readout (10Gbps)
3 x Readout lpGBT
Readout (10Gbps)
Versatile link plus
Control link
Readout links
APDs Pre-Amplifier ADC

Unchanged in Phase-2:
* Geometry
* Crystals
* Avalanche photo-diodes (APDs)

QFN72 package   2 mm x 2 mm

ECAL *Preliminary*   Beam Test 2022
— APD spike
— Scintillation
Amplitude (a.u.)
Time (ns)

APDs
PWO crystal
EM shower

CATIA
CAlorimeter **T**rans-**I**mpedance **A**mplifier

TIA   x10   x1
TSMC 130 nm

New faster amplifier with 2 gains to cover a range from **50 MeV to 2 TeV**

LiTE-DTU
Lisbon-**T**urin **E**CAL **D**ata **T**ransmission **U**nit

ADCH 12 Gain selection 13 Data compression 32 Ouput FIFO + Serization 1.28 Gb/s
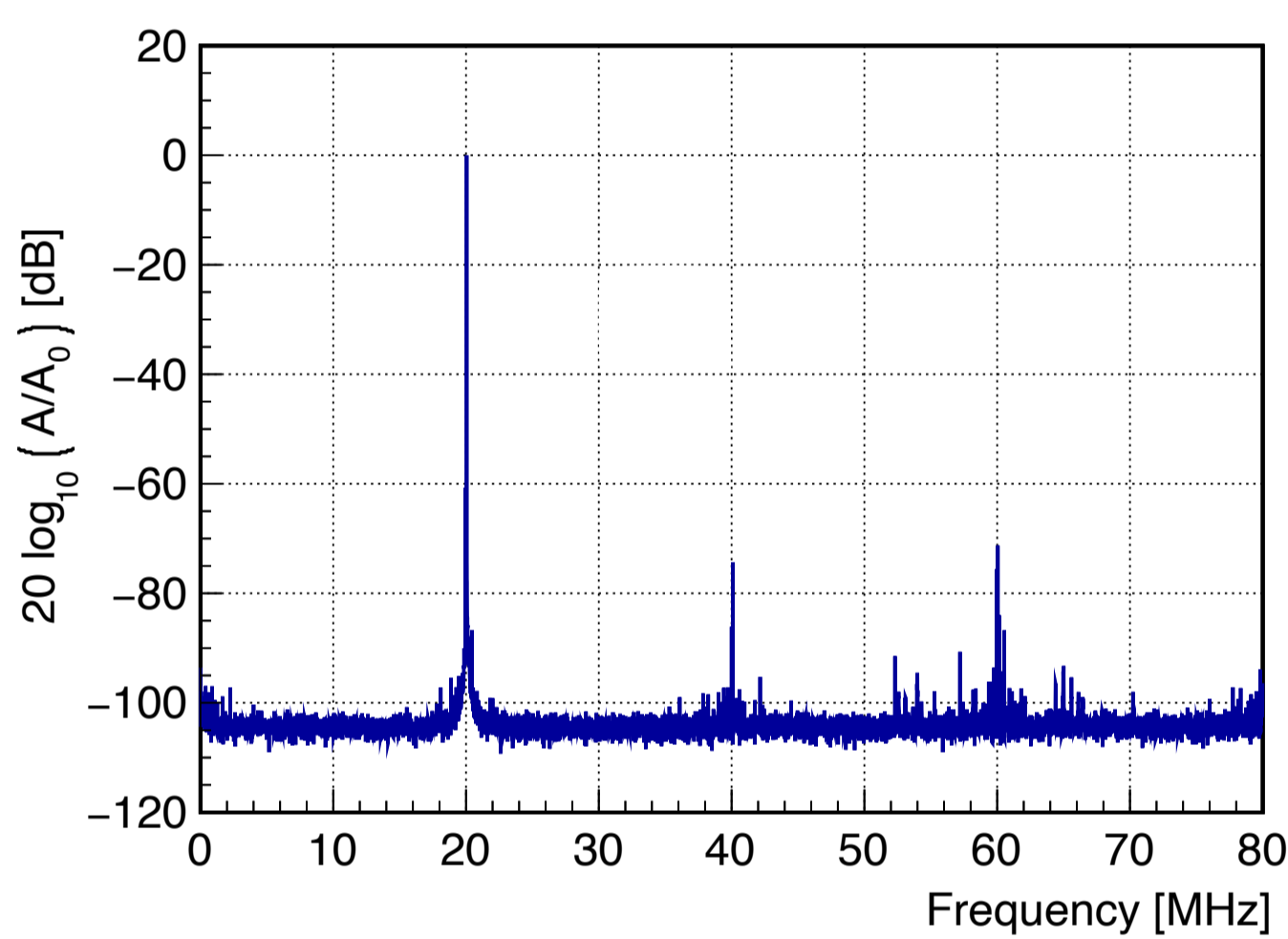ADCL 12
TSMC 65 nm

New data conversion and digital processing ASIC with higher sampling rate: **40 MS/s –> 160 MS/s**

The highest non-saturated sample is **selected with a look-ahead algorithm** and the **data is compressed** to fit the bandwidth of 1.28 Gb/s
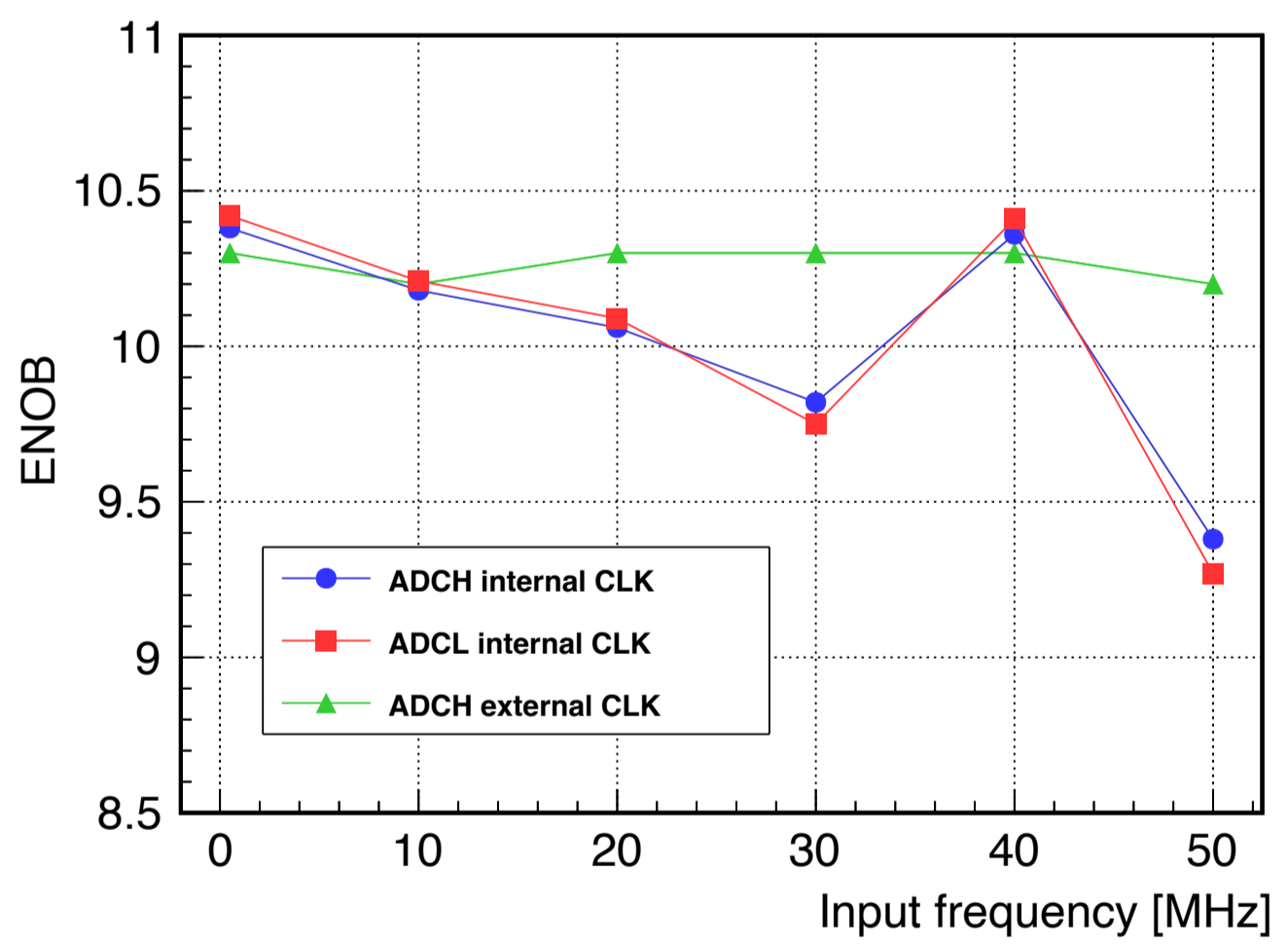
Serialisers send 32-bit words off-detector

Example of Fourier analysis used to evaluate the effective number of bits (ENOB)

$20 \log_{10} (A/A_0)$ [dB]
Frequency [MHz]

ENOB
Input frequency [MHz]
- ADCH internal CLK
- ADCL internal CLK
- ADCH external CLK

The ADCs

* Two **160 MS/s 12-bit** ADC IPs designed by Adesto (now Renesas)

* **Time-interleaved successive approximation register (SAR)** architecture

The LiTE-DTU ASIC

Digital block designed at INFN Torino

x 10 ADC 12   Depth: 8·16 12 Sample selection 13   DTU
x 1   ADC 12
External test clock 1.28 GHz
32 Frame trailer   Data compression
160 MHz PLL
1.28 GHz
Control unit WR full RD empty   Depth: 16
Phase-locked loop (PLL) block taken from CERN lpGBT design
ATU 4 x 32 Serializer Serializer Serializer Serializer   4 x 1.28 Gb/s

The design is made **tolerant to single event upsets (SEUs)** through triple modular redundancy (TMR)

Lossless data compression

* Needed for the transmission of 12+1 bit samples at 160 MS/s (2.08 Gb/s) over a 1.28 Gb/s link

* Compression algorithm –> **simplified Huffman encoding:**

  - If E>2.5 GeV –> 13-bit sample
  - If E<2.5 GeV –> 6-bit sample

  Where the probability of having E>2.5 GeV is less than 5×10^{-5}

fraction of events
— Total
— Scintillation
— APD
E_T (GeV)
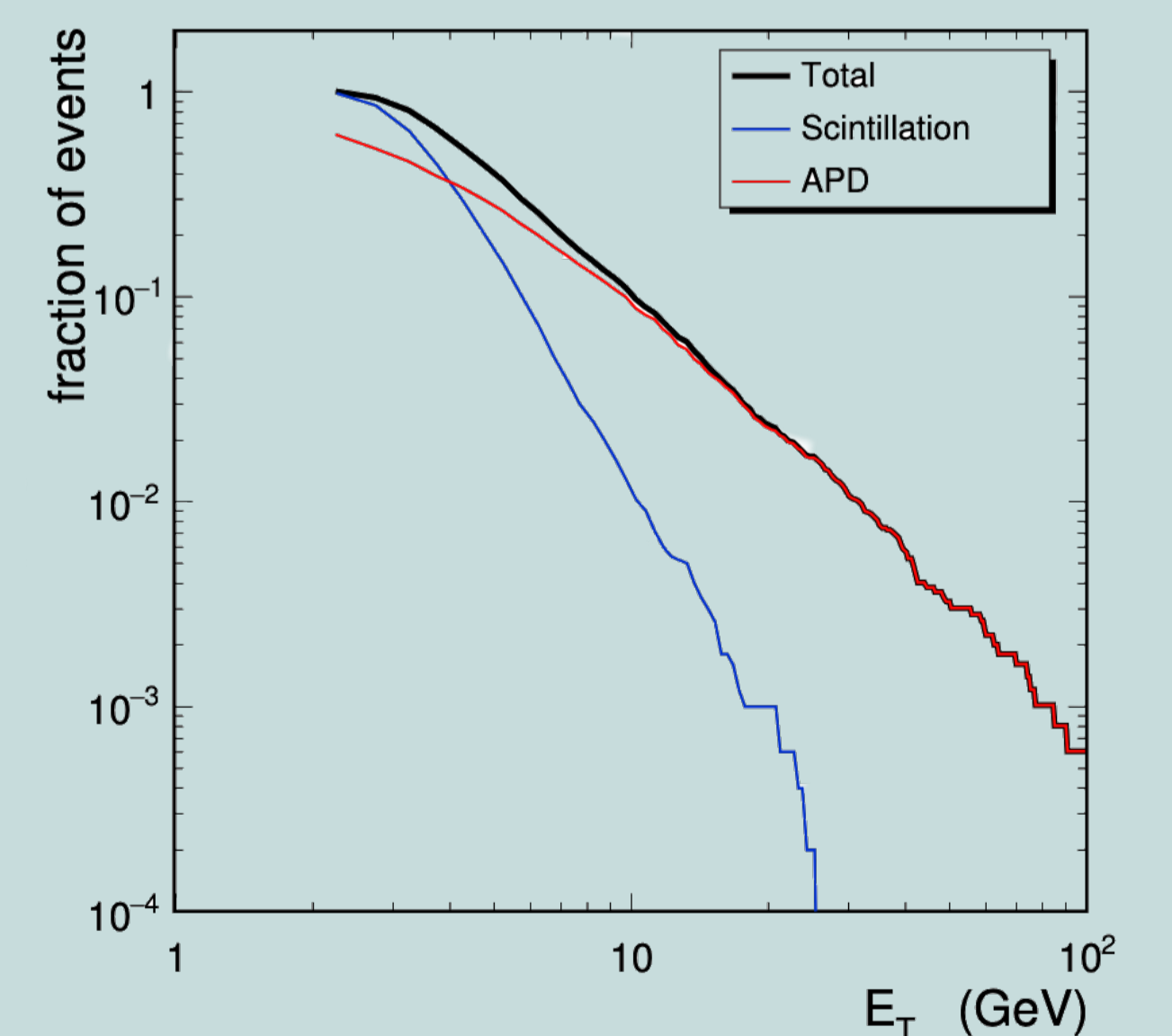
The throughput reduces to ~1.1 Gb/s

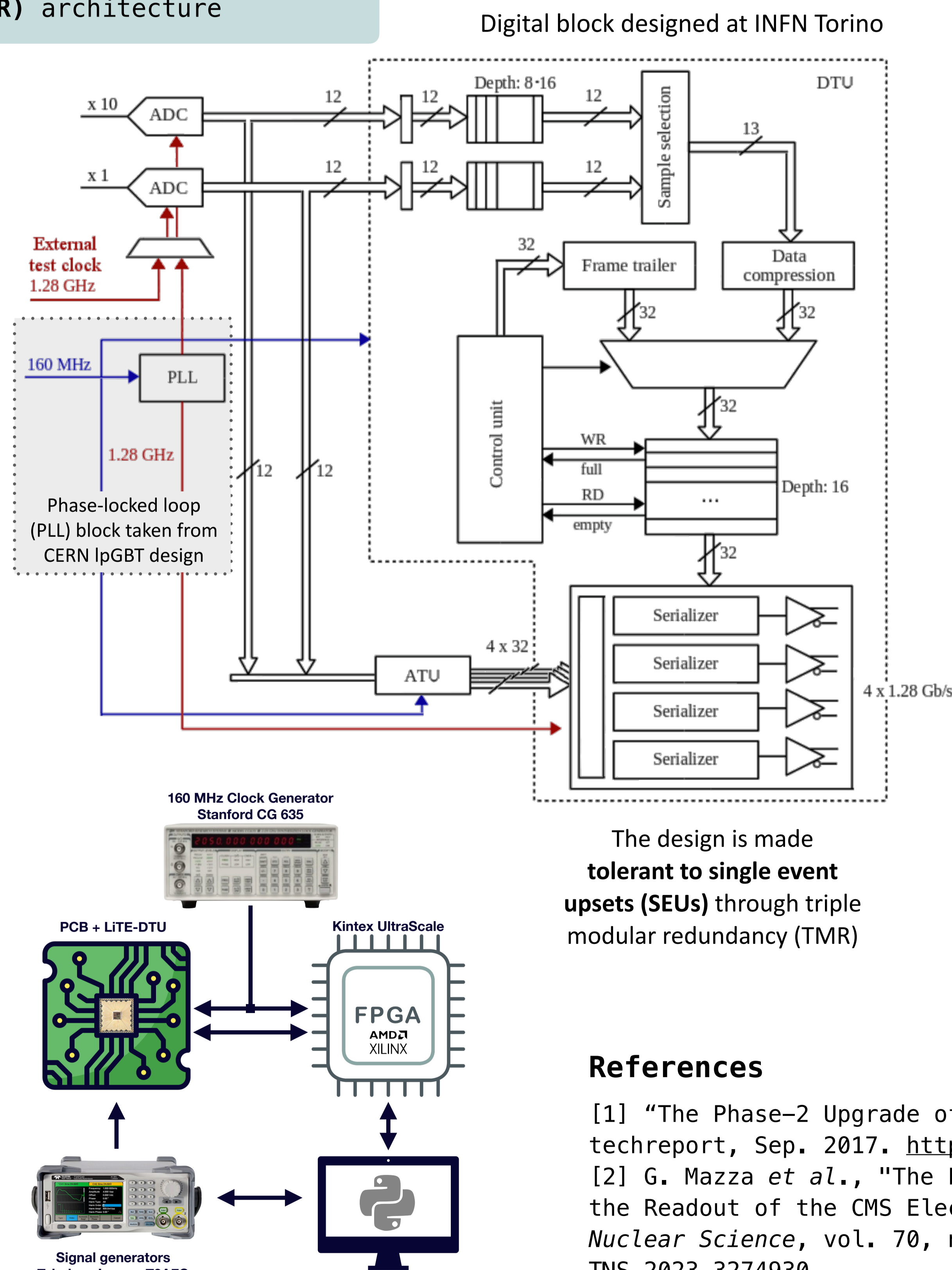### Preproduction on-bench testing

* Automatic test procedure:

  - Reset and power test
  - Configuration and PLL lock check
  - Data alignment
  - ADCs calibration
  - Pulse decoding tests

* Results on 553 chips:

  - **535 fully working**
    10 too noisy (>1 ADC rms)
    1 unable to calibrate
    6 unable to align
    1 unable to contact

  –> **Yield ~97%**

* A simplified schema of the on-bench test setup →

160 MHz Clock Generator Stanford CG 635
PCB + LiTE-DTU   Kintex UltraScale   FPGA AMD XILINX
Signal generators Teledyne Lecroy T3AFG

References

[1] "The Phase-2 Upgrade of the CMS Barrel Calorimeters", CERN, Geneva, techreport, Sep. 2017. https://cds.cern.ch/record/2283187

[2] G. Mazza *et al.*, "The LiTE-DTU: A Data Conversion and Compression ASIC for the Readout of the CMS Electromagnetic Calorimeter", in *IEEE Transactions on Nuclear Science*, vol. 70, no. 6, pp. 1215-1222, June 2023, doi: 10.1109/TNS.2023.3274930.

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