

16<sup>th</sup> Topical Seminar on Innovative Particle and Radiation Detectors IPRD 2023

Title: Hough Transform FPGA Solution for High Energy Physics Online Fast Tracking

Authors: Fabrizio Alfonsi<sup>2</sup>, Francesca Del Corso<sup>2</sup>, Alessandro Gabrielli<sup>1,2</sup>

1)University of Bologna, Italy;

2)Istituto Nazionale di Fisica Nucleare, Bologna section;

Topic: Data Acquisition and Triggering;

In the next few years the High Energy Physics experiments at CERN as CMS and ATLAS will start the upgrade of their exploited technologies and methodologies for the experiment runs at the end of the decade. Through the major upgrades the LHC accelerator as well will face several changes which will allow it to reach a peak of luminosity up to  $5-7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . These and many other new occurrences will force the experiments to handle far more data at the end of the data acquisition chain. For example they will push the major CERN experiments as ATLAS to exploit the online tracking for their inner detector to reach 10 kHz of final selected events from 1 MHz of Calorimeters and Muon Spectrometer trigger discrimination. In the list of the architectures under study to reach the goal of fast tracking there is for example the usage of a "hardware accelerator" farm, an infrastructure made of interconnected accelerators as GPUs and FPGAs to speed up the tracking processes. The project described here is a proposal for a tuned Hough Transform algorithm implementation on high-end FPGA technology, versatile to adapt to different tracking situations. The development platform lets to study different datasets from a software "emulating" the firmware and to consequently perform hardware tests for real online run prototyping. AMD-Xilinx FPGA have been selected to test and evaluate this implementation, in particular few boards have been used to test the reliability and apply specific checks. The VC709 and the VCU1525 accelerator cards are the currently used development boards, with the Alveo U250 under the final implementation steps. What have been exploited are low-level strategies for the firmware architecture and the card's features as PCI Express data transfer and the  $> 1$  million gates array available. The system has been tested with the ATLAS realistic environment. Simulated 200 pile up events have been exploited to measure the algorithm effectiveness. The processing time is in the order of  $< 10 \mu\text{s}$  averagely by internal preliminary estimates, with the possibility to run two events at a time per algorithm instance. Internal efficiency tests have shown conditions which reached  $> 95 \%$  of performance in track finding for single muon tracking.