Radiation Hardness and Quality Validation of the On-Detector Electronics for the CMS Drift Tubes Upgrade

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In view of the High Luminosity LHC upgrade, the so-called Phase 2 upgrade, the electronics of the Drift Tubes (DT) subdetector of CMS will undergo a complete innovation. Requirements in terms of trigger rate will exceed the capabilities of the present electronics [1]. Thus, all the on-detector electronics together with the associated back-end need to be replaced. Maintainability and chamber aging mitigation are also important driving factors for the new design. Leveraging the evolution of fast optical links and the availability of higher bandwidth technologies, the Phase-2 upgrade will be an opportunity for rearranging the partitioning of the electronics. On-detector electronics will be minimized to the digitization and the full data transfer far from the harsh environment of the detector experimental hall, with algorithms processing and data readout pipelining happening in the back-end hosted in the counting room. Profiting from the less constraining conditions and easier access, a much wider assortment of hardware solutions increases reliability and opens to possible future improvements. Phase-2 on-detector electronics for DT consist of about 600 FPGA (Field Programmable Gate Array) based boards called OBDT phi (On-detector Board for Drift Tubes for Phi Chambers) and about 200 boards called OBDT theta (On-detector Board for Drift Tubes for Theta Chambers). . A first demonstrator of the PBDT phi board [2] has been deployed during the last long shut down of LHC on a sector of the detector, and a preproduction of the final electronics has been developed and deployed in CMS during the last winter shutdown. Essential changes have been made to the card to allow integration in the CMS system. Slow control and time distribution are provided through the LpGBT chip and the VTRX+ optical transceiver. The clock distribution on the board has been redesigned, optimizing the tasks of the firmware on the FPGA (it implements 240 TDCs for the hits digitization). A robust safety system has been added to the design to ensure controlled conditions of the card, which is particularly difficult to access for maintenance. Choice of components known to

[1] The Phase-2 Upgrade of the CMS Muon Detectors. Technical report, CERN, Geneva, Sep 2017.

[2] A. Triossi et al. Electronics Developments for Phase-2 Upgrade of CMS Drift Tubes. PoS, TWEPP2018:035, 2019.

have good resistance to radiation was a requirement in the design of the OBDT phi. The main component, the FPGA, is a flash-based PolarFire from Microsemi already qualified in different facilities for radiation hardness tests [3] [4] . As a validation step, two campaigns of radiation test have been carried out on the full OBDT phi board, assessing its behavior during a radiation exposition with a total dose much higher than that integrated during 10 years of HL-LHC. The outcome of the radiation tests along with all the quality tests executed in the laboratory for proving the validity of the card will be illustrated, particularly showing the effectiveness of the TDCs thanks to an extensive qualification on real environmental conditions. Along with the board development, a test bed that exercises all the functionalities of the OBDT phi was prepared. This will provide quality control of the cards after manufacturing and after installation on its mechanics supports and transportation to the installation site.

[3] Microsemi. PolarFire Neutron SEE Test Report. Technical report, Microsemi, LANL, 2018.

[4] A. Scialdone, R. Ferraro. Microsemi PolarFire MPF300TS FPGA PSI Radiation Test Report. Technical report, CERN, 2020.