

## **Title:** The DMAPS Upgrade of the Belle II Vertex Detector

### **Abstract:**

The Super-KEKB collider will undergo a major upgrade to reach the target luminosity of  $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ . A long shutdown is foreseen around year 2027, which provides the opportunity to revisit significant parts of the Belle II experiment and adapt them to the expected change of the experimental conditions. In particular, a new pixelated vertex detector (VTX) is being designed to fit the upgraded interaction region. This new silicon tracker aims to be both more robust against the expected higher level of machine background and more performant in terms of precision and standalone track finding efficiency.

The VTX design presented here features an envelope close to the present one, spanning from radii of 14 mm to 135 mm. The baseline layout consists of two identical layers composing the inner part (iVTX) and three outer layers (oVTX), all arranged in a barrel-shaped geometry, with minimal material budget.

It is equipped with a dedicated depleted-MAPS CMOS sensor named OBELIX. The latter is an approximately 2 cm x 3 cm large die designed in the Tower 180 nm technology, which pixel matrix is derived from the TJ-Monopix-2 sensor originally developed for the ATLAS experiment. Featuring a 33  $\mu\text{m}$  pitch, the pixel sensor will integrate hits over a 100 ns period while dissipating less than 200 mW/cm<sup>2</sup> at an average hit rate of 60 MHz/cm<sup>2</sup>. The digital trigger logic is entirely revisited to match Belle II requirements of 30 kHz average trigger rate with 10  $\mu\text{s}$  trigger delay and a maximum hit rate of 120 MHz/cm<sup>2</sup>. A first complete version of the sensor is being designed and is expected to be submitted to foundry by late 2023.

The two iVTX layers have a sensitive length of about 12 cm and are based on an “all-silicon ladder” concept aiming for a material budget below 0.2 %  $X_0$ /layer, benefitting from air cooling. One ladder is made of a 4-sensor wide module cut out from the processed wafer and submitted to post-processing operations in order to connect them at one end.

As for the oVTX, the target material budget is ranging from 0.3 %  $X_0$  for layer 3 up to 0.8 %  $X_0$  for the 70 cm-long ladders of the fifth and most external layer. An evolved design of the ladder concept used in the ALICE-ITS2 is adopted, with a light mechanical structure, supporting a liquid-cooled plate.

The talk will review all aspects of the project: the tests of the TJ-Monopix2 validating the pixel matrix performance, the OBELIX-1 features and design status, and finally prototype fabrication and tests for the iVTX and oVTX concepts.

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**Request:** Oral presentation

**Speaker:** to be defined upon acceptance

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