The DMAPS Upgrade of the Belle II Vertex Detector

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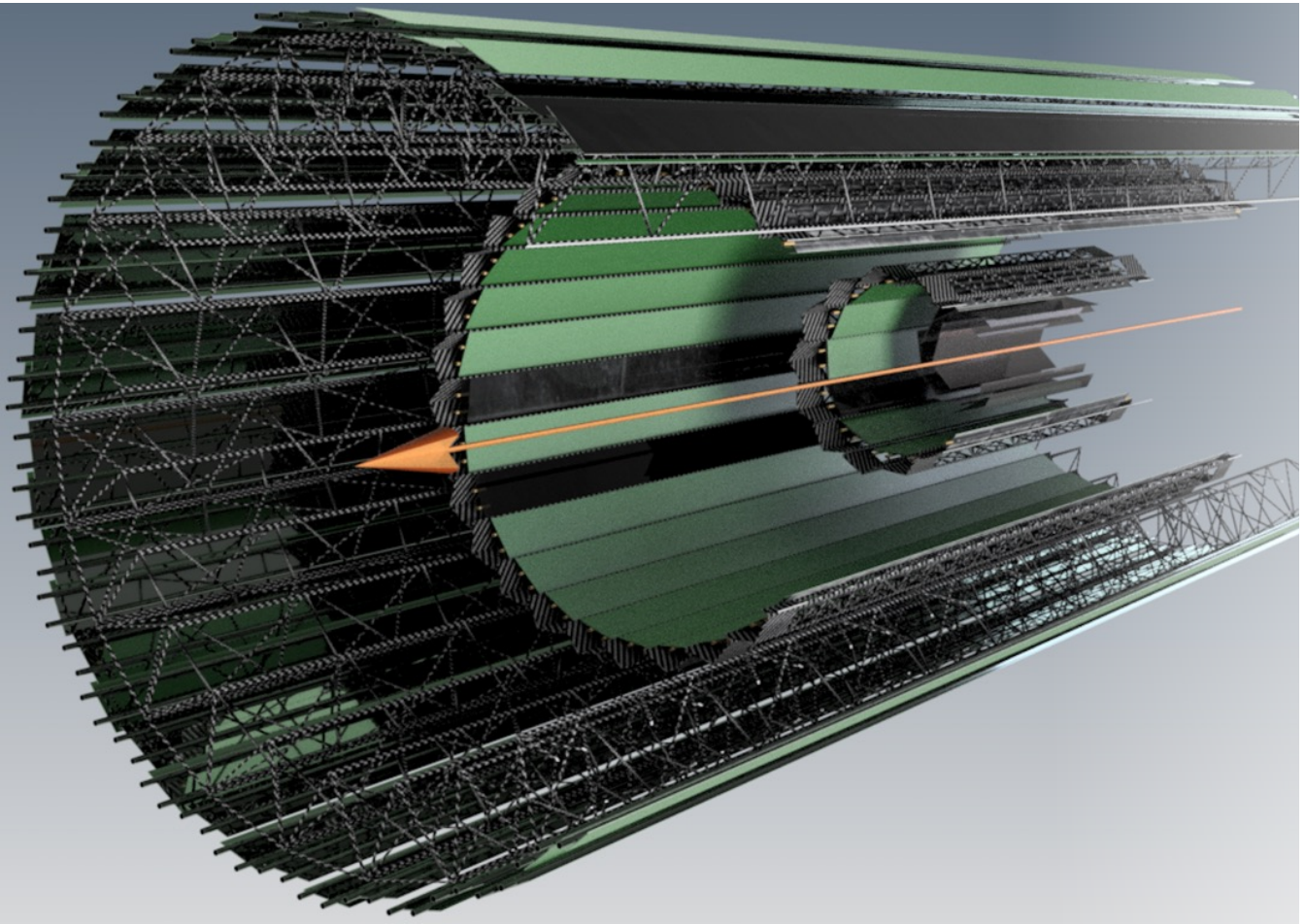


16TH TOPICAL SEMINAR ON INNOVATIVE PARTICLE AND RADIATION DETECTORS (IPRD23)

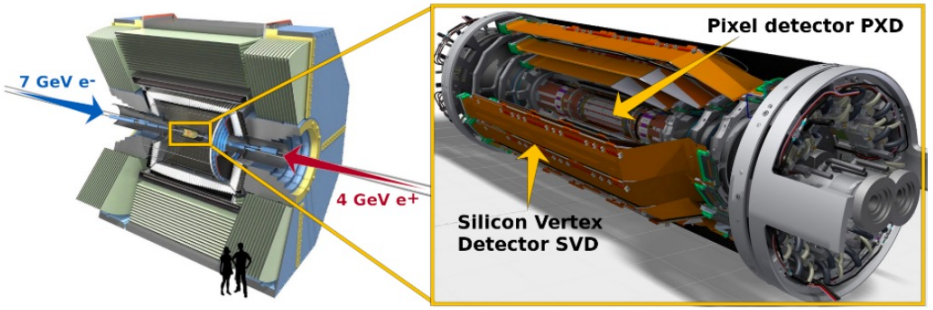
Siena, 25 - 29 September 2023

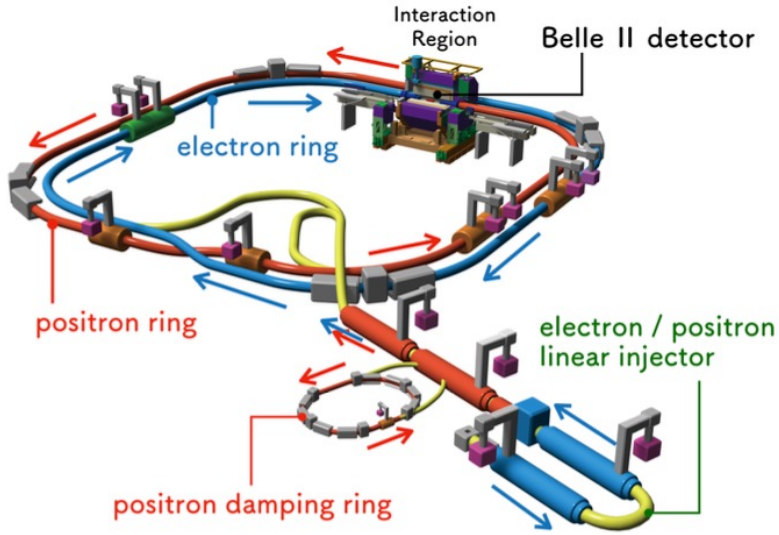
OUTLINE

- Upgrade motivations
- All-pixel VTX design
- Vertexing/Tracking performances
- The OBELIX chip
- Chip TJ Monopix2:
  - Lab. Test Results
  - Test Beam Results
- Mechanics: iVTX & oVTX concepts:
  - Low-mass ladder R&D
  - support structure&cold-plate prototypes
- Conclusions

SuperKEKB and Belle II Upgrade Motivation(s)

The **SuperKEKB** upgrade is planned during the **L**ong **S**hutdown **2** (around 2027): a major redesign of the I.R. needed to reach the target luminosity ($L = 6\ 10^{35}\ cm^{-2}\ s^{-1}$) to increase the sensitivity of the Belle II experiment in searches for possible effects beyond the SM in flavor, tau, EW and dark sector physics.



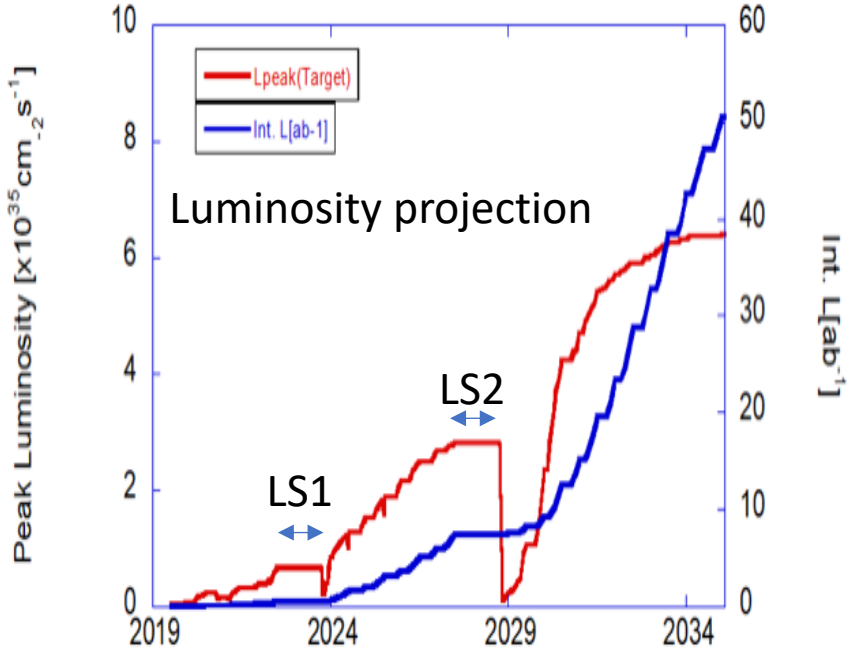


The current VXD (PXD + SVD)
has quite limited safety margins for running at higher luminosity:

- Performance degradation expected for higher occupancy

LS2 provides the opportunity to install an upgraded detector to cope with the expected change of the experimental conditions.
The new pixel vertex detector (VTX) should improve:

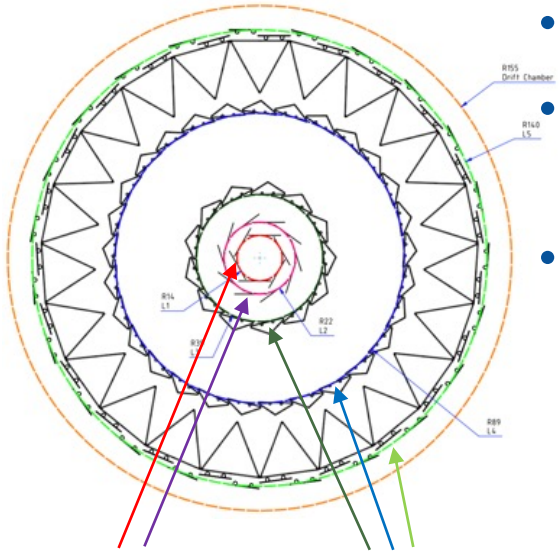
- robustness against harsh machine backgrounds, predicted at the higher luminosity with large extrapolation uncertainties
- resolution and track finding efficiency



The VTX baseline Concept

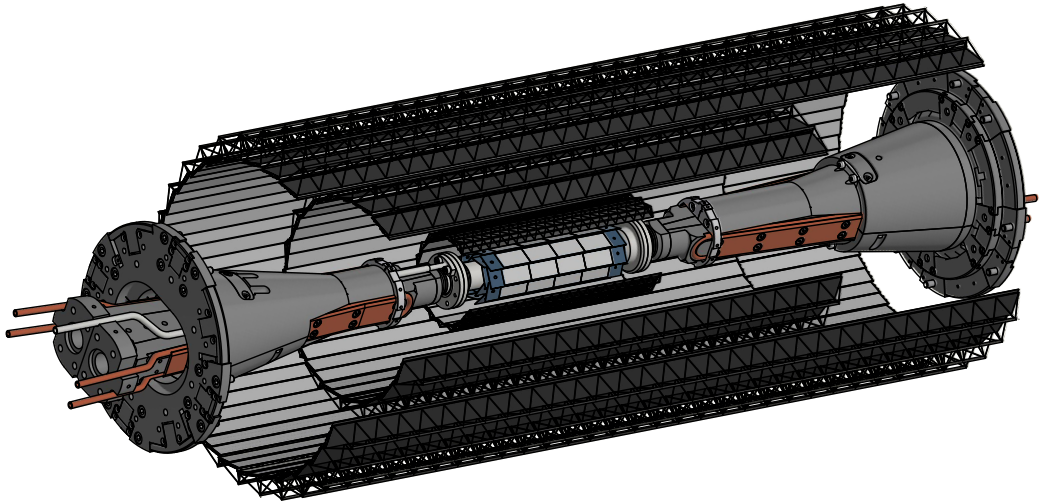
- **Low material budget** (~50 µm thin sensors):
  0.1% X_0 (L1-2), 0.3-0.5% X_0 (L3-4), 0.8% X_0 (L5)

- **Requirements:**
  - **Radiation levels for L1** (r=1.4 cm)
    - TID: ~10 Mrad/year
    - NIEL: $\sim 5 * 10^{13}$ n_{eq}/cm^2/year
  - **Hit-rate up to 120 MHz/cm²**
  - **Resolution < 15 um**
  - **Fast integration time 50-100 ns**
  - **Operation simplicity and reduced services**



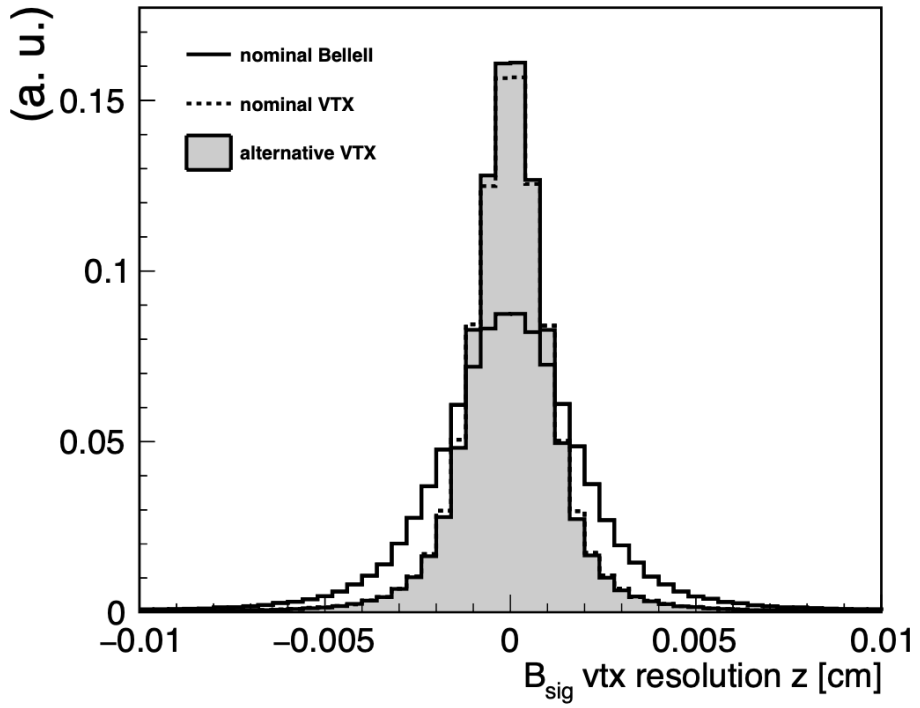
- 5 straight **fully pixelated** barrel layers
- **Same sensor chip for all layers**
- **iVTX**: Innermost section (2 layers), self-supporting, air cooled
- **oVTX**: Outer sections (3 layers), CF structure, water cooled
  - L3@3.9 cm (alternative @6.9 cm)
  - L4@90 cm, L5@13.5 cm
- **Power dissipation** ~200 mW/cm²

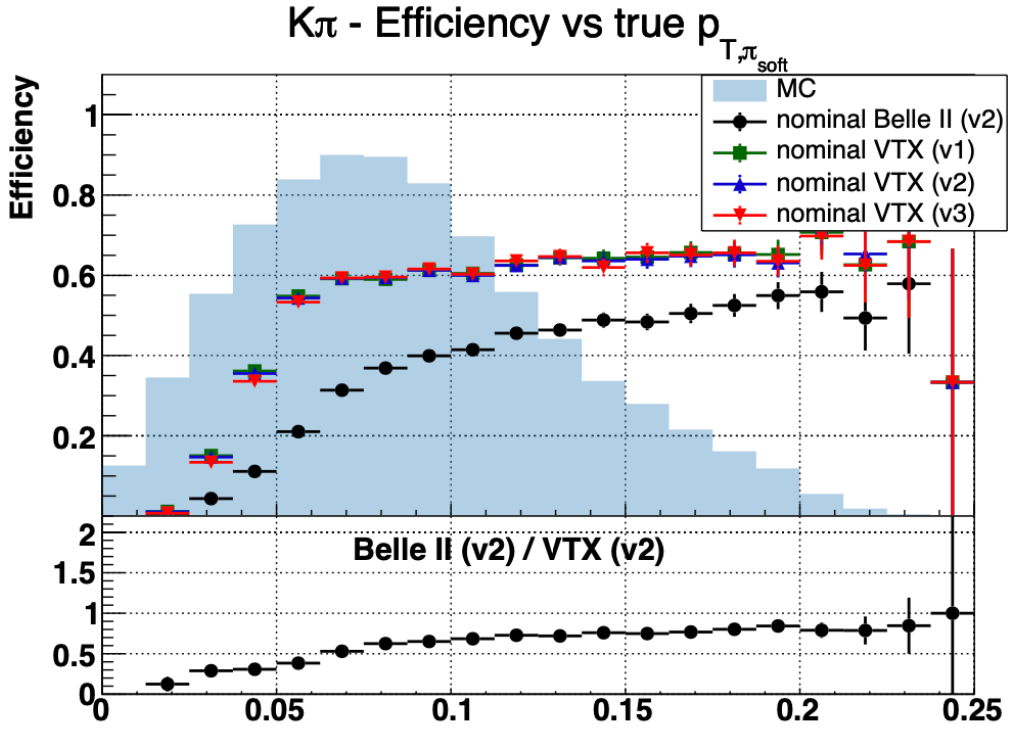
- **Depleted monolithic active CMOS** pixel sensors
  - Chip size: 2x3 cm²
  - Moderate pixel pitch 33 µm²



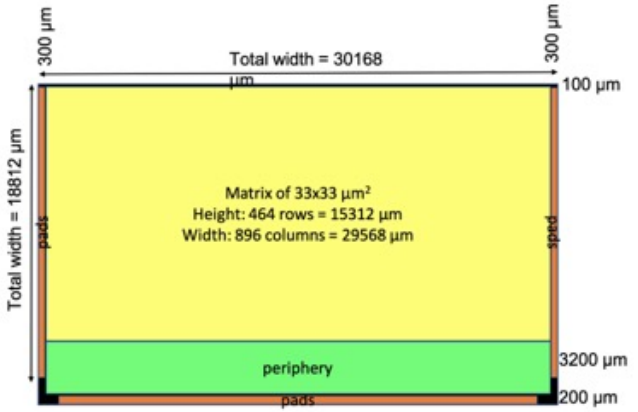
VTX: Vertex/Tracking Performance

- Performance studies using benchmark channels, based on simulations of signal events with 3 possible cases of overlaid background (best:v1, intermediate:v2, worst:v3):
  - Possibility to include all layers in the tracking
  - A factor 200 in reduction in occupancy due to the faster integration time (and smaller pitch)
- VTX provides 35% better vertex resolution than the current VXD in the channel $B^0 \to J/\psi K_S^0$ and it is insensitive to the level of background
- Better tracking efficiency than current VXD at low momentum (soft pions from D^*).





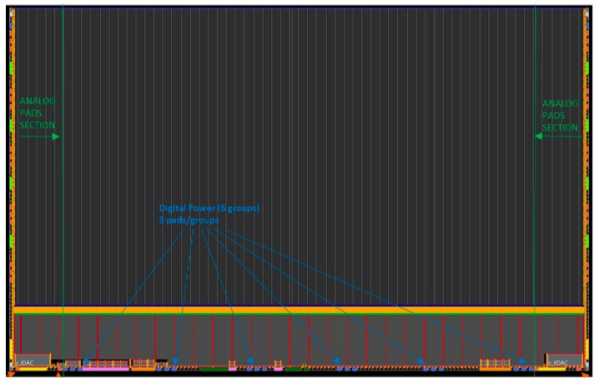
The OBELIX (Optimized BELle II pIX chip)

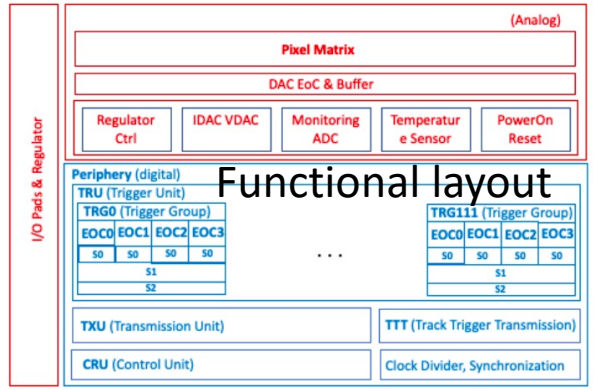


OBELIX MAPS design is based on the existing TJ-Monopix2(*) chip (TowerJazz 180 nm), developed for ATLAS, with core spec's on readout speed & max. rate matching Belle II needs. OBELIX will include:

(*) NIMA 978 (2020) 164460

- a new digital periphery for the trigger logic
- a trigger signal & finer time resolution on external layers, to improve BG rejection.





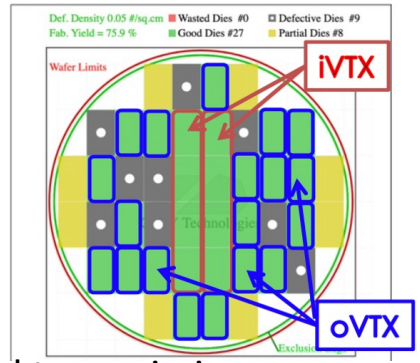
Functional layout

Design features:

- Signal digitization: ToT (7 bits, 20 MHz)
- Threshold value set at single pixel level
- End-of-Column Logic trasmits ToT and timestamp (Bunch Crossing Id), Timestamp precision: 50 ns
- Matrix r.o. logic sustains a hit-rate > 600 MHz/cm^2. Sensor peripheral logic able to trasmit data up to a hit-rate of 120 MHz/cm^2 (340 Mbps throughput).

Extensive tests on TJ-Monopix2 as a "proof of principle" of prototype sensor for Belle II VTX:

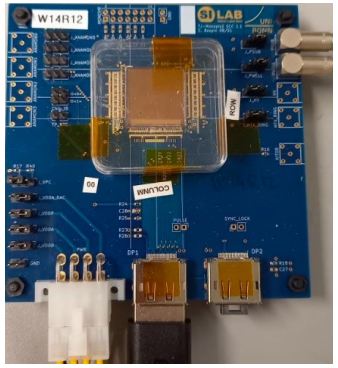
- Full chacterization on bench: threshold scans, calibrations
- Test-beams@DESY: Efficiency/Resolution measurements
- Radiation hardness (NIEL and TID irradiation campaigns in progress)



Chip size optimized to maximize the number of 4 contiguous sensors

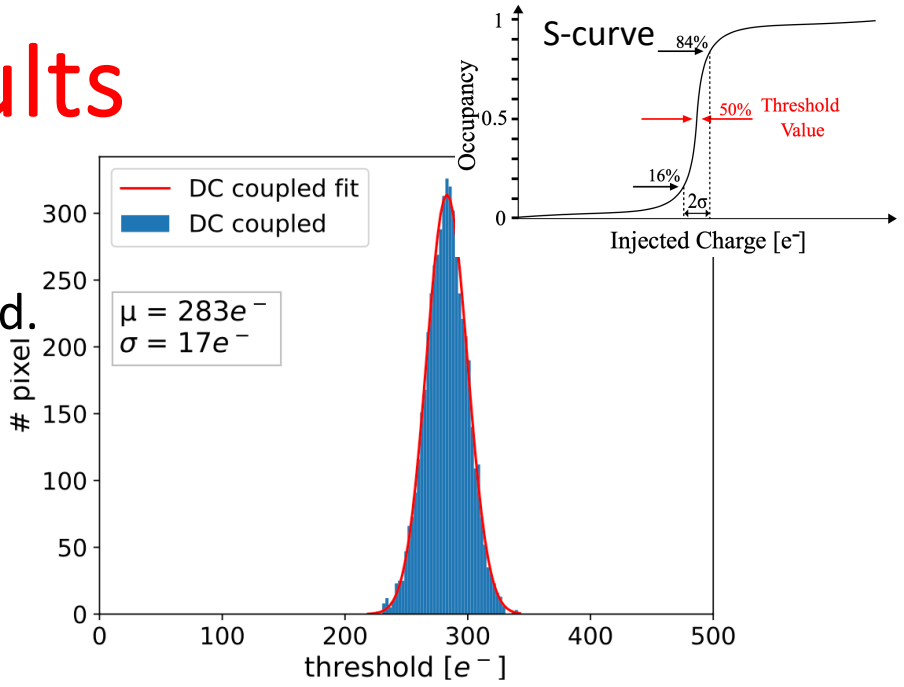
The submission of the chip to the foundry is expected at the end 2023.

TJ Monopix2 Lab test results



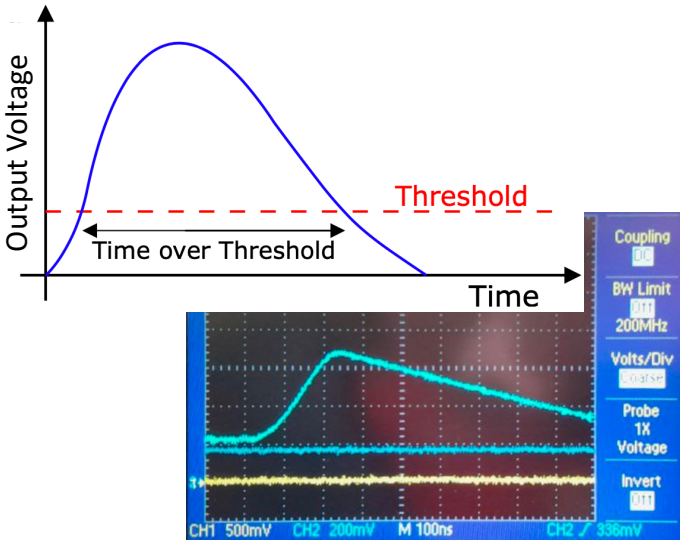
- Tests done in in Bonn, Pisa, HEPHY, CPPM, Gottingen
- S-curve tests with internal $C_{injection}$ to determine threshold.

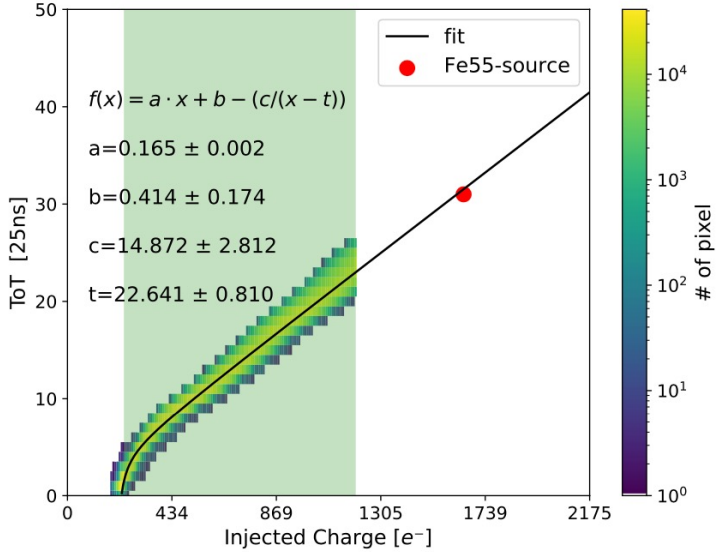
Sensor tuned for low threshold and low dispersion:
Threshold: (280 ± 17)e− , Noise: 8e−

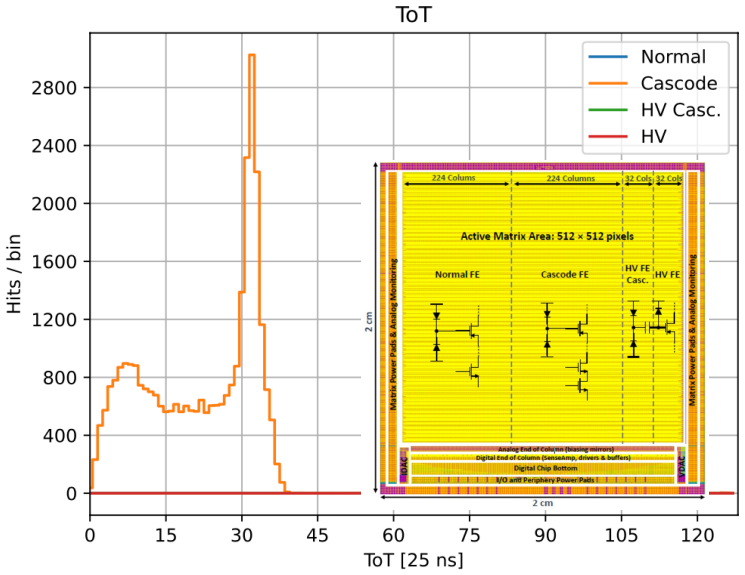


- Calibrate **T**ime-**o**ver-**T**hreshold with injection test:

(ToT in units of 25 ns 7-bit encoded)
Absolute calibration with Fe^{55} source agrees with design, measurements ranging 8.5 - 10 e-/DAC







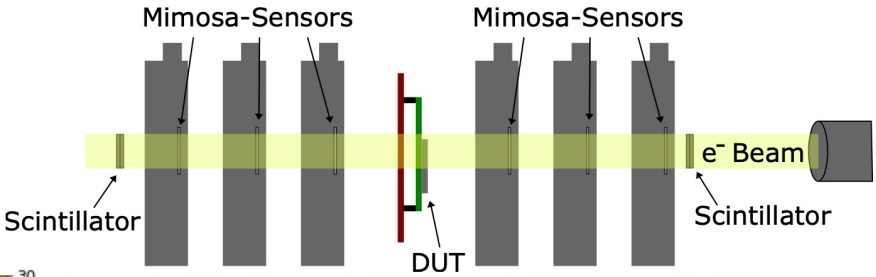
TJMP2 sensor is divided in 4 regions with different pixel FE

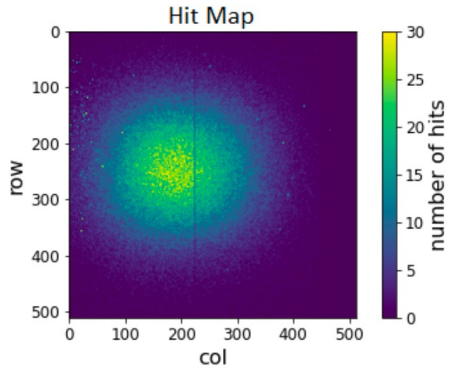
Test-Beam campaign (Desy: 4 GeV e-)

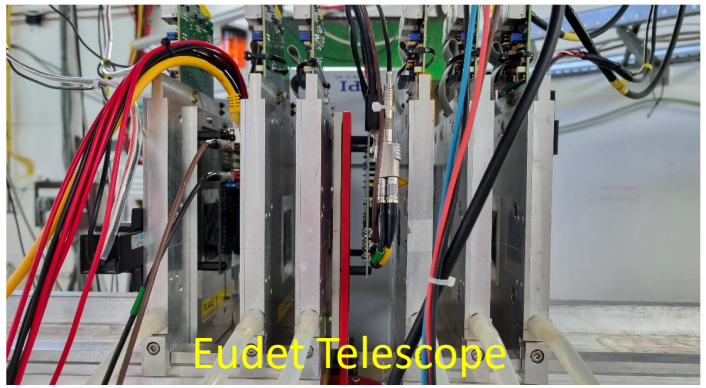
In June ’22: e- perpendicular to DUT

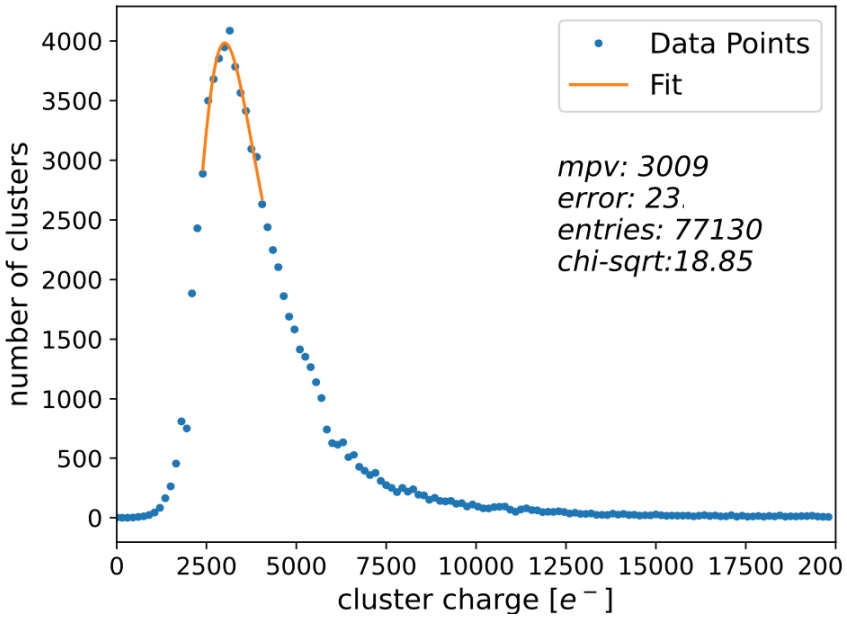
- Unirradiated chip
- Preliminary settings: used very high thr ~ 500e-
- Hit efficiency: 99.54 +- 0.04 %
- Cluster position residuals: 9.15 um

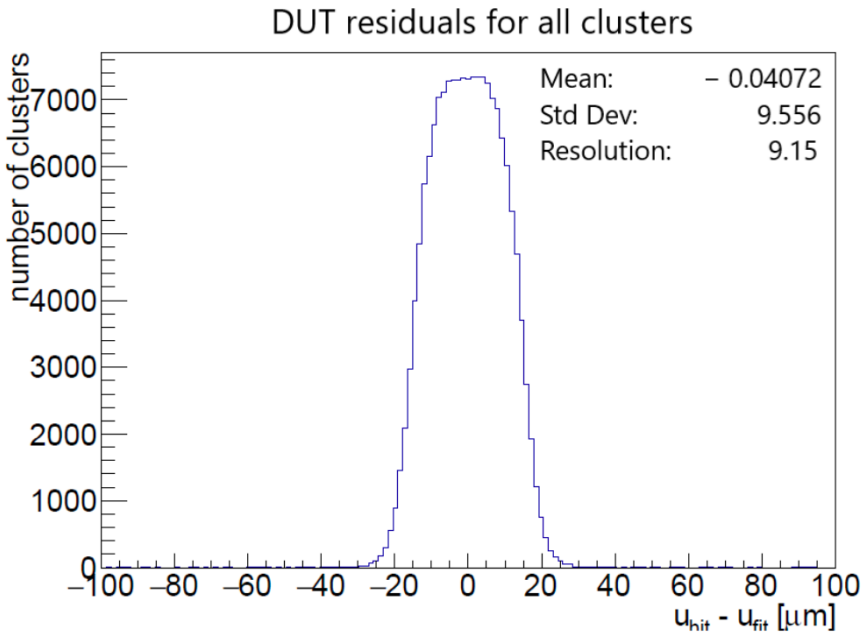
(< pitch/$\sqrt{12}$=9.5 um)











New test beam in July 2023:

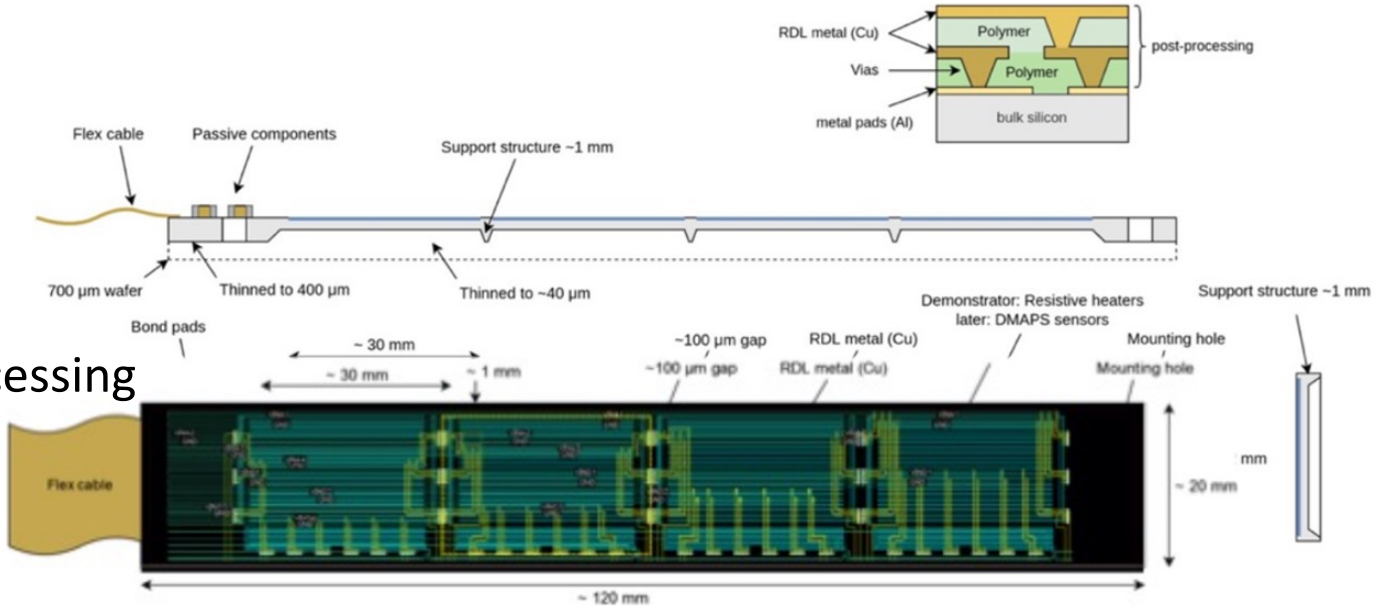
- Lower thr settings
- Angle scan
- Efficiency for irradiated chip (10^{14} – 10^{15} n_{eq}/cm^2)
- Data analysis ongoing:

(encouraging preliminary results!)

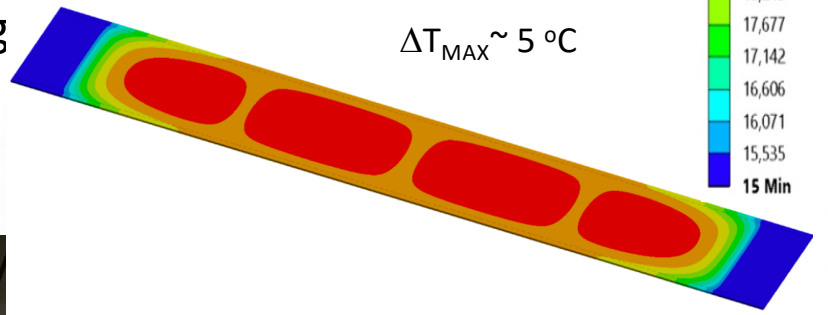
iVTX Demonstrator

All-Silicon module concept:

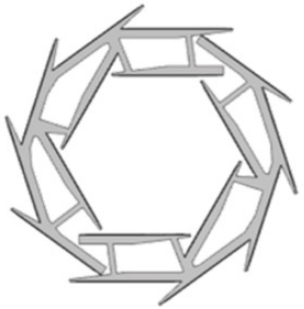
- 4 contiguous sensor block diced
- Hetherogeneous thinning for stiffness
- To interconnet sensors on the ladder, a post processing step etches metal strip on the redistribution layer (prototypes in production by IZM-Berlin)



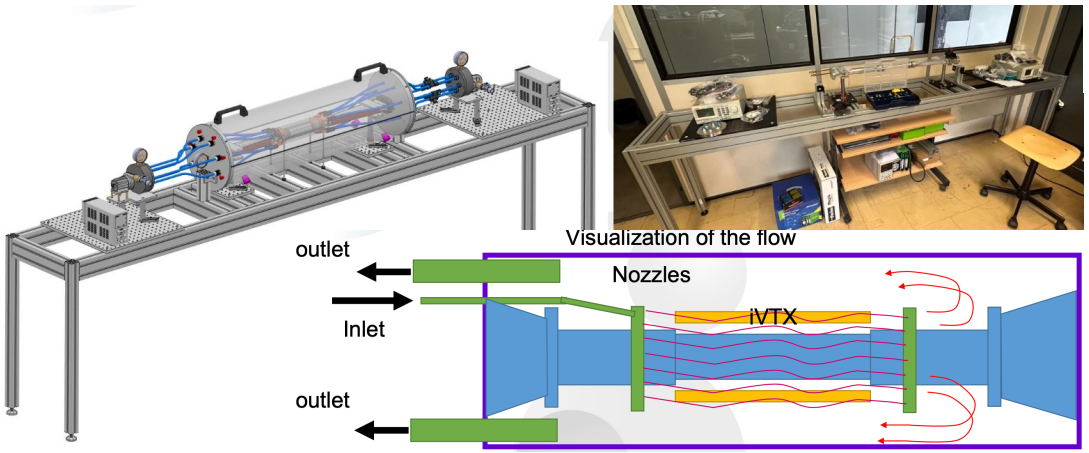
Results from air-cooling simulations on a single ladder: air at 15°C with speed ~10 m/s needed to evacuate a uniform power density of 200 mW/cm^2 , reaching a max. temperature of 20°C.



ΔT_{MAX}~ 5 °C



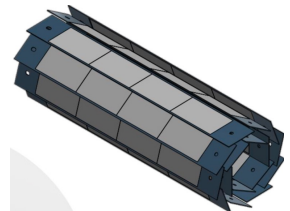
Windmill support structure
radii =14 + 22 mm



Visualization of the flow

Under set-up @IJCLab (Paris) a test-bench facility to evaluate the efficiency of an air-cooling system for the whole iVTX detector (P~80 W):

- heat exchange by convection
- air flow through the actual iVTX geometry
- mechanical vibrations with v_{air}~10 m/s to be measured.

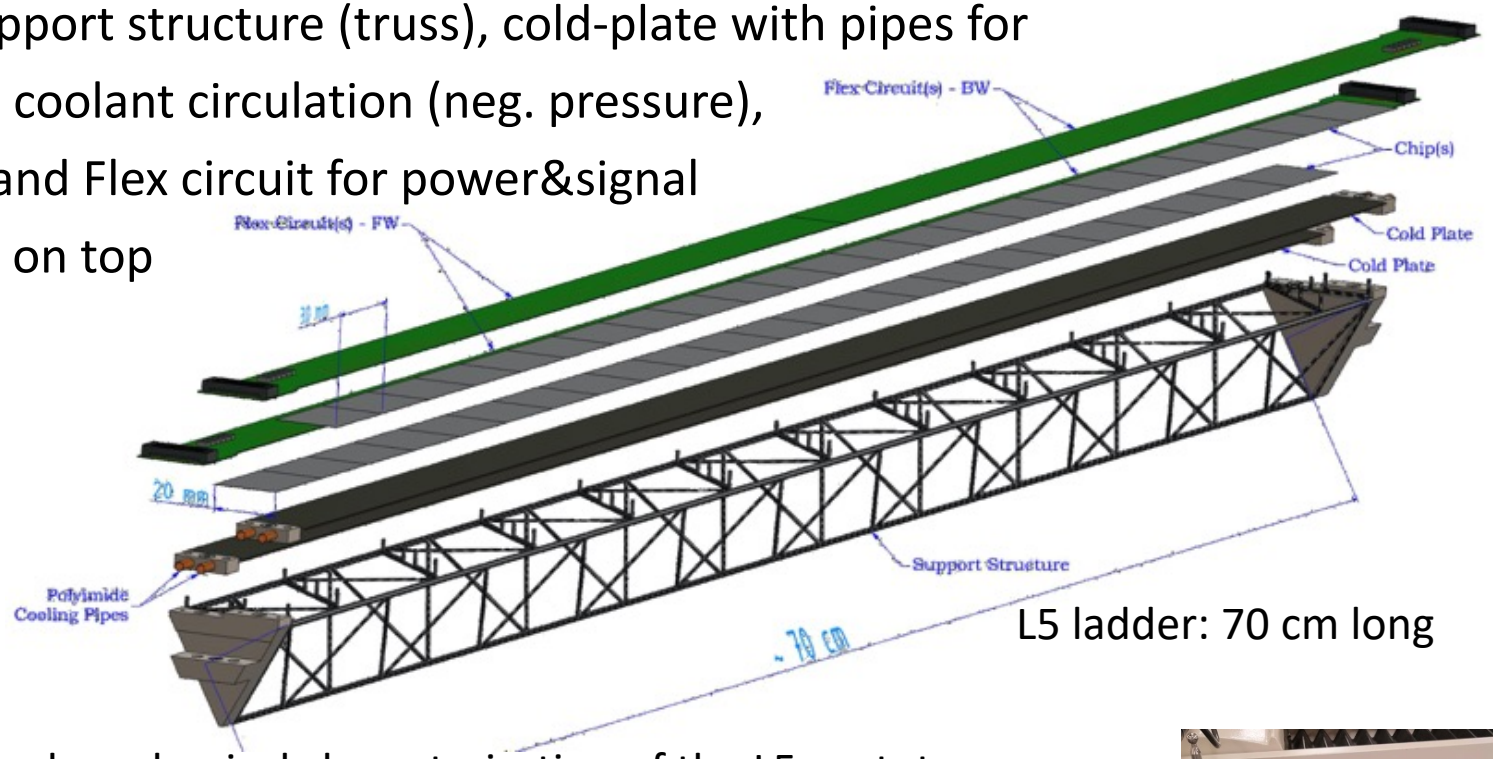


oVTX Thermomechanics

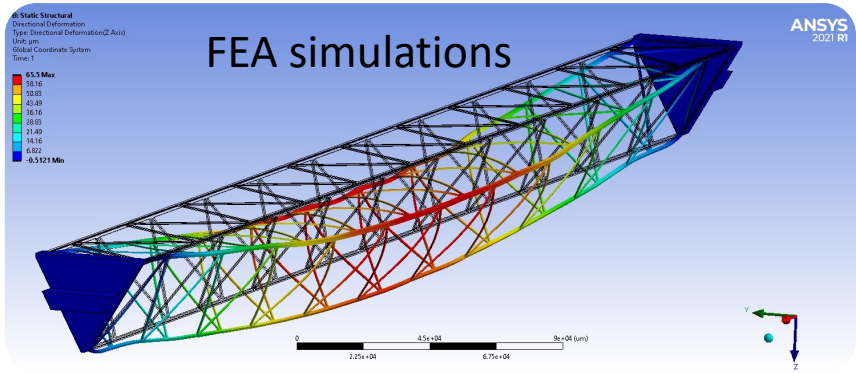
Ladder structure design inspired by ALICE ITS2, composed of:

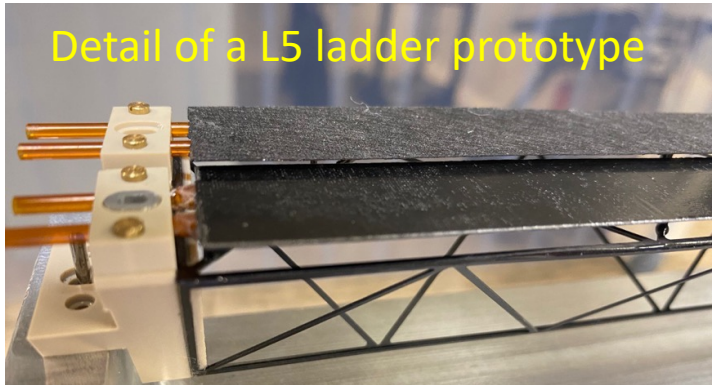
CF support structure (truss), cold-plate with pipes for liquid coolant circulation (neg. pressure),

Chip and Flex circuit for power&signal glued on top

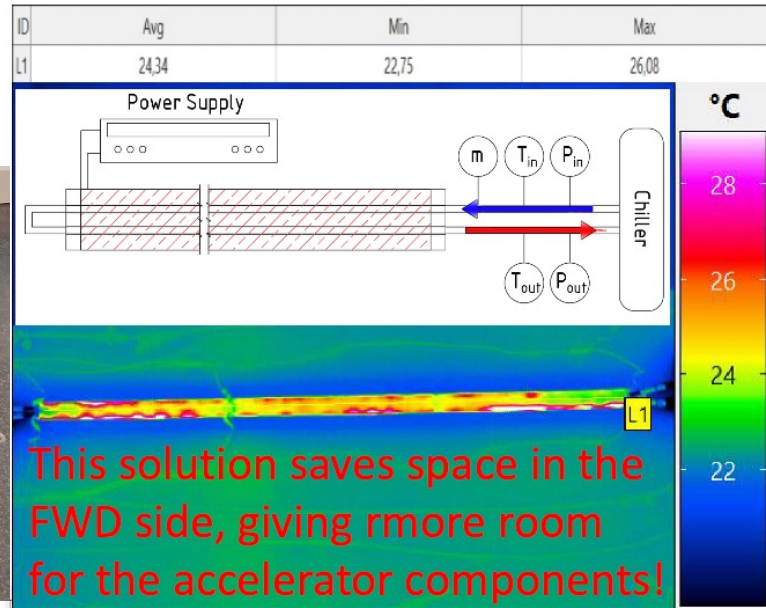


L5 ladder: 70 cm long



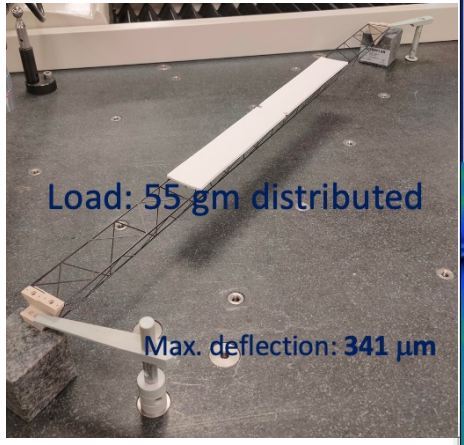


U-turn flow ΔT_{max}= 3.3 °C



Performed mechanical characterization of the L5 prototype:

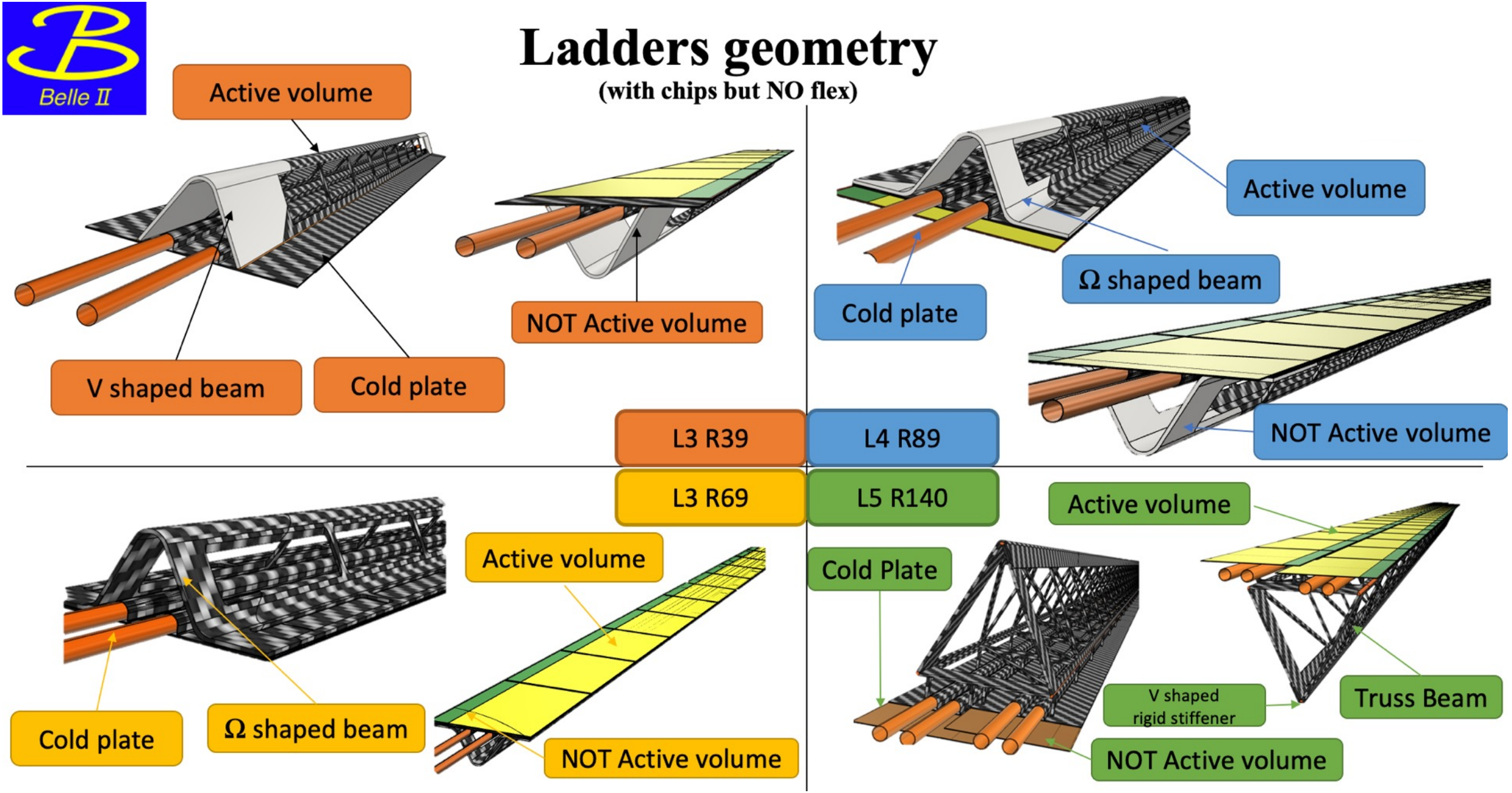
- Distortion: measurements of sagitta (~340 um)
- Vibration: 1st resonance frequency (~250 Hz) (<< earthquake f.)



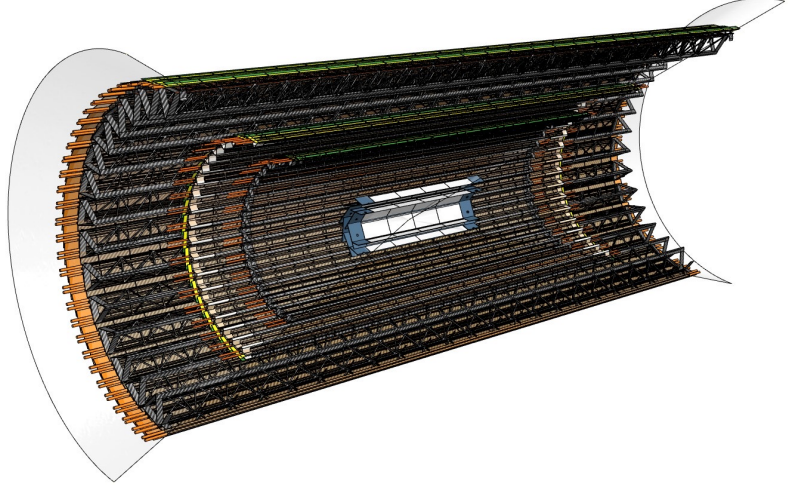
Thermal characterization:

- Used Kapton heaters, inlet (T=10°C) and outlet on one side
- Uniform temperture along the ladder ΔT max=3.3 °C

oVTX


Ladders geometry
(with chips but NO flex)
Active volume
V shaped beam
Cold plate
NOT Active volume
Active volume
Ω shaped beam
Cold plate
NOT Active volume
L3 R39
L4 R89
L3 R69
L5 R140
Active volume
Cold plate
Ω shaped beam
Active volume
NOT Active volume
Cold Plate
Active volume
V shaped
rigid stiffener
Truss Beam
NOT Active volume

Conclusions



- The SuperKEKB collider is planning a major upgrade of the I.R. to reach the design luminosity.

- **All-layer monolithic** vertex detector upgrade (**VTX**) to be installed in LS2 in ~2027:
  - More performant and resilient against higher machine backgrounds
  - Defined target spec's in terms of material budget, spatial resolution and integration time window
  - Baseline chip technology TJ180 nm, evolving from TJ-Monopix2:

  OBELIX: First steps towards a Belle II CMOS sensor, **submission in Q4 2023/Q1 2024**

- Realization of prototypes of inner/outer layers ongoing, submitted to the mechanical, thermal and electrical characterization.

- In the finalization phase the CDR of the Belle II Upgrade.