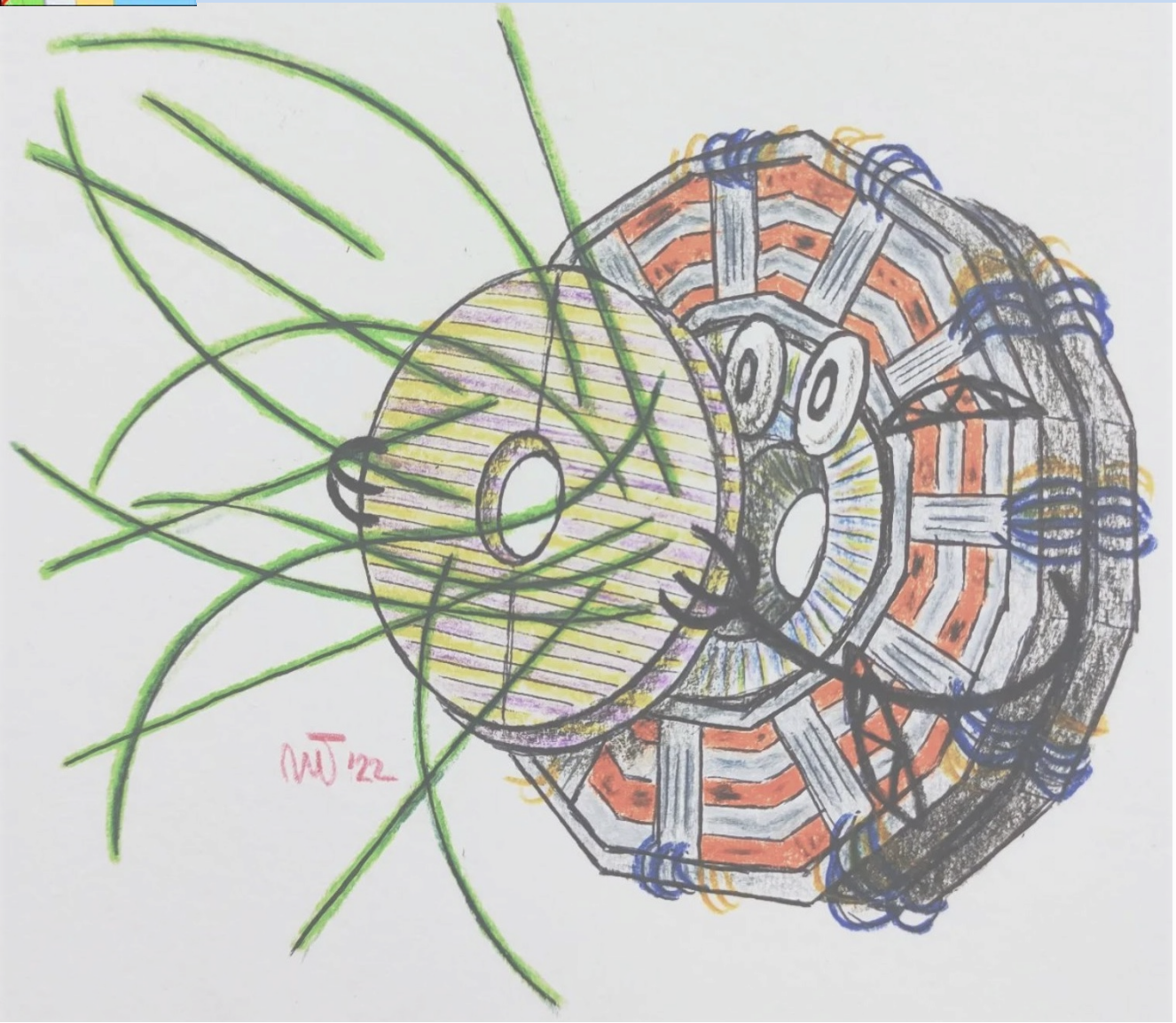
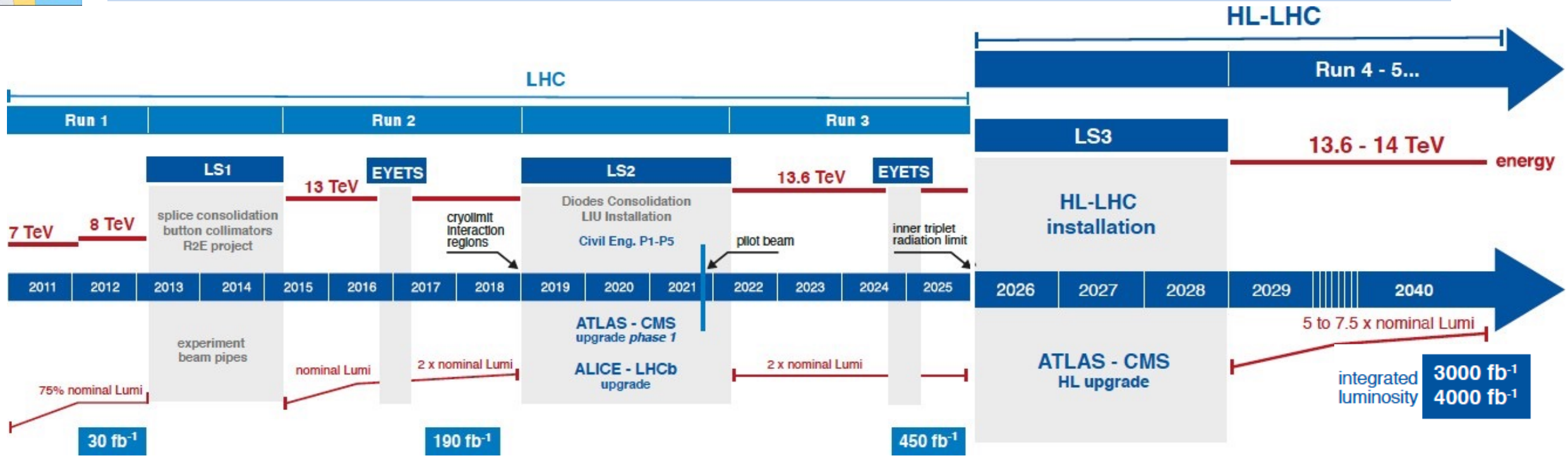
TOPICAL SEMINAR ON INNOVATIVE PARTICLE
AND RADIATION DETECTORS (IPRD23)
Siena 25-29th September



Low Gain Avalanche Detectors for Precision Timing in the CMS MTD Endcap Timing Layer

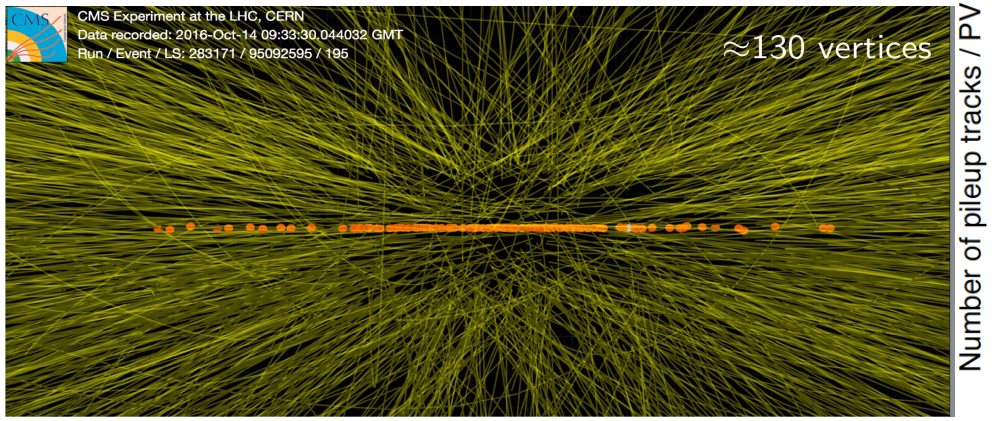
Marco Costa (INFN &University of Torino)
on behalf of CMS collaboration

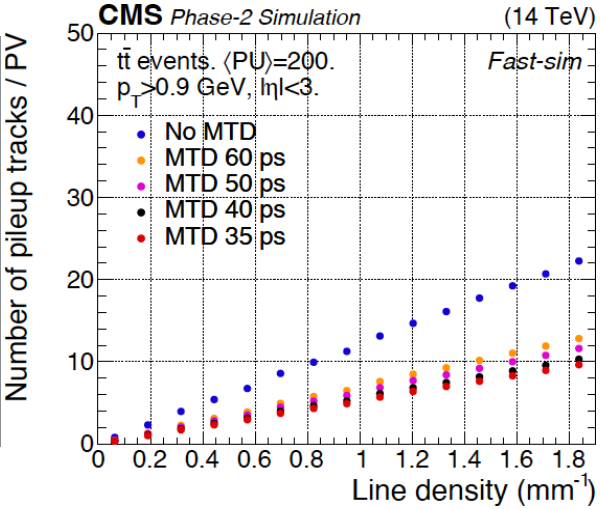
High-Luminosity LHC

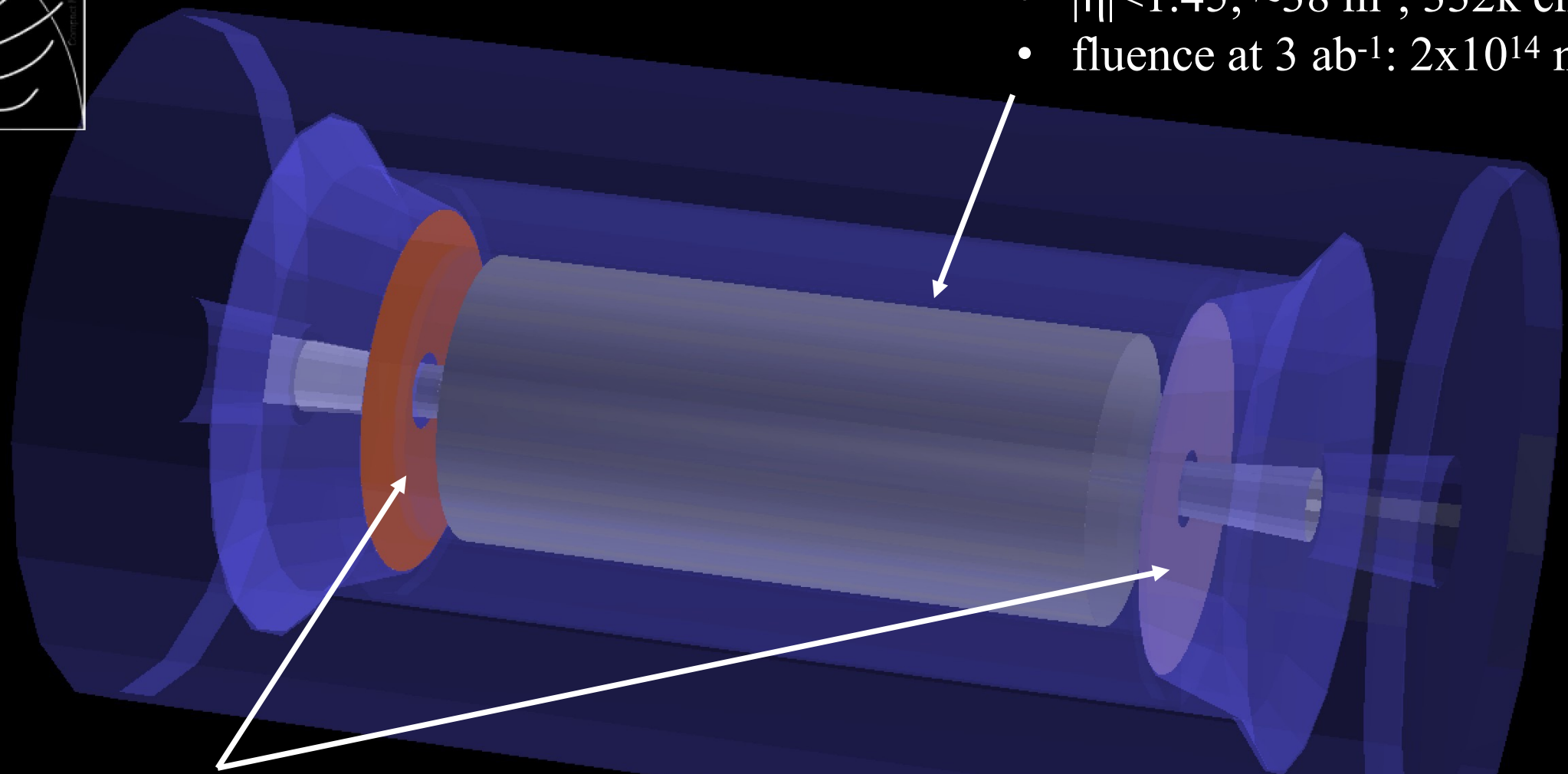


The HL-LHC will have x3-4 instantaneous and x10 integrated luminosity, requiring **detector upgrades**

- To deal with enhanced pileup interaction and radiation damage levels at the HL-LHC
- To improve the experiment for better discovery potential and/or measurement precision







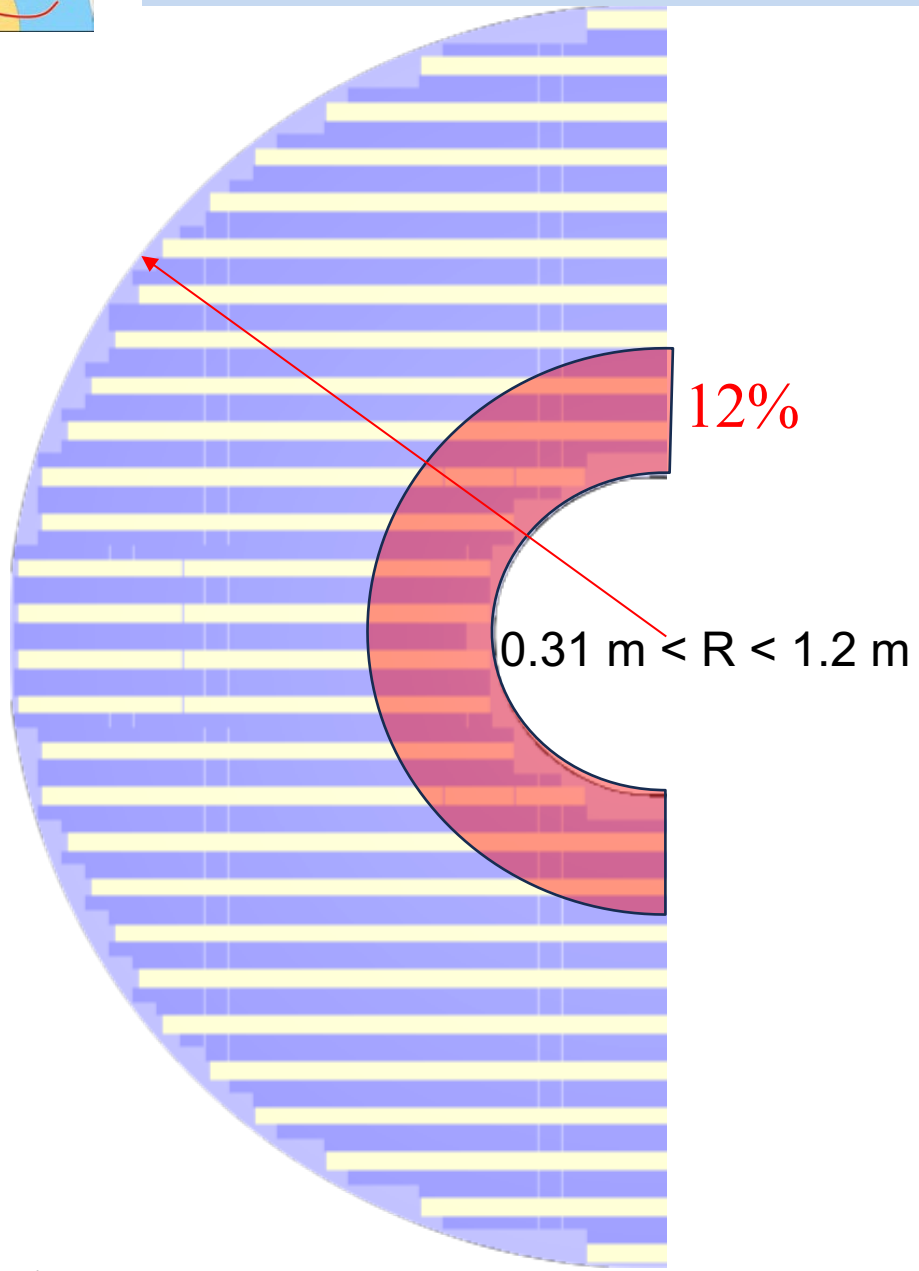
BTL: LYSO bars + SiPM

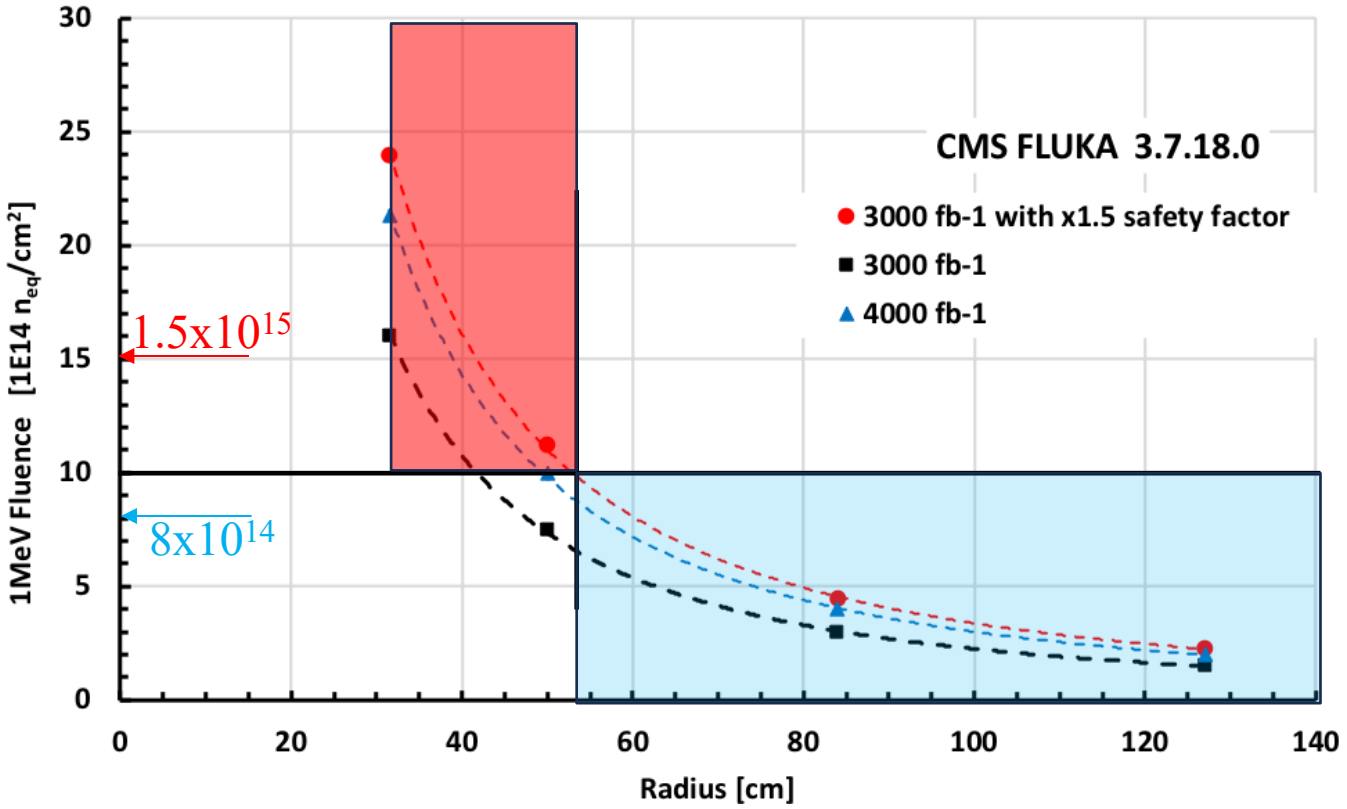
- $|\eta|<1.45$; ~38 m^2; 332k channels
- fluence at 3 ab^{-1}: $2x10^{14}$ n_{eq}/cm^2

This talk: ETL: Si with internal gain (LGAD)

- $1.6<|\eta|<3.0$; ~14 m^2; ~8.5M channels
- fluence at 3 ab^{-1}: ~$2x10^{15}$ n_{eq}/cm^2

ETL Requirements

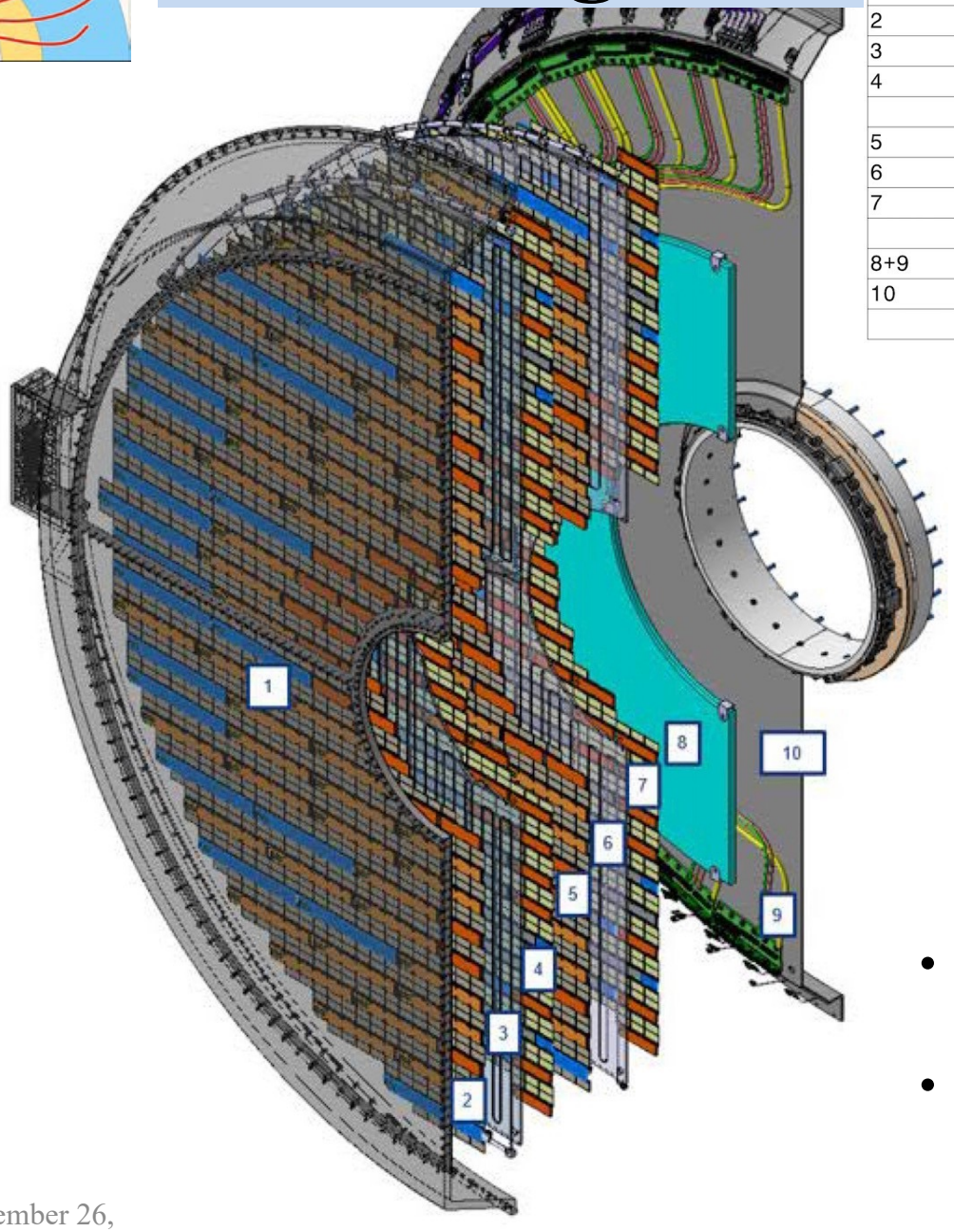


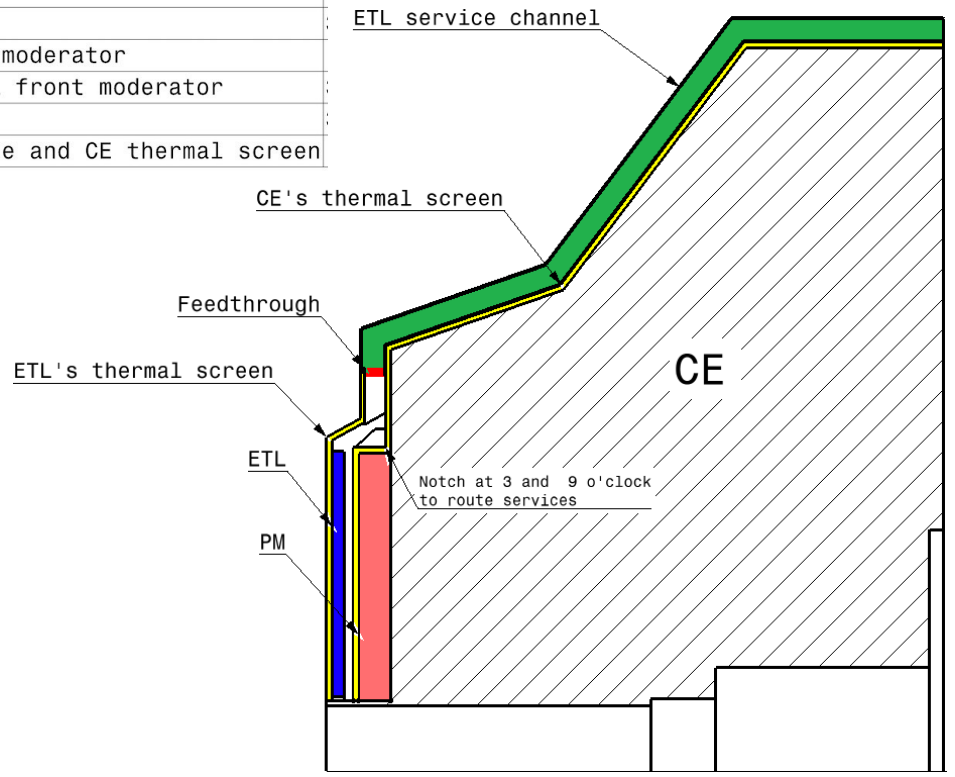


- **Time resolution**: <35 ps per track at the beginning of HL-LHC
- **Fill-factor** (ratio of active and total detector surface): >95%
- **Low occupancy**: <0.1% at low η, 1% at highest η
- **Radiation tolerance**: up to 1.7×10^{15} n_{eq}/cm^2
  - Only 12% of surface will reach higher fluences than 1×10^{15} n_{eq}/cm^2

ETL Design

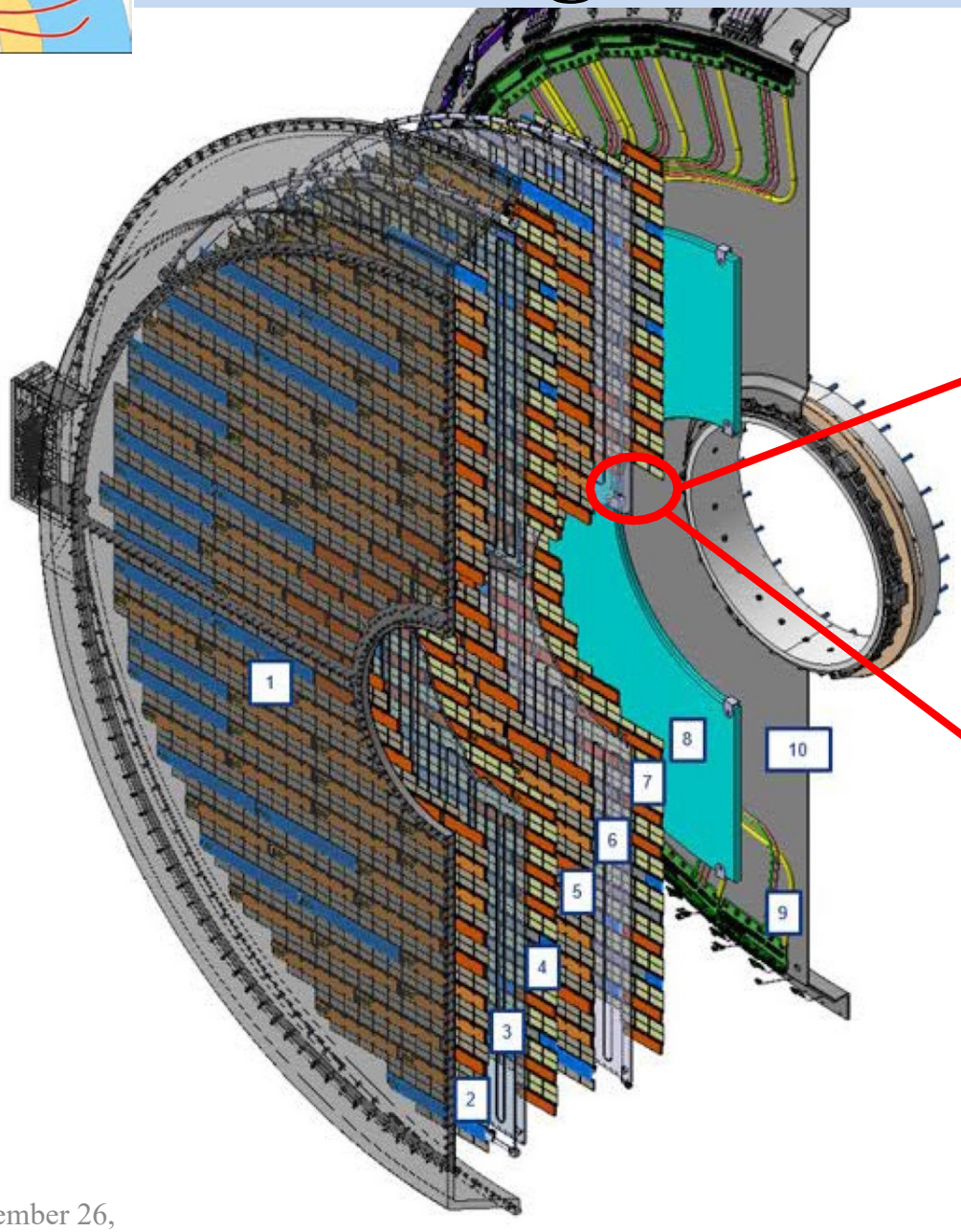
Element	
1	Thermal screen
	Gap between thermal screen and Face 1
2	Face 1 - active layer
3	Front disc
4	Face 2 - active layer
	Gap between Face 2 and Face 3
5	Face 3 - active layer
6	Back disc
7	Face 4 - active layer
	Gap between Face 4 and ETL front moderator
8+9	Patch panels 0 + cables [9] + ETL front moderator
10	ETL back support plate
	Gap between ETL back support plate and CE thermal screen





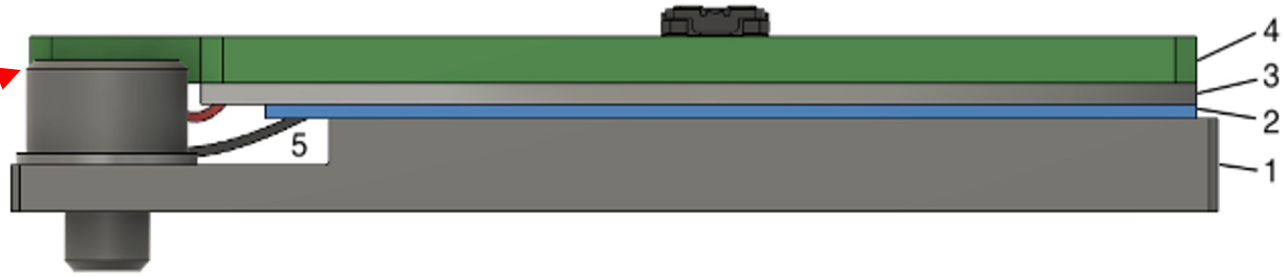
- Two ETL disks on each side allowing up to 2 measurements per track: <50 ps per hit → <35 ps per track
- Independent volume isolated and operated separately from HGCAL: stageable, serviceable, maintainable

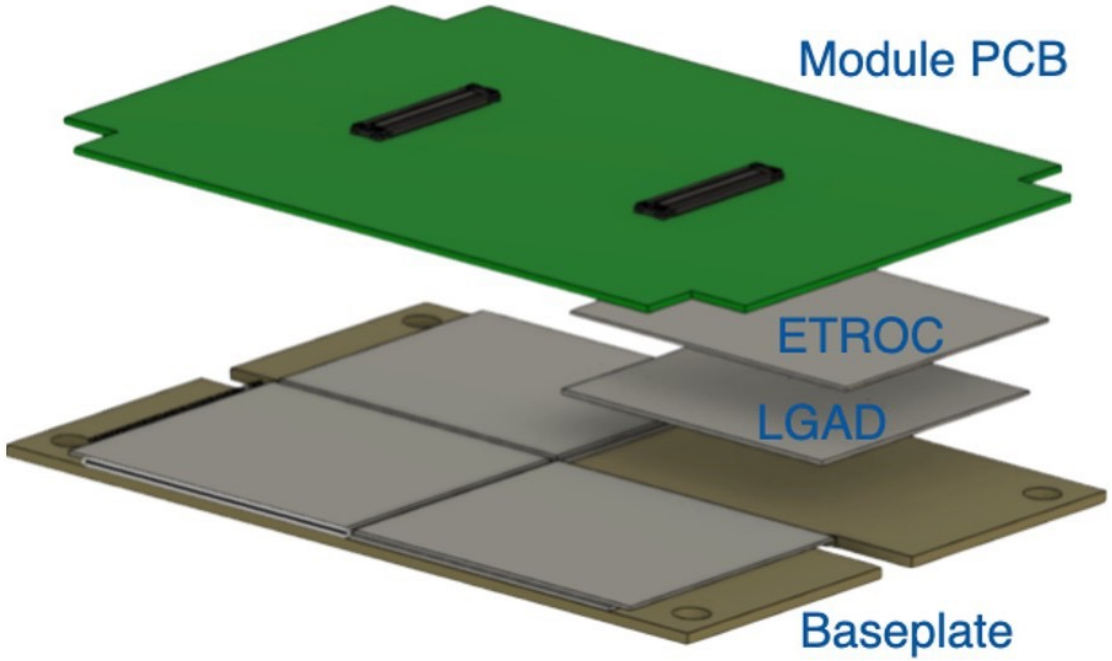
ETL Design



Module = fundamental Unit

1: Base plate (AlN)
2: LGAD
3: ETROC
4: PCB
5: Wire bonds
6: Board-to-board connector

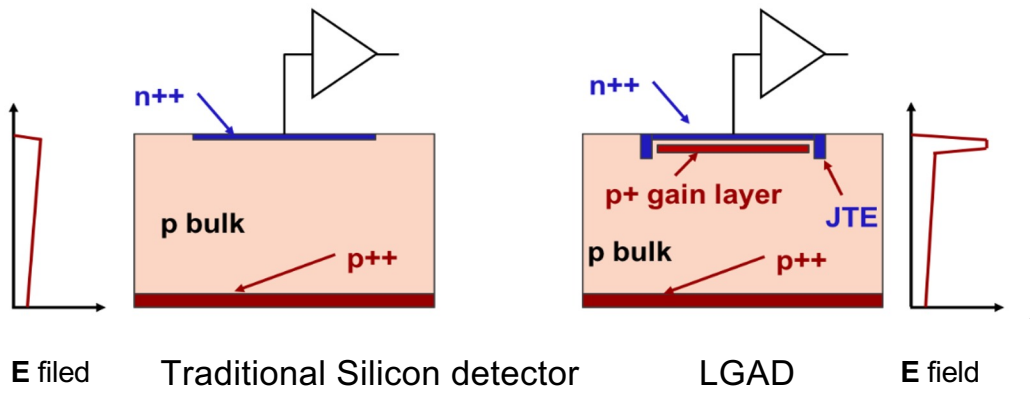


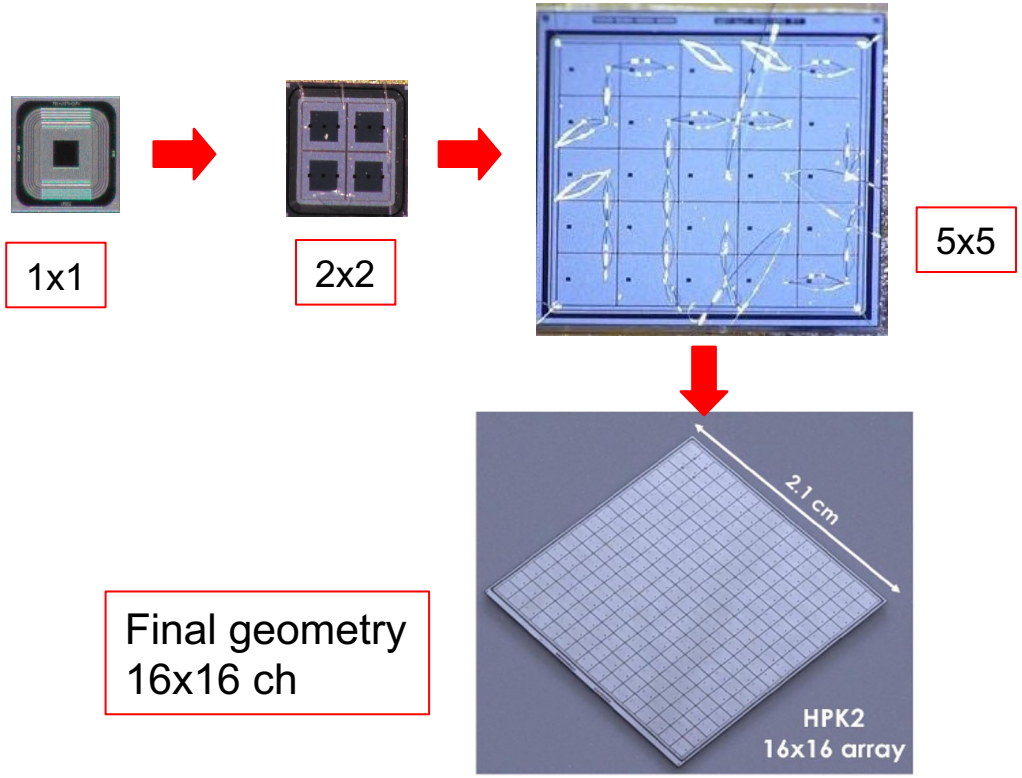


ETL Sensor technology

- ETL will be instrumented with Low Gain Avalanche Diode (LGAD) sensors optimized for timing measurements at LHC
- LGADs has an internal gain layer, which is a highly-doped thin layer near the p-n junction, where a high local electric field producing charge multiplication with a moderate gain factor of 10-30 to maximize signal/noise ratio

- **ETL sensor requirements:**
  - Sensor size: 50 µm-thick, 16×16 pads array with 1.3×1.3 mm^2 pads, whose size is determined by occupancy and read-out electronics
  - Low leakage current to limit power consumption and noise
  - Large and uniform signals: >8 fC pre-radiation, >5 fC after highest irradiation point
  - Minimized "no-gain" area: inter-pad distance < 50 µm
- From the beginning to the end of HL-LHC lifetime, sensors expected to:
  - Achieve single hit time resolution < 50 ps when coupled to the ASIC (30-40 ps for the bare sensor)
  - Deliver > 8 fC of charge
- LGADs suited for radiaton: unchanged performance up to 1.5E15 n_{eq}/cm^2, and then slight slow degradation
- Worked with multiple vendors to develop prototype sensors and optimize their designs for ETL

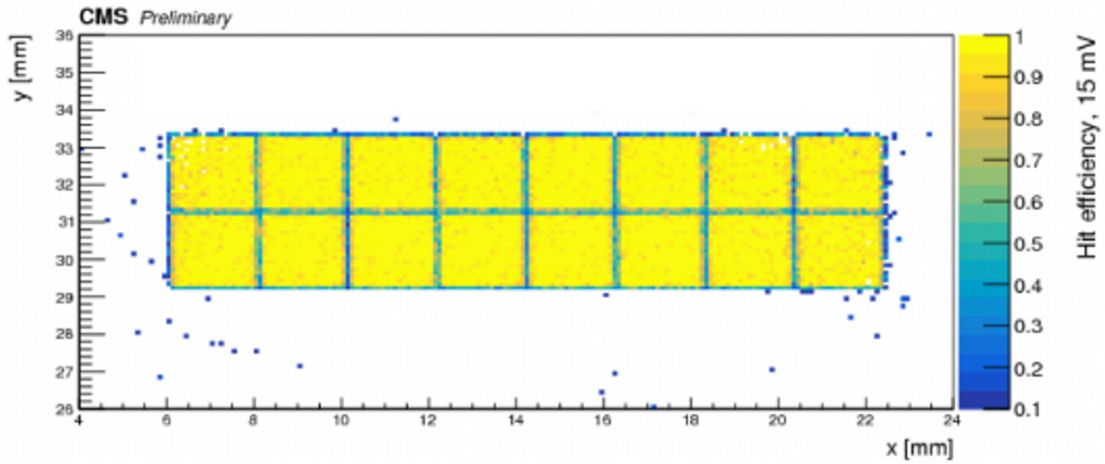




Final geometry
16x16 ch

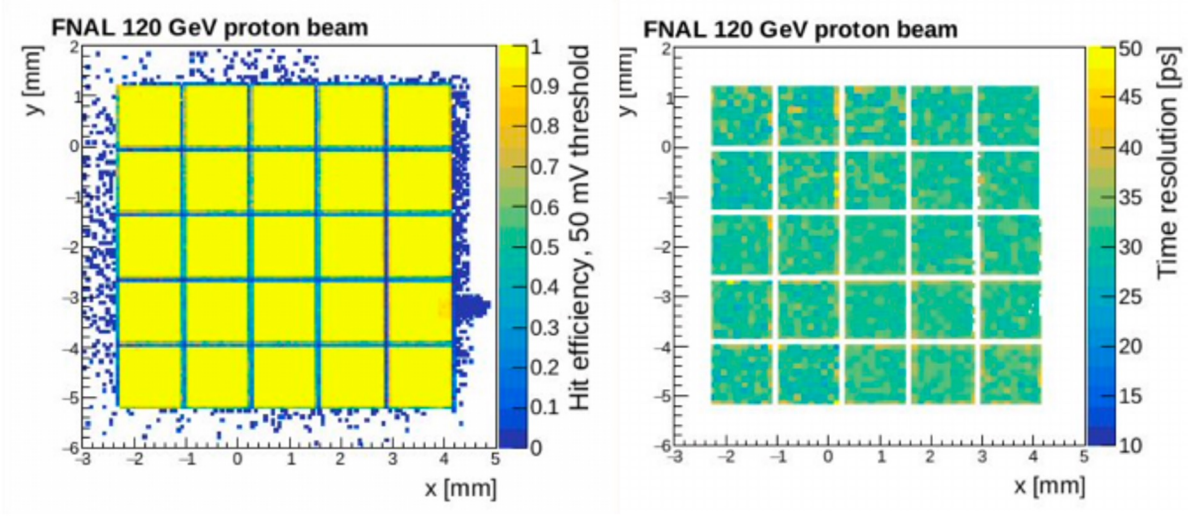
Performance of LGADs

FNAL Test Beam Results

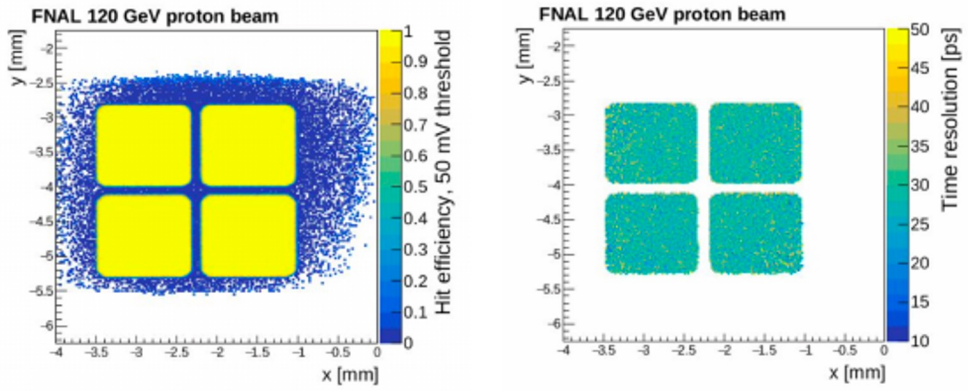


FBK 2×8 array (first prototype sensor production)

Irradiated 8e14 n_{eq}/cm^2



Non-irradiated FBK 5x5 array



Non-irradiated IHEP IME 2x2 array

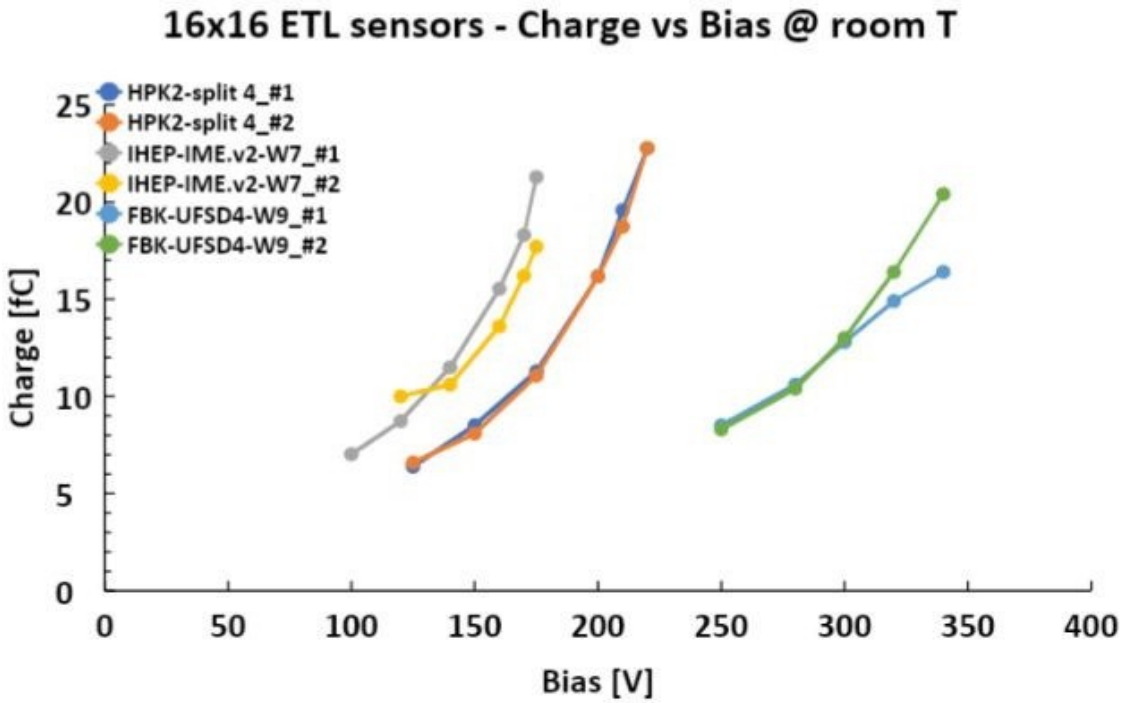
- Maps measured at FNAL
- Resolution for non irradiated sensors ~ 30 ps
- Hit efficency
  - reaches ~ 100 % for non irr.
  - reaches ~ 99 % for irr.

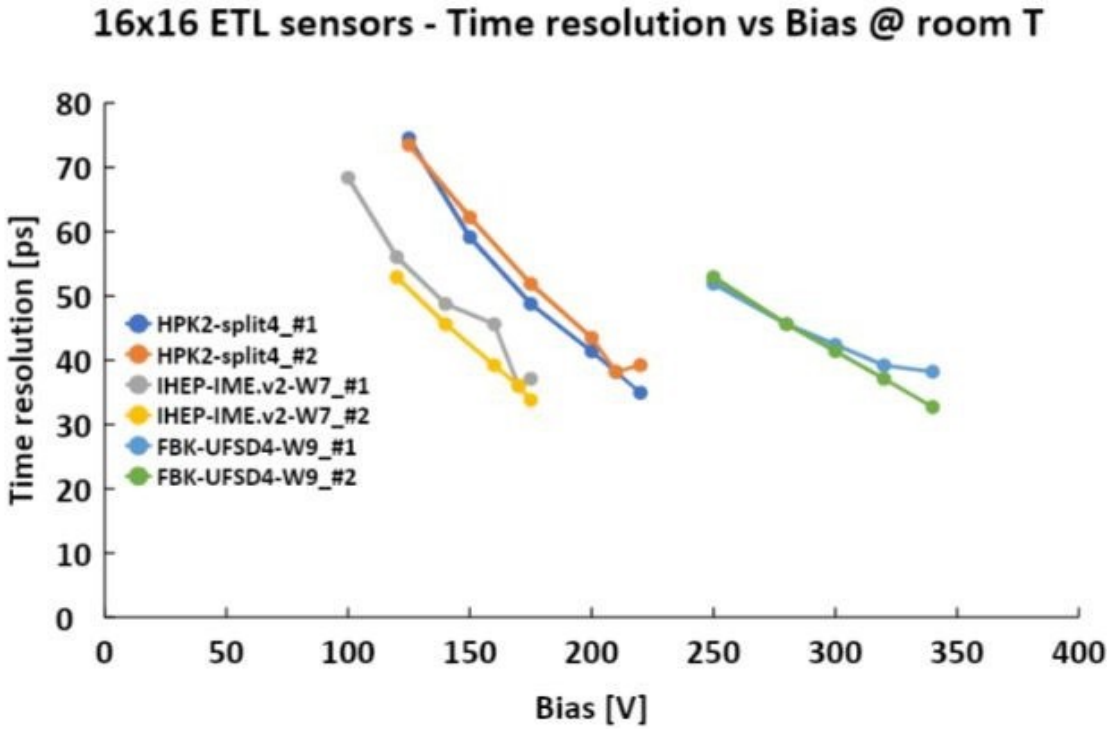
Performance of LGADs

DESY Test Beam Results

Non irradiated sensors

Measurement at room temperature





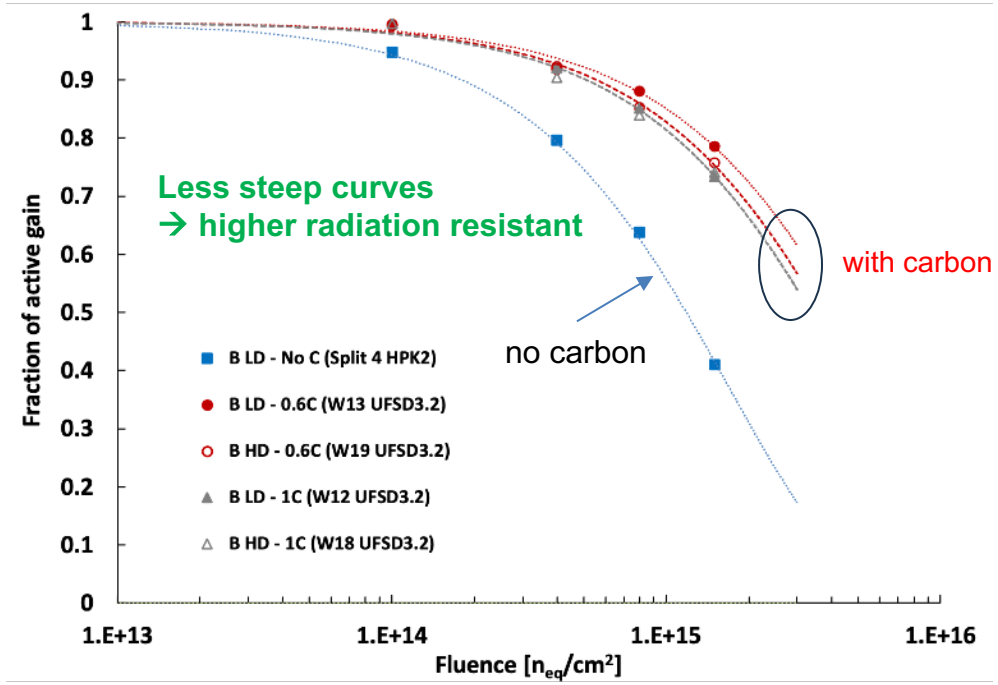
All sensors tested reached a time resolution in the 35-40 ps range, delivering >15 fC of charge

Data analysis by M. Ferrero, L. Lanteri and F. Siviero

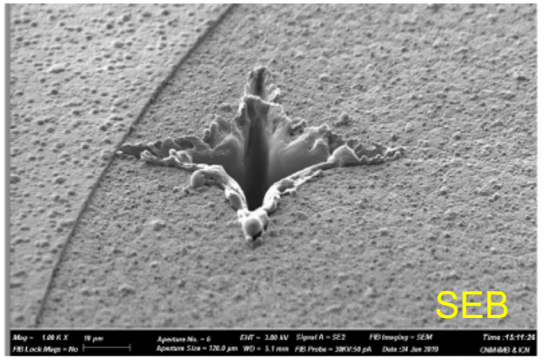
LGADs: Radiation affected performance

- There are two major radiation effects that affect the performance:
  - **Gain layer depletion**
  - **Single Event Burnout (SEB)**

- **Gain layer** can be "recovered" by increasing the bias V_{bias} (see following slides) and using carbon to mitigate the acceptor removal

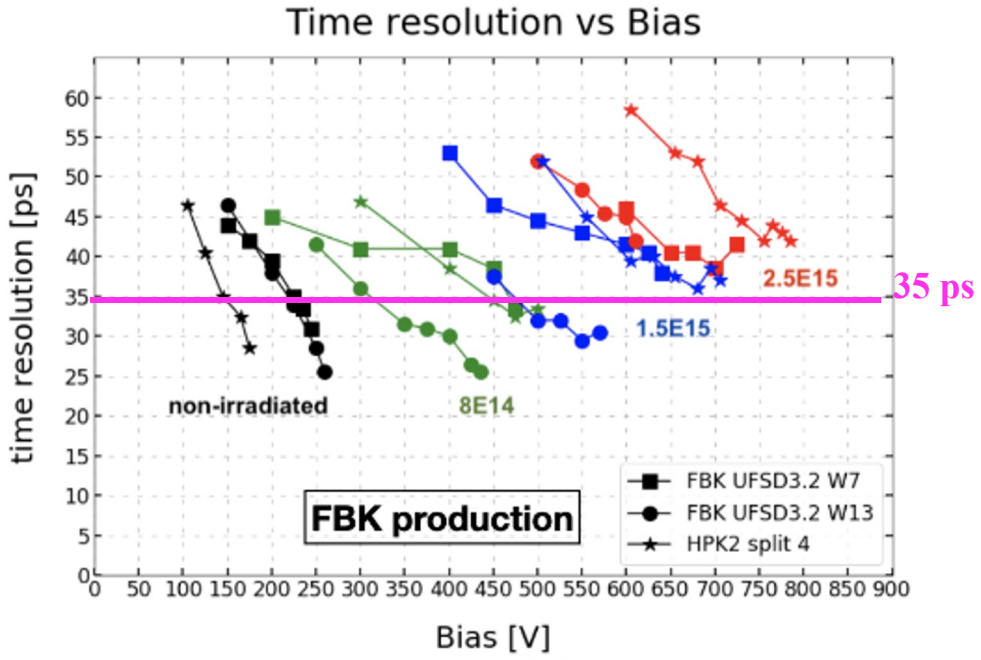


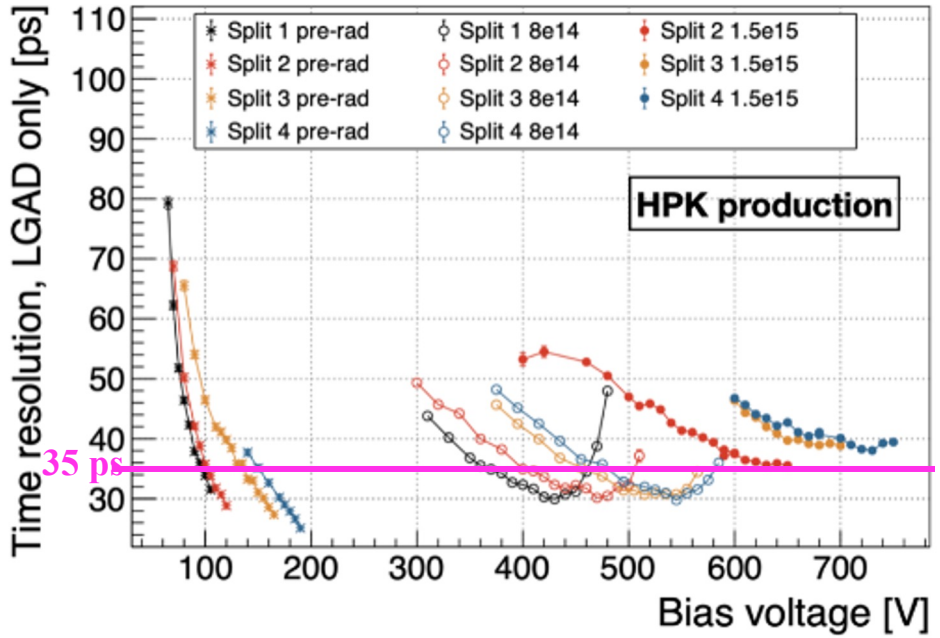
- **SEB** can be avoided by carefully choosing V_{bias} operation range (see following slides)
  - *An incoming particle releases a lot of energy over a small volume, 5-10 μm*
  - *The local electric field is high enough to create a conductive channel*
  - *The energy stored in the sensor capacitance discharges burning the sensor*



Performance of LGADs

- Timing resolution measurements on **Irradiated Sensors** in Torino and at Fermilab
  - Using beta-source setups ^{90}Sr or dedicated TB's
  - Very fast low noise electronic
  - Temperature -25 °C
  - For different fluencies

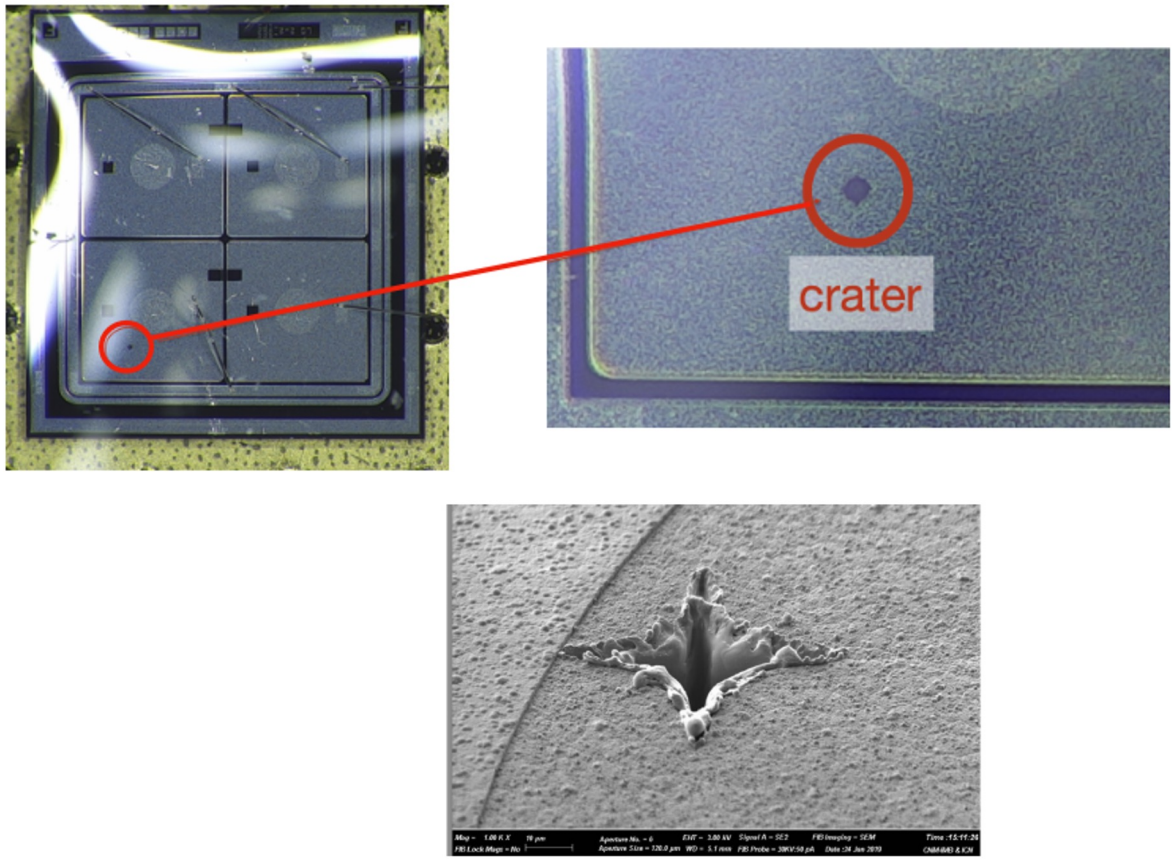


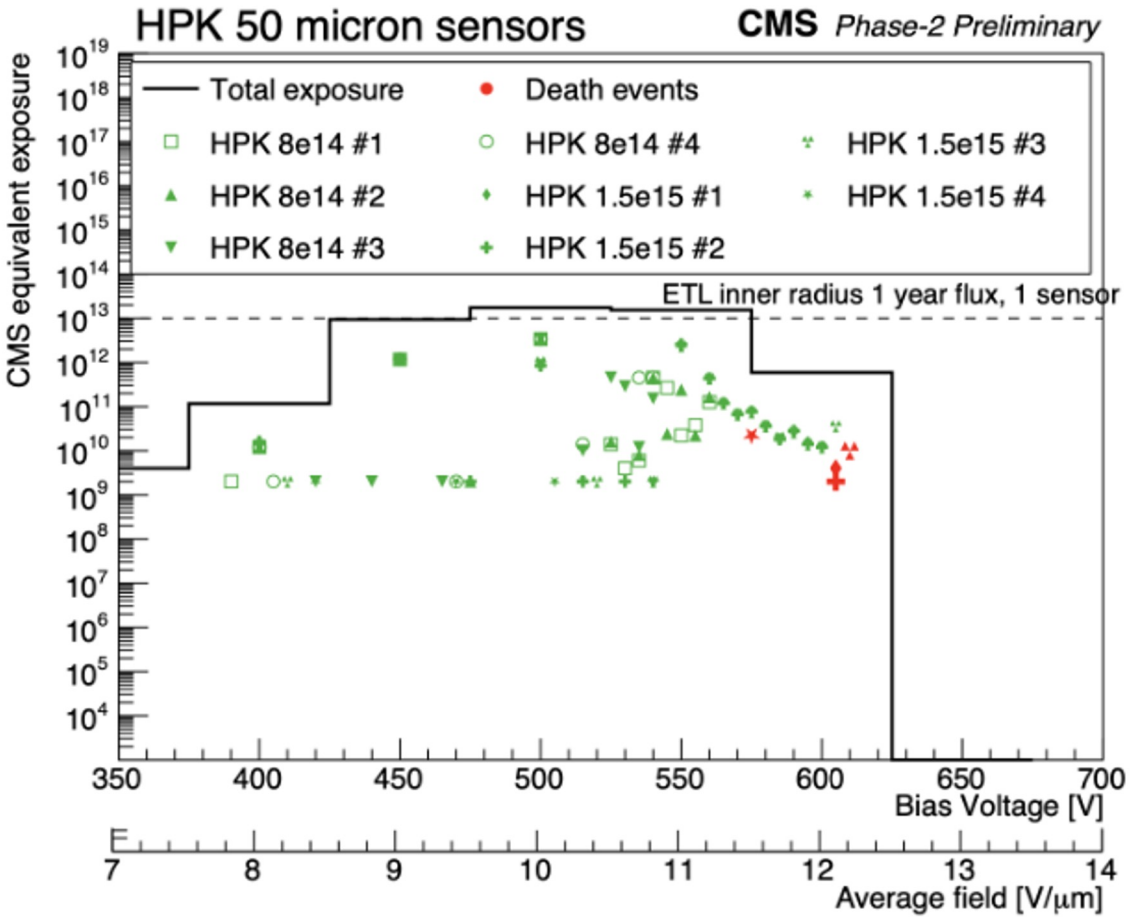


- Time resolution between 35ps and 40ps
- Good agreement between TB and β-measurements

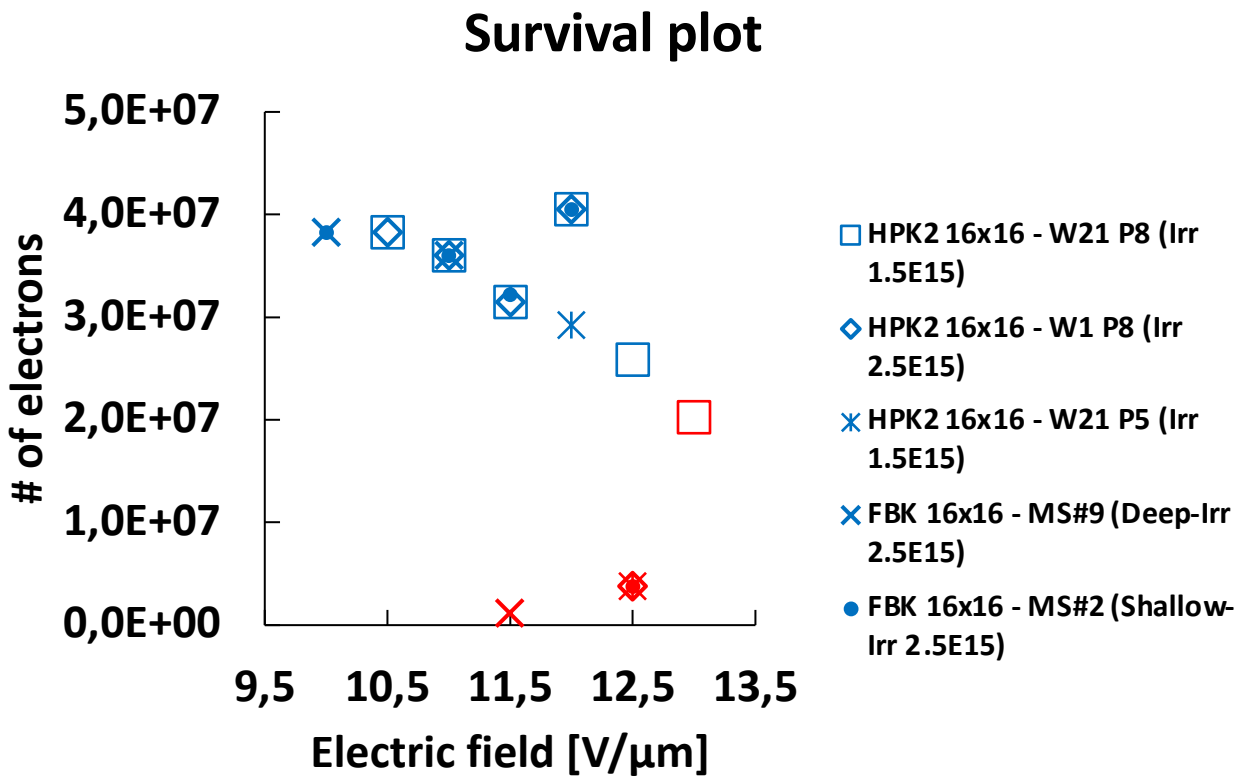
FNAL TB: Single Event Burnout on 2x2 devices

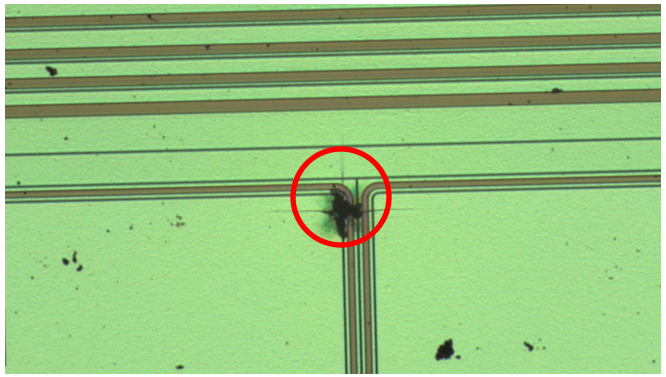
- High-rate test beam at FNAL demonstrate survival of irradiated LGADs at > 11 V/μm under a flux corresponding to ~1 year running for the sensors in ETL inner region





DESY TB: SEB results on 16x16 devices





Analysis by Marco Ferrero

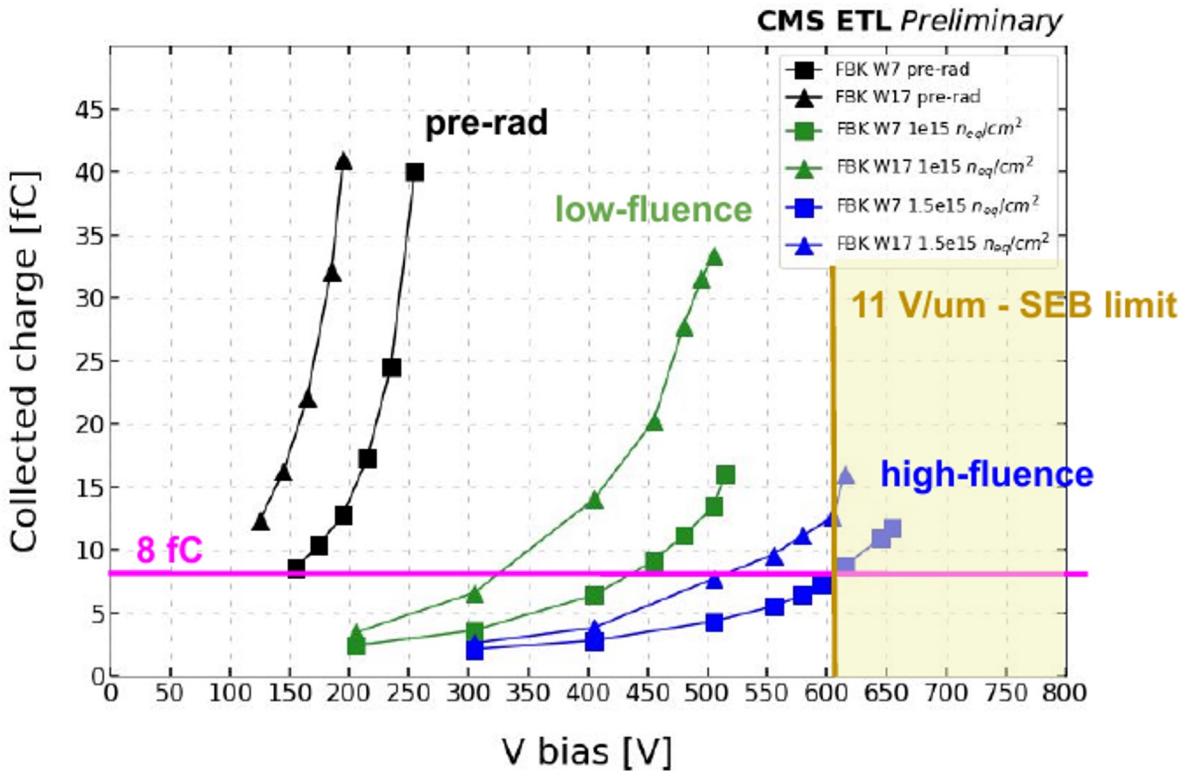
- Six HPK and FBK large devices (irradiated at 1.5 $\cdot 10^{15}$ and 2.5 $\cdot 10^{15}$ n_{eq}/cm^2 tested during SEB test beam campaign.
- Large sensors biased to generate bulk electric field above 10 V/µm
- All tested sensors survived below the bulk electric field 11.5V/µm
- For all tested sensors SEB happened between 11.5 and 13 V/µm
- Optical inspection found craters in each sensor burnt-out

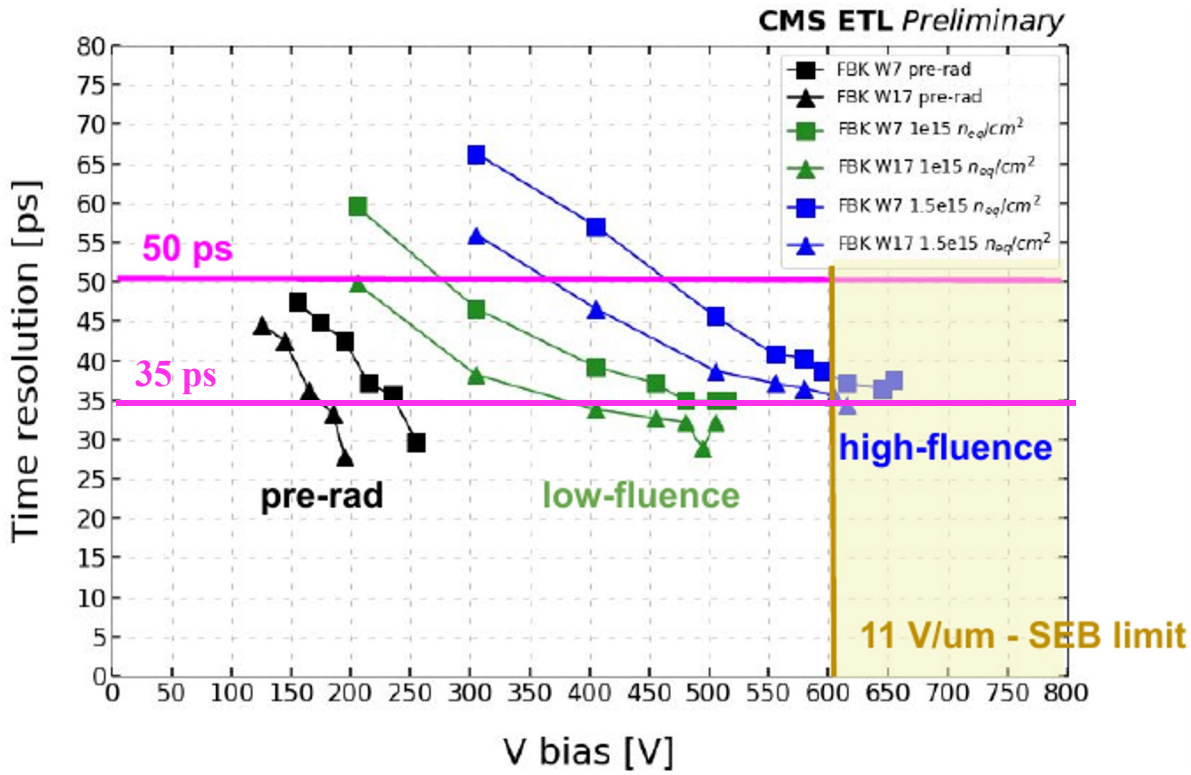
→ craters have typical cross shape due to SEB

→ Most of craters are located where there is the metal contact and n-deep implant

Performance of LGADs

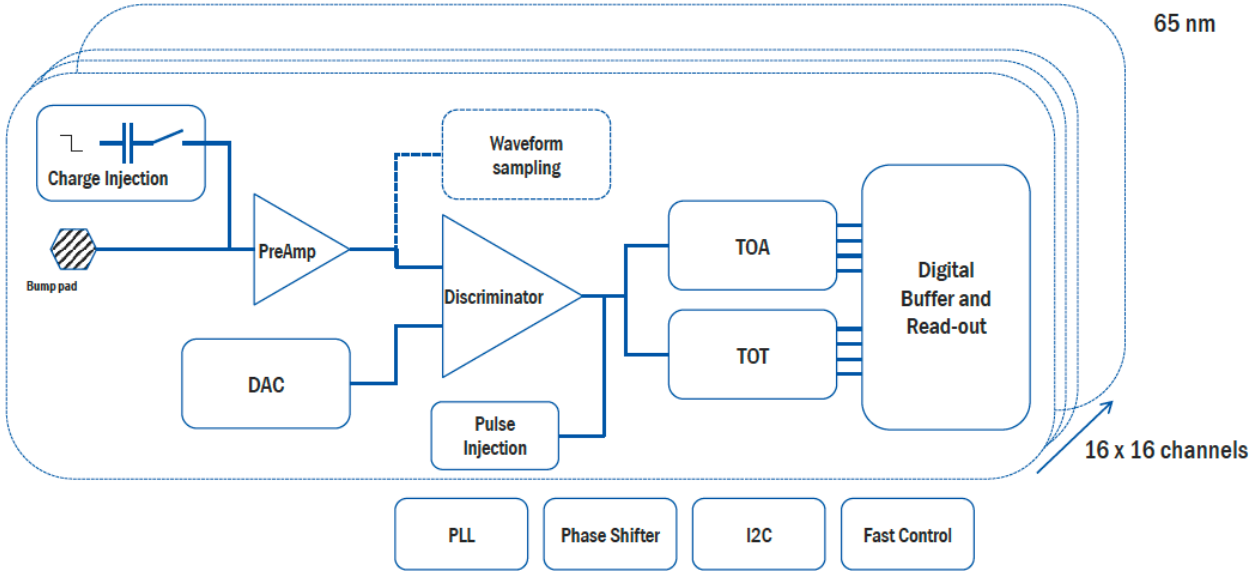
Example of Market Survey sample performance: FBK 55 micron thick sensors tested with the β-source setup

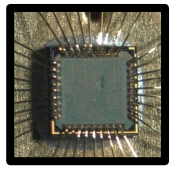


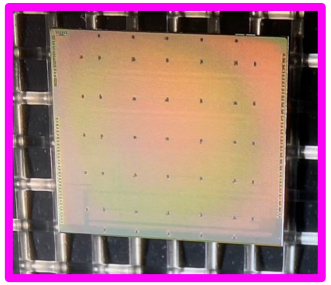


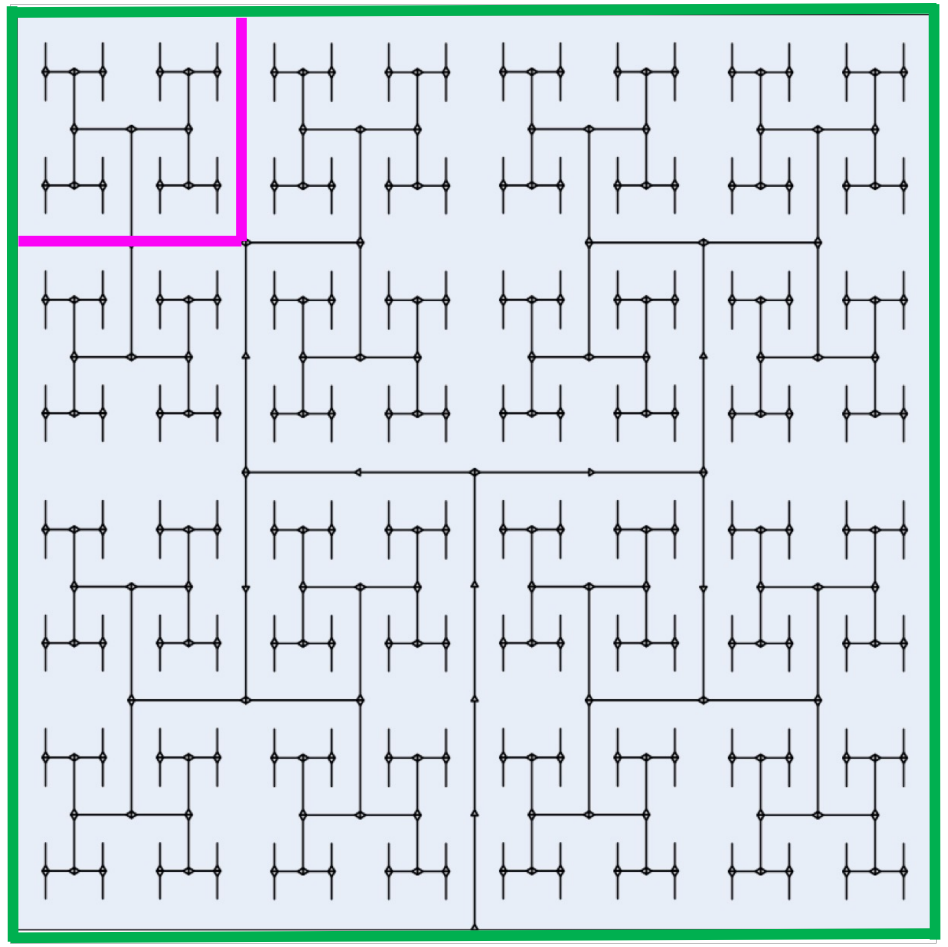
Overall time resolution and delivered charge of bare sensors within requirements

ETL Readout Chip (ETROC)









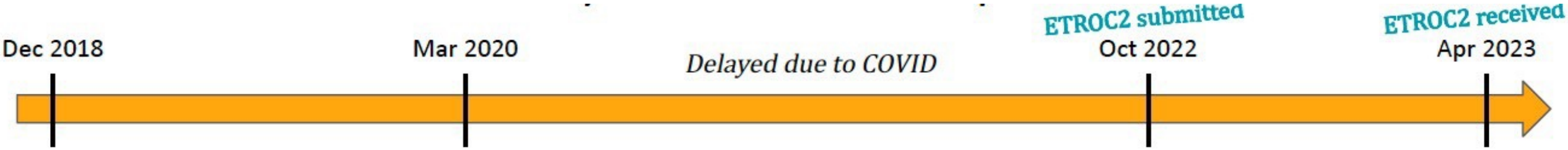
- **Delicate balance act from:**
  - **Low noise & fast rise time**

$$\sigma_{jitter} \sim \frac{e_n C_d}{Q_{in}} \sqrt{t_{ri}} < 40\ ps$$

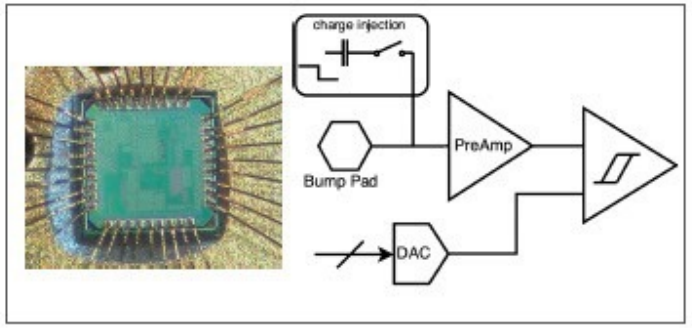
  - **Power budget: 1 W/chip, ~4 mW/channel**
- **ETROC innovation:**
  - **Very low power TDC, using simple delay cells with self-calibration**

- ✓ **ETROC0 : single analog channel**
- ✓ **ETROC1: with TDC and 4x4 clock tree**
- ✓ **ETROC2: 16x16 full size full functionality**
- D **ETROC3: 16x16 preproduction chip**

ETROC

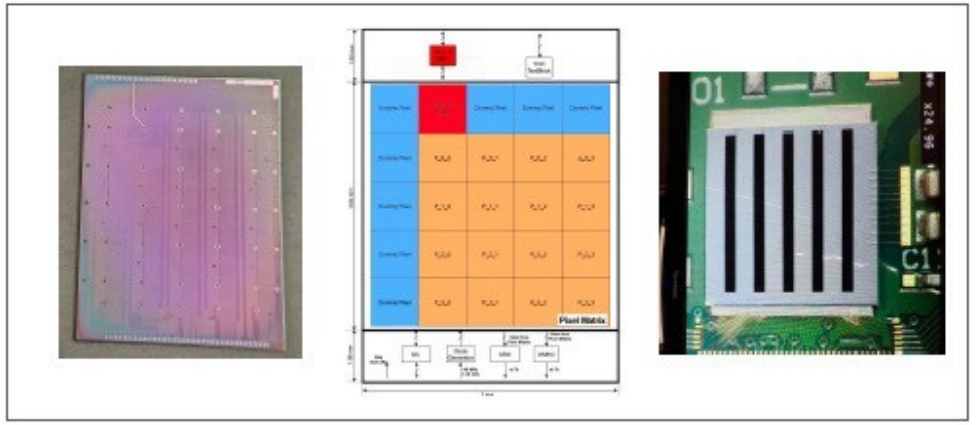


ETROC0 (1x1)



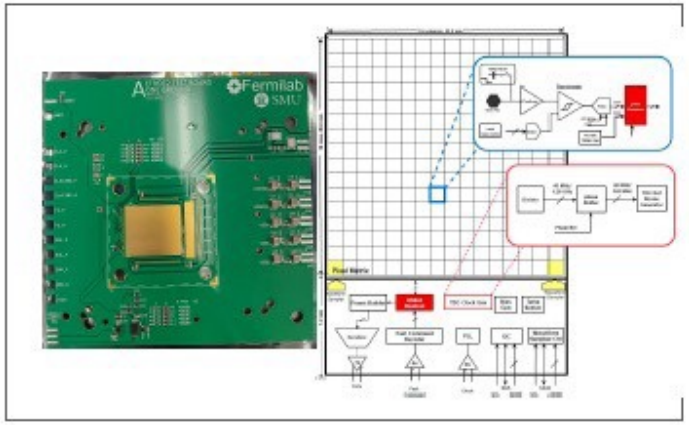
- Analog front-end only
- Wire-bonded with LGAD sensor reached ~33 (30) ps time resolution per hit with preamp. waveform at room temp. (-25 degree C)
- Passed 100 Mrad TID

ETROC1 (4x4)



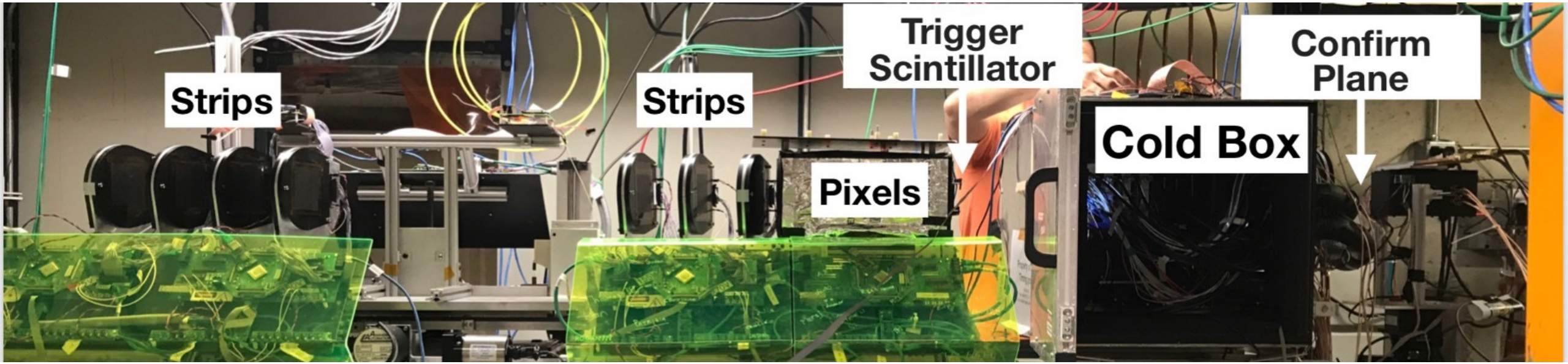
- Added low-power TDC and 4x4 H-tree for clock distribution
- Bump-bonded with LGAD sensor reached ~42 ps time resolution per hit with TDC data

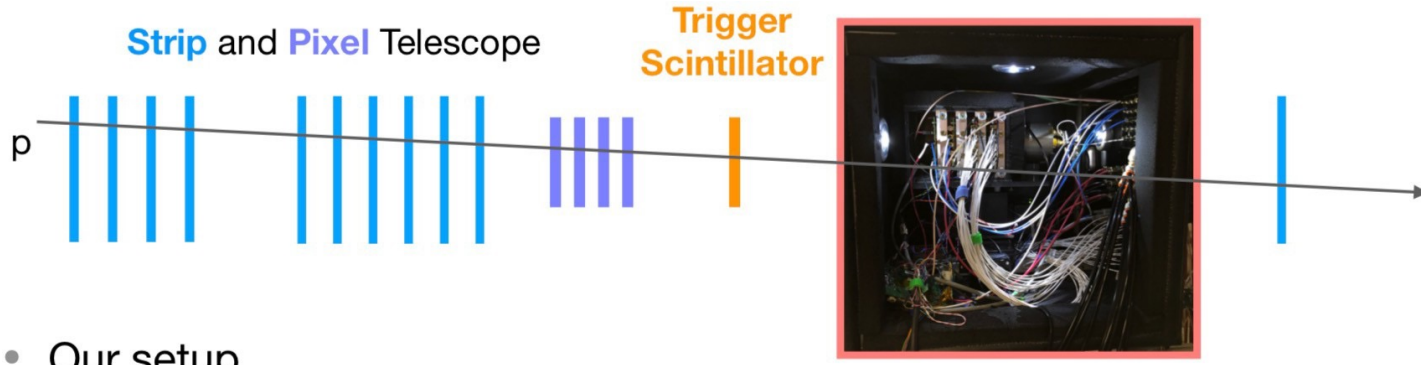
ETROC2 (16x16)



- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator

LGAD+ETROC0 – Test Beam Results



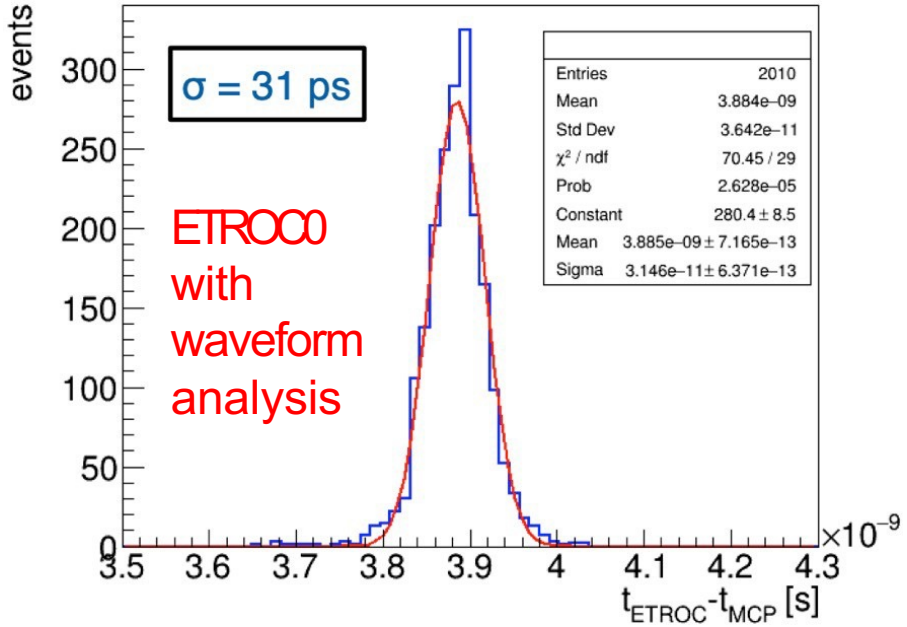


- Our setup
  - Independent scintillator provides trigger
  - Telescope provides proton track
  - Oscilloscope saves waveforms
  - Study Δt(LGAD,MCP)

Cold box

LGAD boards on cooling blocks

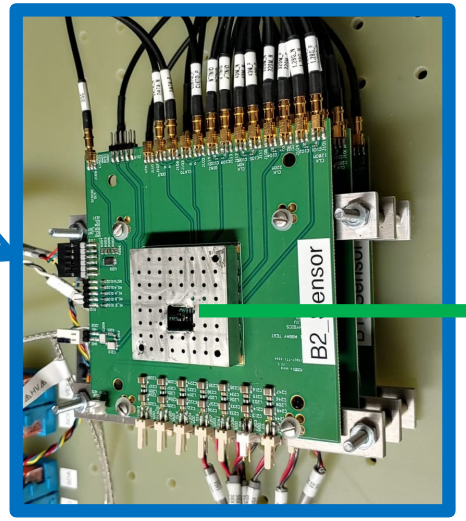
MCP (Photek) time reference

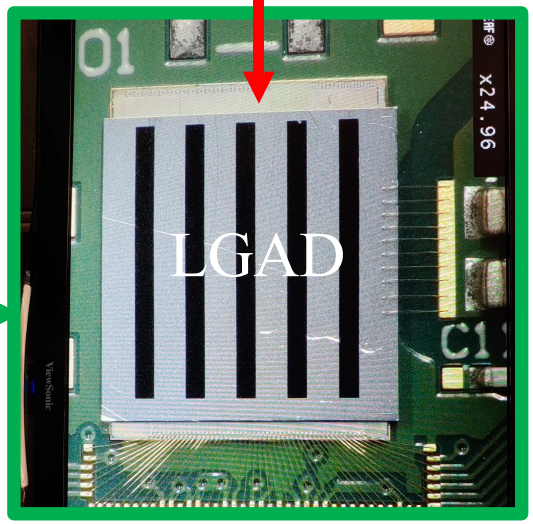


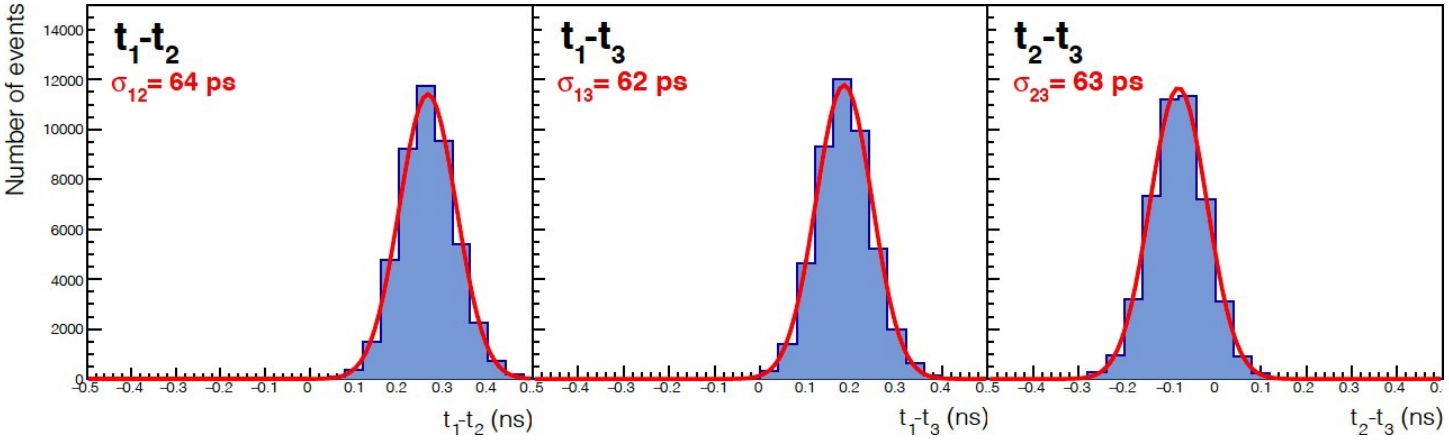
LGAD+ETROC1 – FNAL Test Beam Results

ETROC1 Test Board

ETROC1







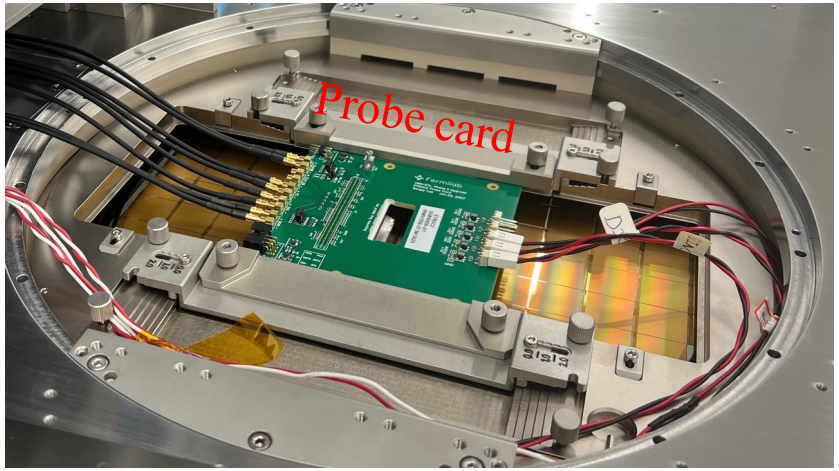
LGAD+ETROC1 resolution is from TDC digital outputs

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$

~42 -46 ps

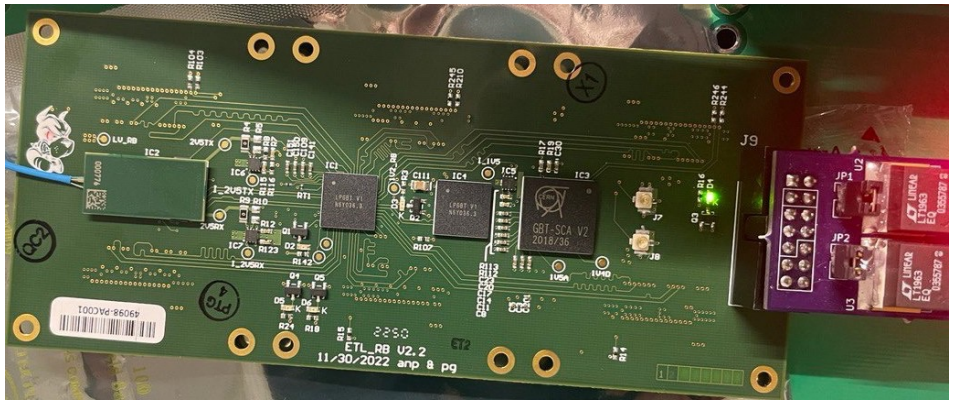
ETROC2

- ✓ Initial check on power consumption; detailed study later
- ✓ I2C communication to global circuit and individual pixels
- ✓ Phase-Locked Loop
- ✓ Automatic threshold calibration
- ✓ Digital readout with pattern generator
- ✓ Fast command
- ✓ Initial test with charge injection; detailed check on-going
- ✓ Initial Total Irradiation Dose test; detailed check on-going
- ✓ Initial waveform sampler test; detailed check on-going
- ✓ Initial test of ETROC2+LGAD; detailed check on-going, beam test planned in Sept. (SPS), Dec. (DESY) and Jan-24 (FNAL)
- Wafer probe test started
- Single Event Upset test being planned



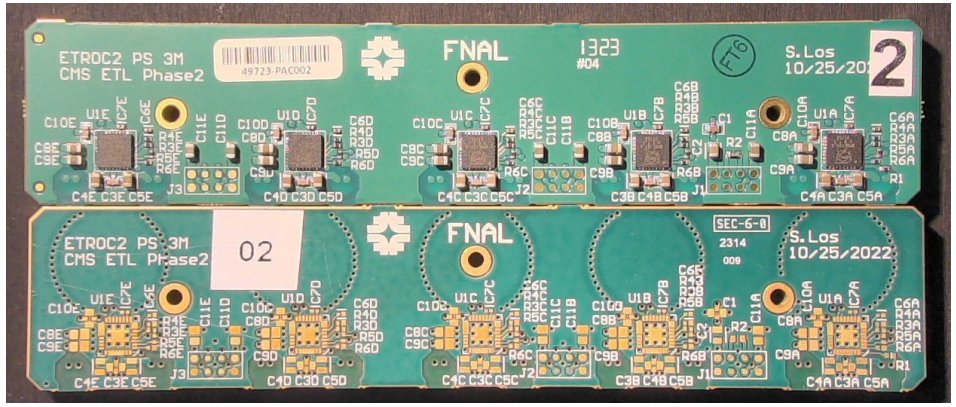
Readout and Power Boards

- Prototype V2 Power board
  - Efficiencies ~ 65-67%
- Prototype V2 Readout board
  - LpGBTv1+VTRX

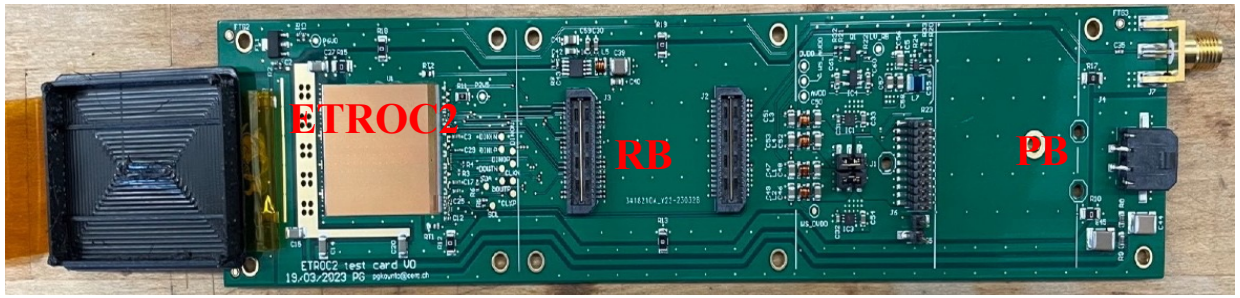


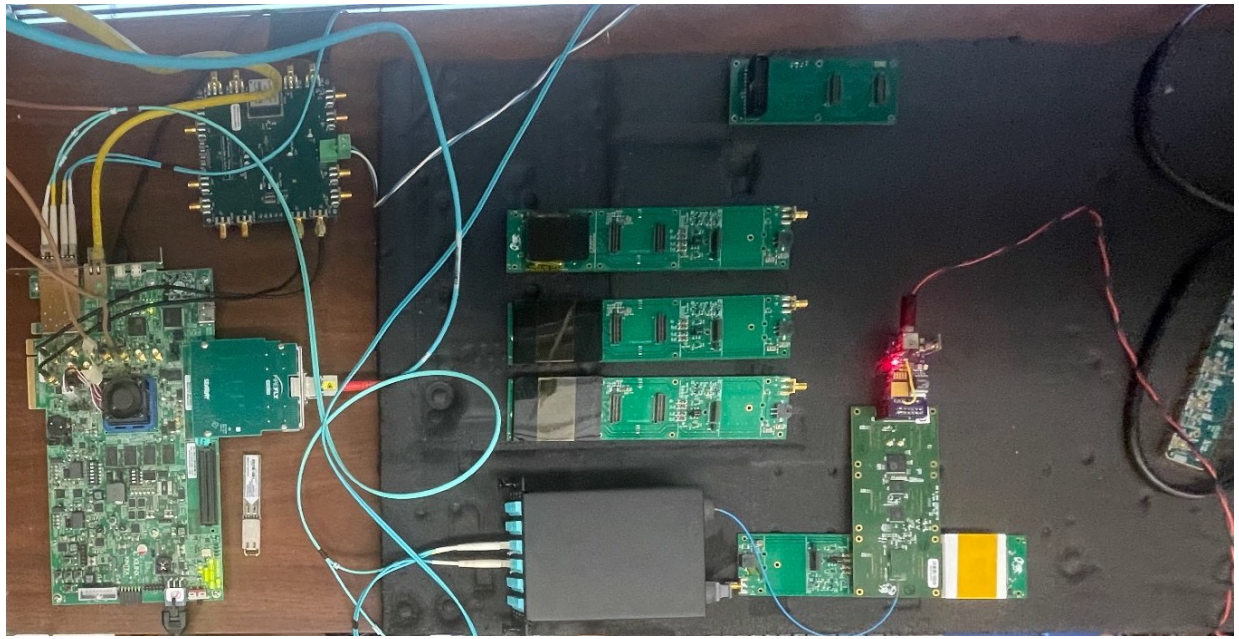
Pactron

Saturn

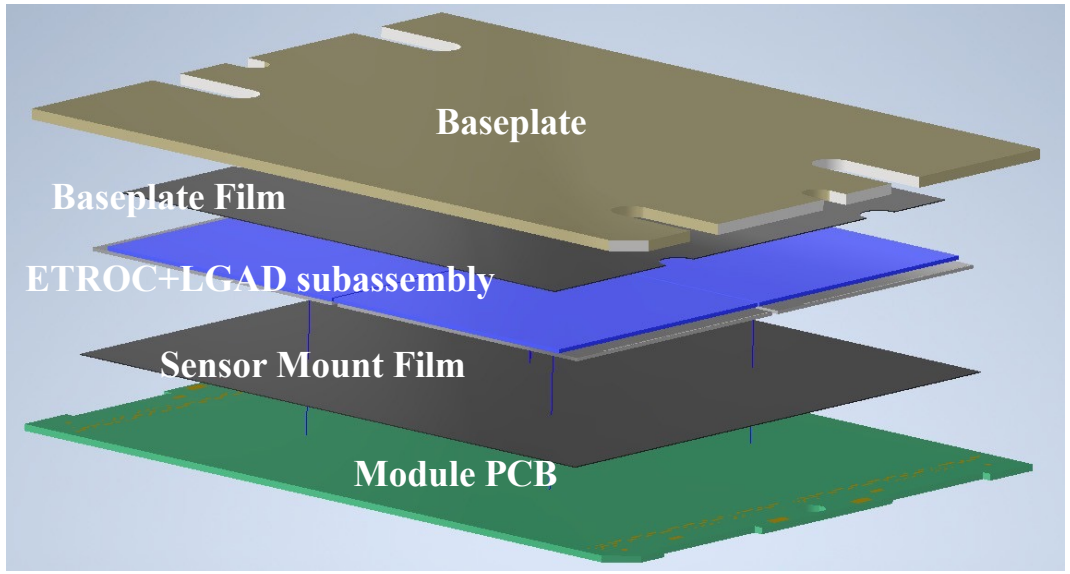


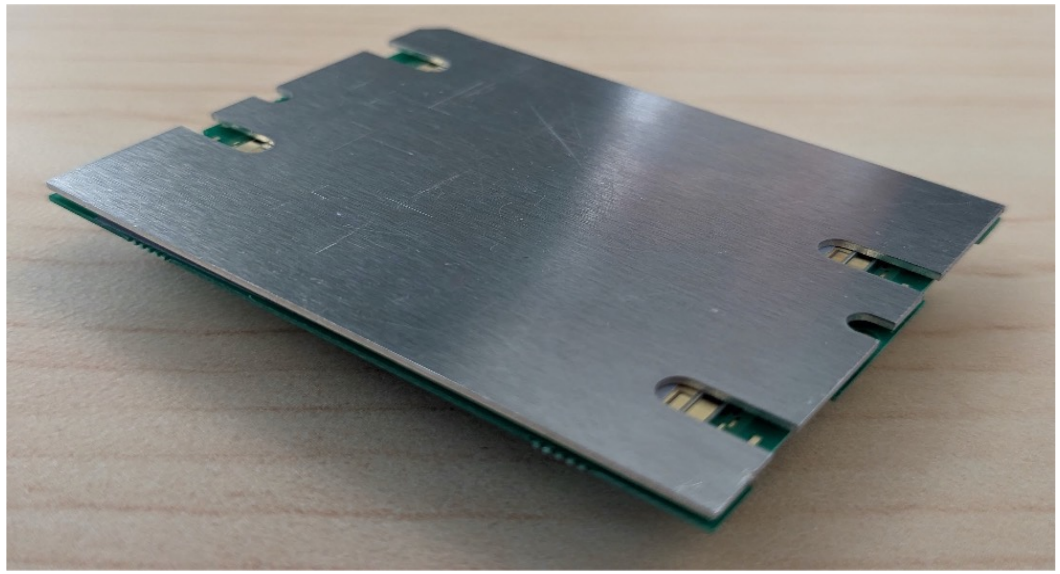
- First system test with bare ETROC2 on the first functional module PCB successful;
- Full demonstration rely on complete system test

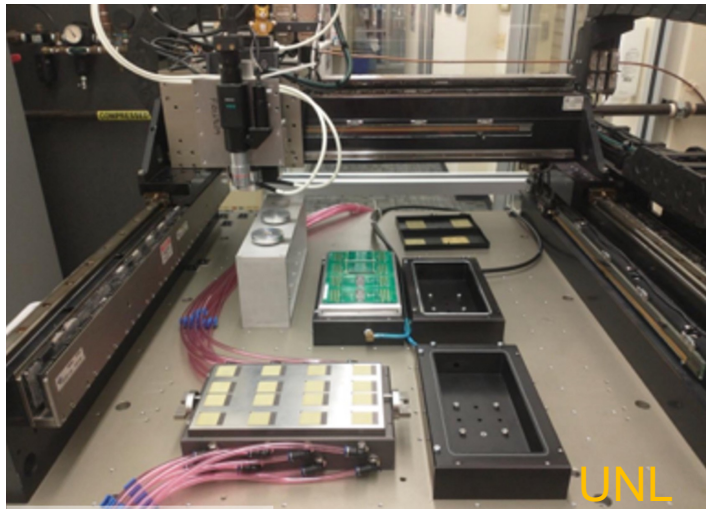


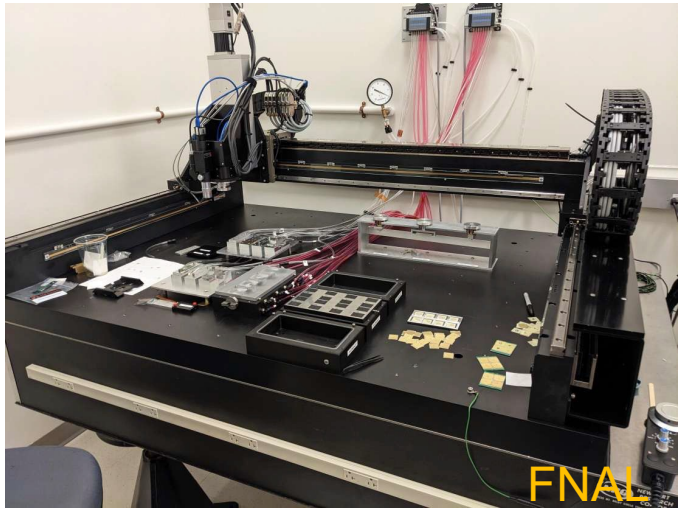


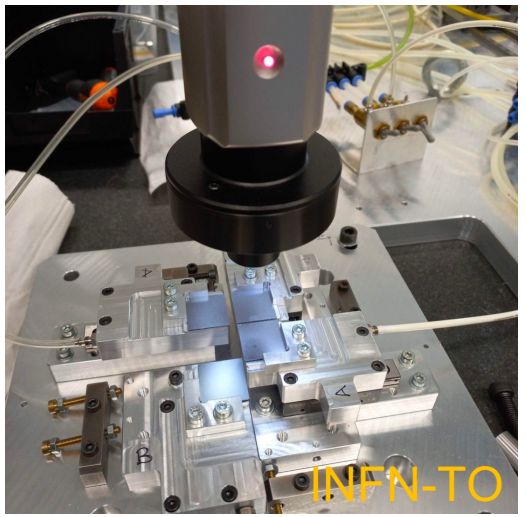
ETL Module Assembly











Summary and Outlook

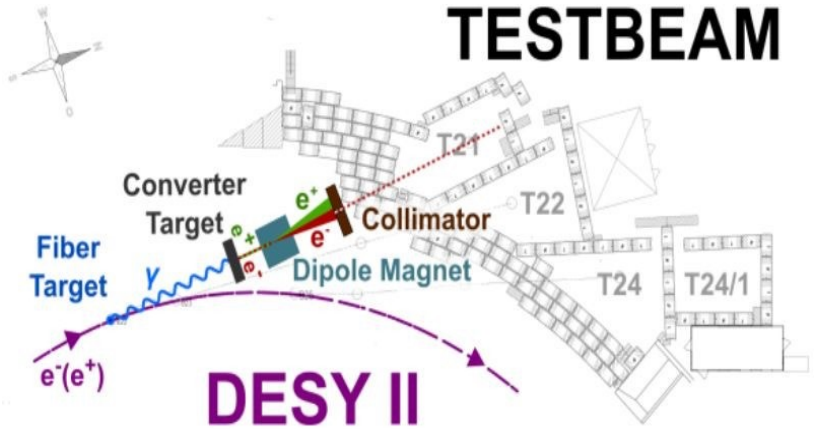
- MTD will be essential for the CMS physics program at HL-LHC
  - Reduce pile-up contributions, improve object reconstruction, enable new physics opportunities
- Mature design for ETL has been established through extensive prototyping and testing
  - LGAD read out by ETROC will provide the needed timing resolution and radiation tolerance at $1.6 < |\eta| < 3$
- ETL is entering a decisive phase of final prototyping
  - Successful MS for LGAD sensors is being concluded
  - Initial testing of ETROC2 indicate no major problem but more to learn in coming months
  - Module design and assembly procedure ready to assemble first functional prototypes
  - Successful initial system test with bare ETROC2 using prototype readout and power boards
  - Other detector system components (cooling, mechanic prototypes, and integration optimization) in progress

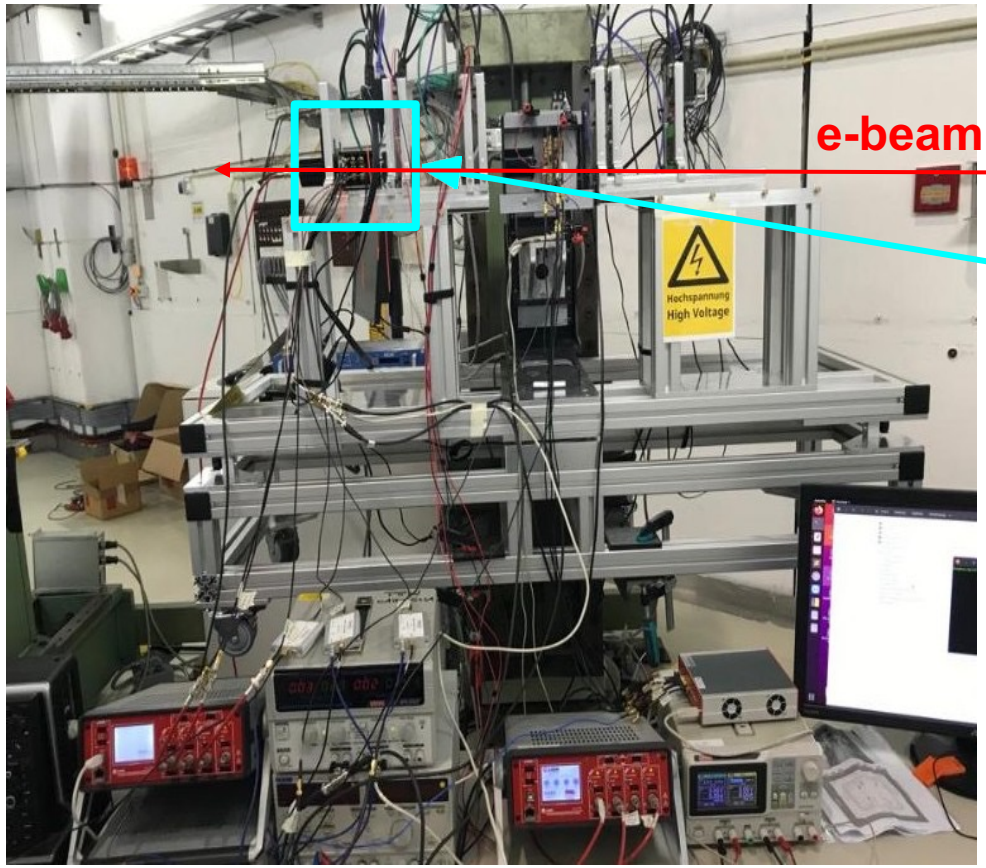

THANK YOU!

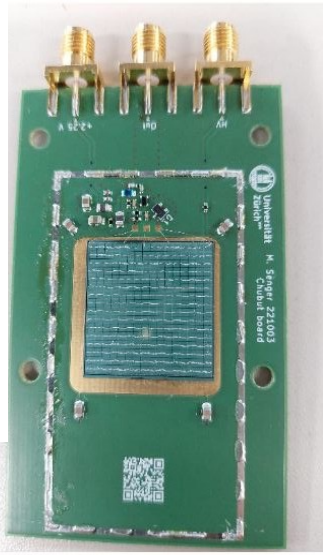
BACKUP

Performance of LGADs

- **1 - 6 GeV electrons** beam, ~ 1 mrad divergence
- **~ 10k particles $s^{-1}cm^{-2}$** rate: depending on energy, beamline, collimation
- Stable and very reliable beam (**99% uptime**)



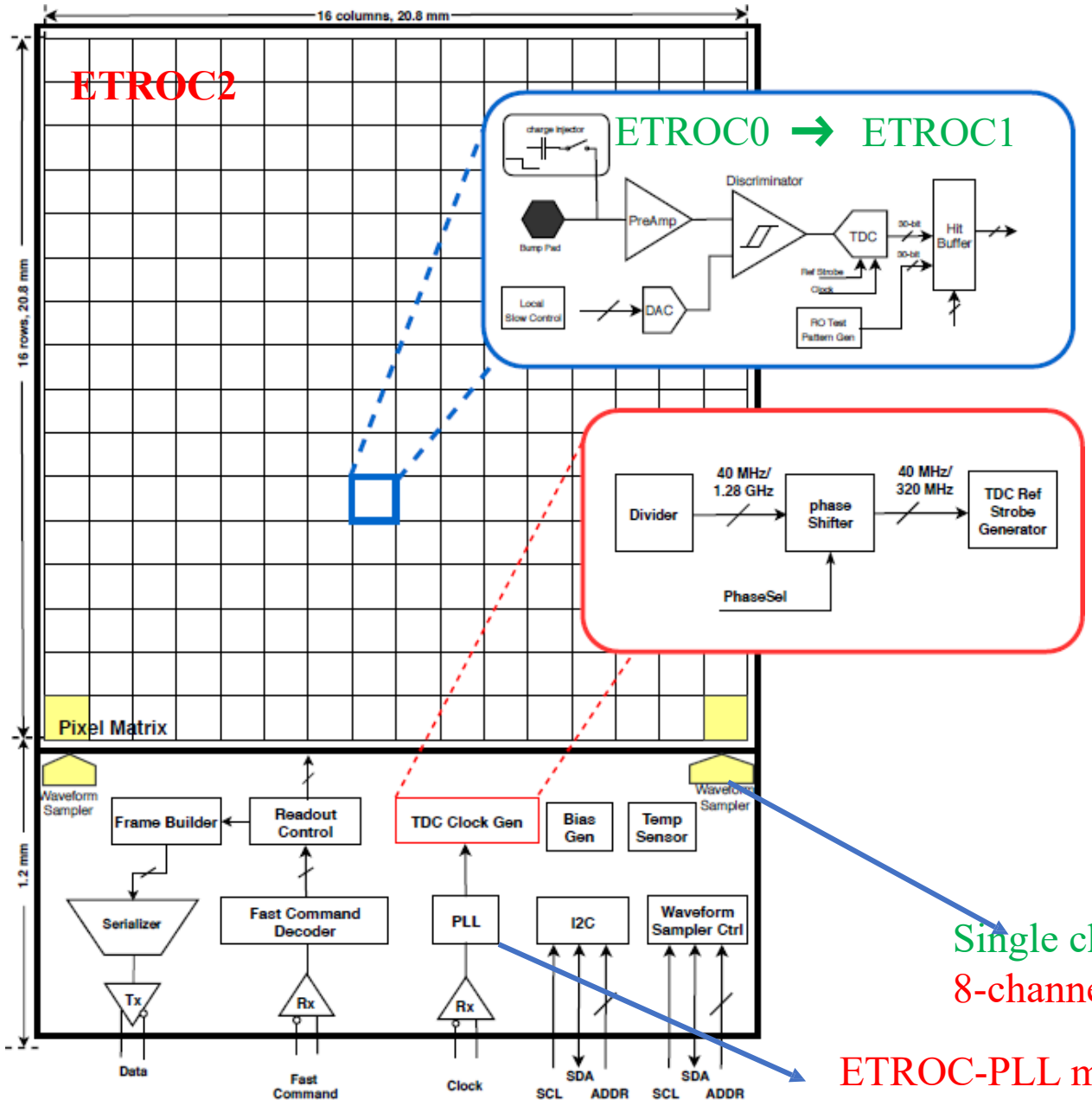




A 16x16 bonded to the UCSC-UZH board

Credits: F. Siviero

ETROC2



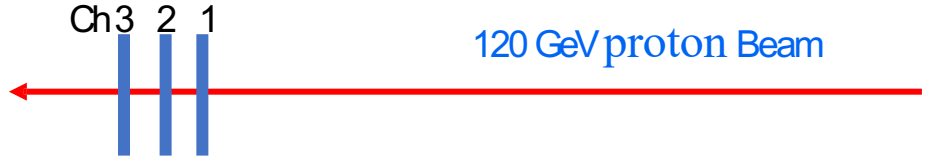
- **ETROC0**: front-end good (TID & beam)
- **ETROC1** status summary: front-end + TDC good
  - Bare ETROC1 extensively tested, excellent TDC performance
  - On-going test beam testing for bump-bonded LGAD+ETROC1, initial results promising
  - TID and SEU test to be done
- **ETROC2** design status: marching forward
  - All critical components are prototyped
    - **Waveform Sampler prototype chips**: good
    - **ETROC PLL Mini-ASIC chips**: SEU test good, TID test to be done
  - The rest of the digital circuitries and system interfaces are *being implemented/prototyped* in firmware

Single channel ADC mini-ASIC (submitted May 2019)
8-channel ADC waveform sampler (submitted March 2020)

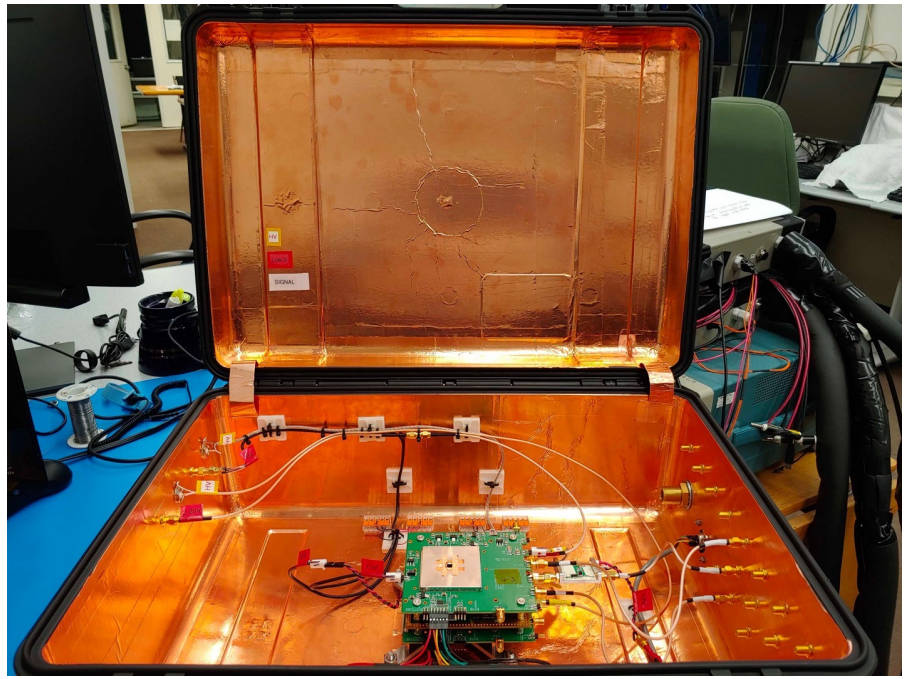
ETROC-PLL mini-ASIC (submitted May 2020)

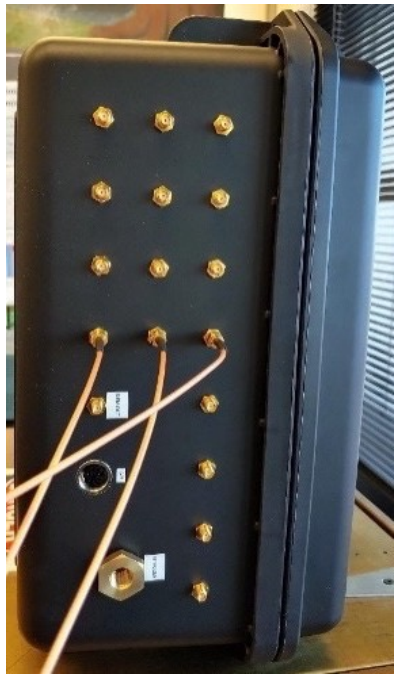
LGAD+ETROC0 – Test Beam Results

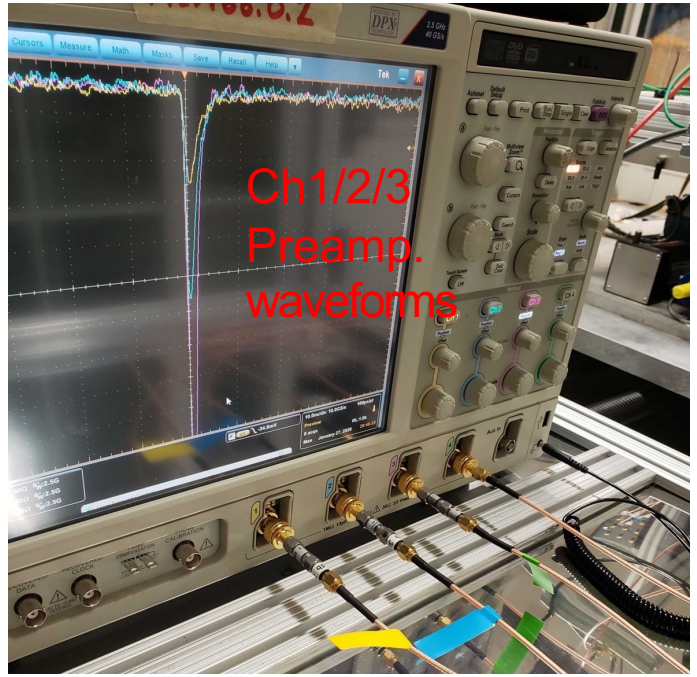
Simple ”suitcase” setup in parasitic mode running at FNAL MTest

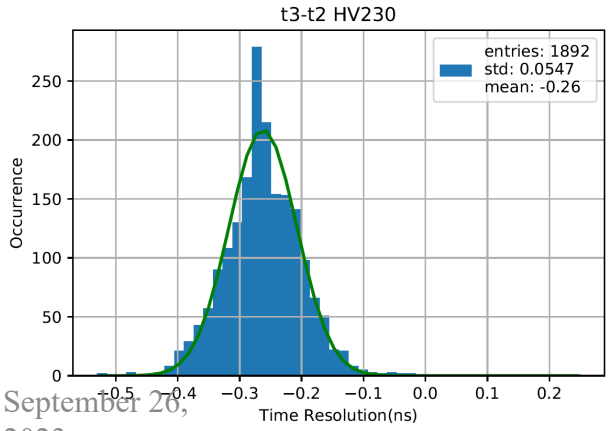


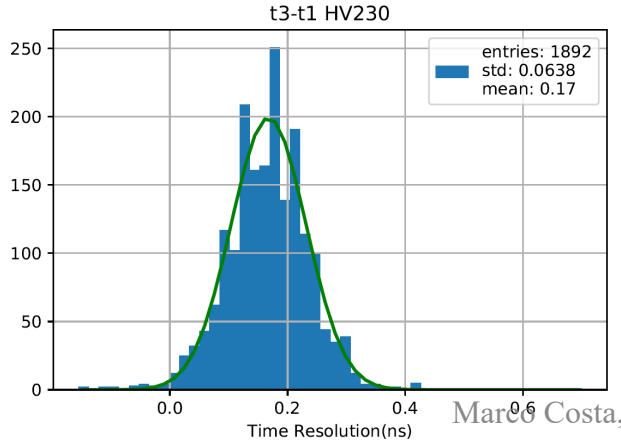
Jan-Feb 2020

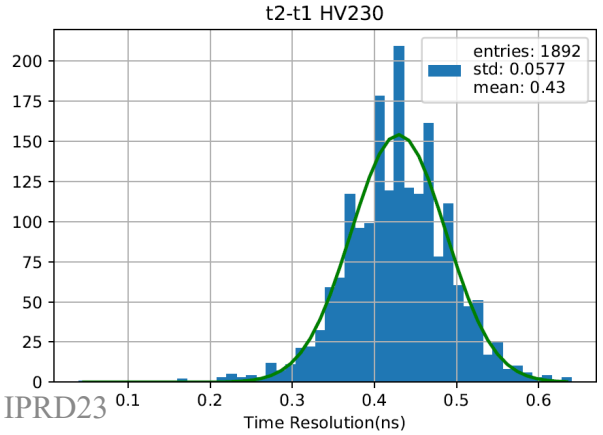












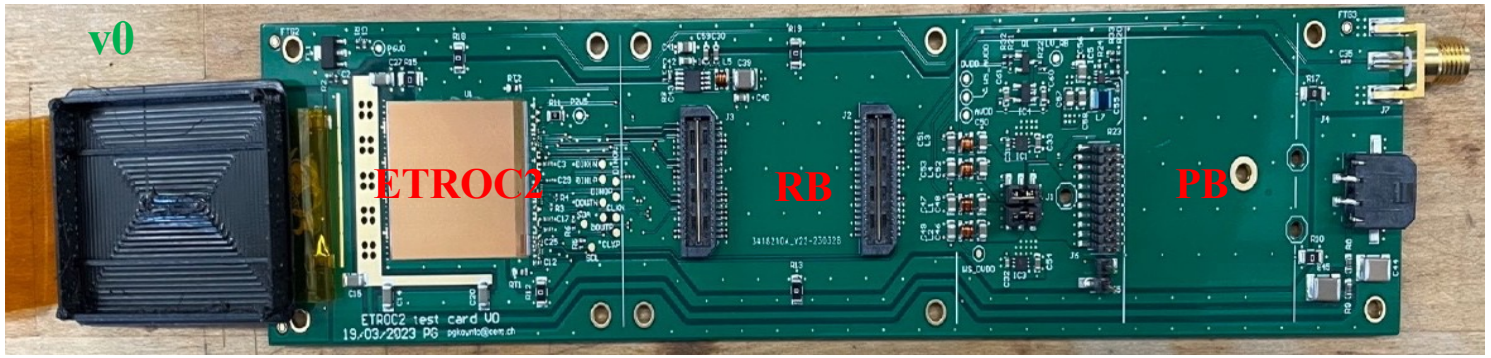
$$\sigma_+ = \sqrt{0.5\ 2(\sigma^+_{+-} + \sigma^+_{\cdot+} - \sigma^+_{\cdot-})}$$

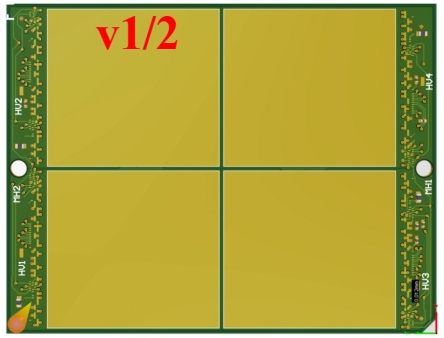
$$\approx 33\ (ps)$$

from LGAD+ETROC0 preamplifier waveforms

Module PCB

- **v0 ETROC+LGAD test card: in use for system tests**
  - RBv2 compatible, interfaces to PB prototypes and external power supply, robust connector for bias voltage
  - Includes debugging features, e.g., discrete preamplifier to observe LGAD signal directly
  - 10 boards assembled for initial test of bare ETROC2; next revision with minor updates and fixes available soon

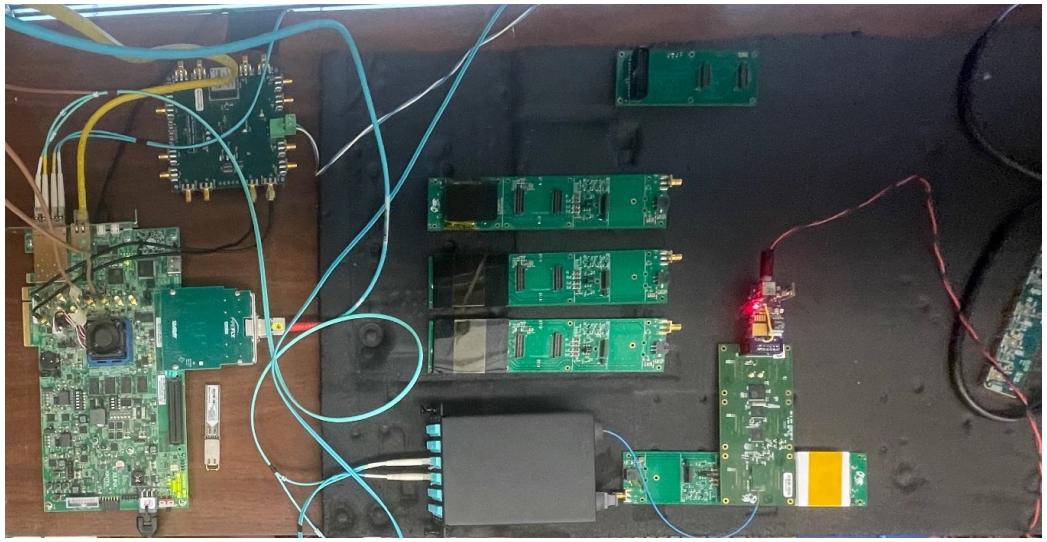




- **v1 Mechanical prototype for assembly optimization:** design in progress
  - Discussion between electronics engineers and modules team to define the mechanical specifications
  - Fabricate a work-in-progress PCB design and send to module production team to get feedback on mechanics, allow them to refine and test tooling, understand any potential issues w/ component placement, etc.
- **v2 full functioning prototype:** submission mid-summer
  - Fully functioning module PCB with four ETROCs in a "CMS-like" form factor
  - Based on whatever feedback and understanding we have from ETROC testing over the next few months
  - Explore layout requirements (blind vias, layer count, stackup, etc)
- **v3/v4 Initial/final design targeting ETROC3**

System Test

- First version of a functional module PCB (v0) is used for initial system tests of ETROC2
  - Directly interfaces with RBv2; internal power converter for initial tests for ETROC2; can eventually host power board prototype or FEAST modules
  - First batch of 10 boards: 6 mounted with bare ETROC2, 4 working, 2 not working ones will have ETROC2 replaced; 3 more will mount bare ETROC2 soon
  - Working on first revision with feedback from electrical tests and first experience with ETROC2
- Software and Firmware developed with emulator, essentially plug-and-play with the real ETROC2
  - Successful I2C communication, read/write to peripheral and pixel configuration registers, fast communication, readout of internal test data and data words after L1A
  - Currently setting up monitoring of reference voltage, internal and external temp measurements,
  - Immediate next steps: threshold scan and charge injection



Successful tests

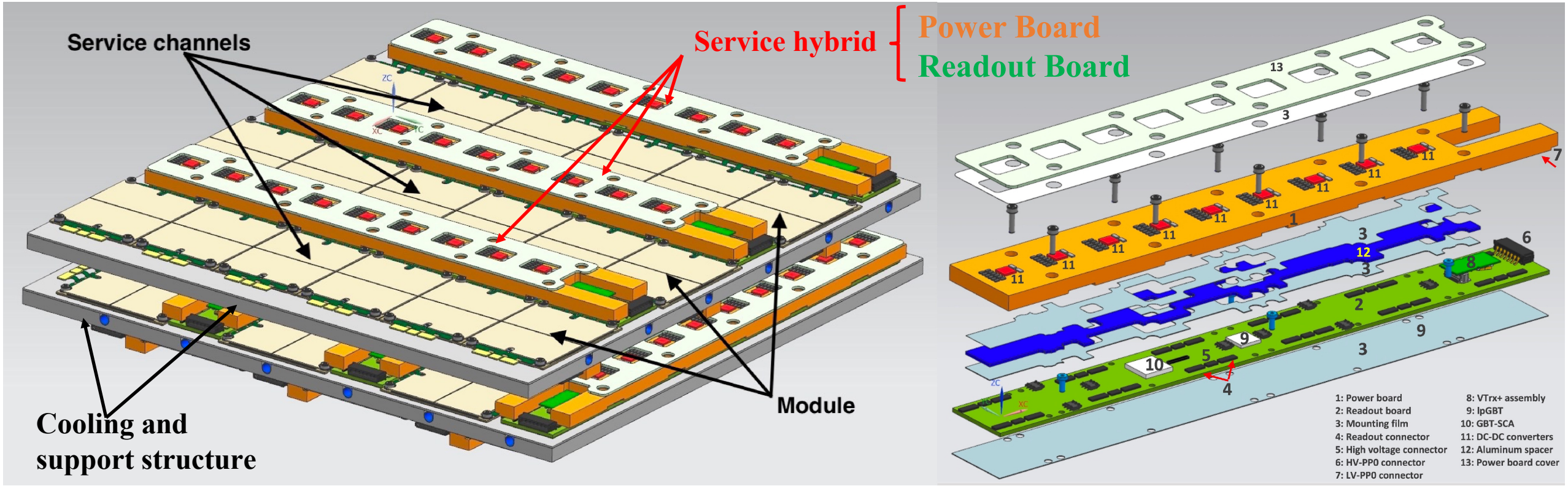
```
 - Checking peripheral status:
Perif status reg='fcBitAlignError': ret=0
Perif status reg='PS_Late': ret=1
Perif status reg='AFCcalCap': ret=32
Perif status reg='AFCBusy': ret=0
Perif status reg='fcAlignFinalState': ret=0
Perif status reg='controllerState': ret=11
Perif status reg='fcAlignStatus': ret=0
Perif status reg='invalidFCCount': ret=1372
Perif status reg='pllUnlockCount': ret=1
Perif status reg='EFuseQ': ret=0

 - Running pixel sanity check:
Passed!

 - Running pixel random check:
Passed!

 - Checking configuration for pixel (4,5):
Pixel (row=4, col=5) config reg='CLSel': ret=0, exp=0
Pixel (row=4, col=5) config reg='IBSel': ret=7, exp=7
Pixel (row=4, col=5) config reg='RfSel': ret=2, exp=2
```

ETL – Service Hybrid



- **Service Hybrid** is an assembly of two PCBs, a Power Board and a Readout Board, servicing 12 modules.
- **Power Board** distributes low voltages provided by power supplies to ETROCs, slow control adapter chip, lpGBT, and VTRx+. The voltages are regulated by radiation hard and B-tolerant DC-DC converters on the power board.
- **Readout Board** distributes bias voltages to LGAD sensors, receives and distributes fast control signals and slow controls to ETROCs, and route data and monitoring information from ETROCs to backend DAQ.