Title: Pixel Detector Hybridization and Integration with Anisotropic Conductive Adhesives

Abstract/Summary:

A reliable and cost-effective interconnect technology is required in the development of hybrid pixel detectors. The interconnect technology needs to be adapted for the pitch and die sizes of the respective applications. For small-scale applications and during the ASIC and sensor development phase, interconnect technologies must also be suitable for the assembly of single-dies typically available from Multi-Project-Wafer submissions.
Within the CERN EP R&D program and the AIDAinnova collaboration, innovative and scalable hybridization concepts are under development for pixel-detector applications a future colliders. This contribution presents recent results of a newly developed in-house single-die interconnection process based on Anisotropic Conductive Adhesives (ACA). The ACA interconnect technology replaces solder bumps with conductive micro-particles embedded in an epoxy layer applied as either film or paste. The electro-mechanical connection between the sensor and ASIC is achieved via thermo-compression of the ACA using a flip-chip device bonder. The ACA technology can also be used for ASIC-PCB/FPC integration, replacing wire bonding or large-pitch solder bumping techniques.
A specific pixel-pad topology is required to enable the connection via microparticles and create cavities into which excess epoxy can flow. This pixel-pad topology is achieved with an in-house Electroless Nickel Gold process that is also under development within the project.
The ENIG and ACA processes are qualified with a variety of different ASICs, sensors and dedicated interconnect test structures, with pad diameters ranging from 12 µm to 140 µm and pitches between 20 µm and 1.3 mm. The produced assemblies are characterized electrically, with radioactive-source exposures, and in tests with high-momentum particle beams.
This contribution introduces the developed interconnect and plating processes and showcases different hybrid assemblies produced and tested with the above mentioned methods. A focus is placed on recent optimization of the plating and interconnect processes, resulting in an improved plating uniformity and interconnect yield.

[308 words]

Authors:

Alexander Volker alexander.volker@cern.ch

Janis Viktor Schmidt janis.viktor.schmidt@cern.ch

Dominik Dannheim dominik.dannheim@cern.ch

Peter Svihra peter.svihra@cern.ch

Mateus Vicente Barreto Pinto m.vicente@cern.ch

Rui de Oliveira rui.de.oliveira@cern.ch

Justus Braach justus.braach@cern.ch

Matteo Centis Vignali mcentisvignali@fbk.eu

Giovanni Calderini giovanni.calderini@lpnhe.in2p3.fr