TIFPA Trento Institute for Fundamental Physics and Applications

UNIVERSITÀ DI TRENTO

Simulation and first characterization of MAPS test structures with gain for timing applications

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ARCADIA

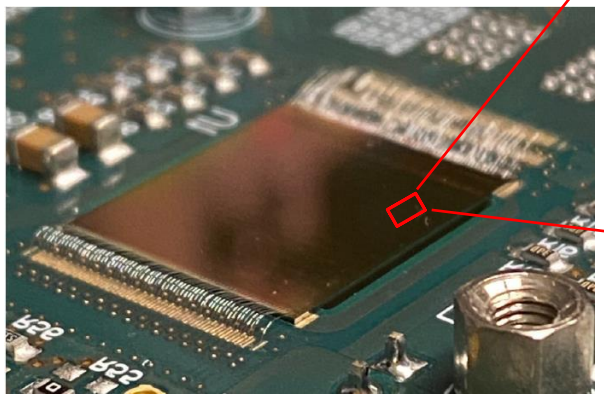
***A**dvanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays*

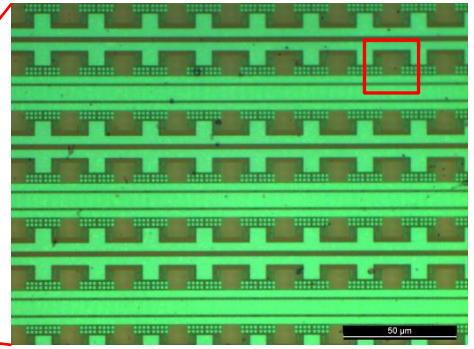
Outline

1) ARCADIA sensor concept
2) Passive test structures
3) Electrical characterization
4) Laser characterization
5) Conclusions

ARCADIA Project

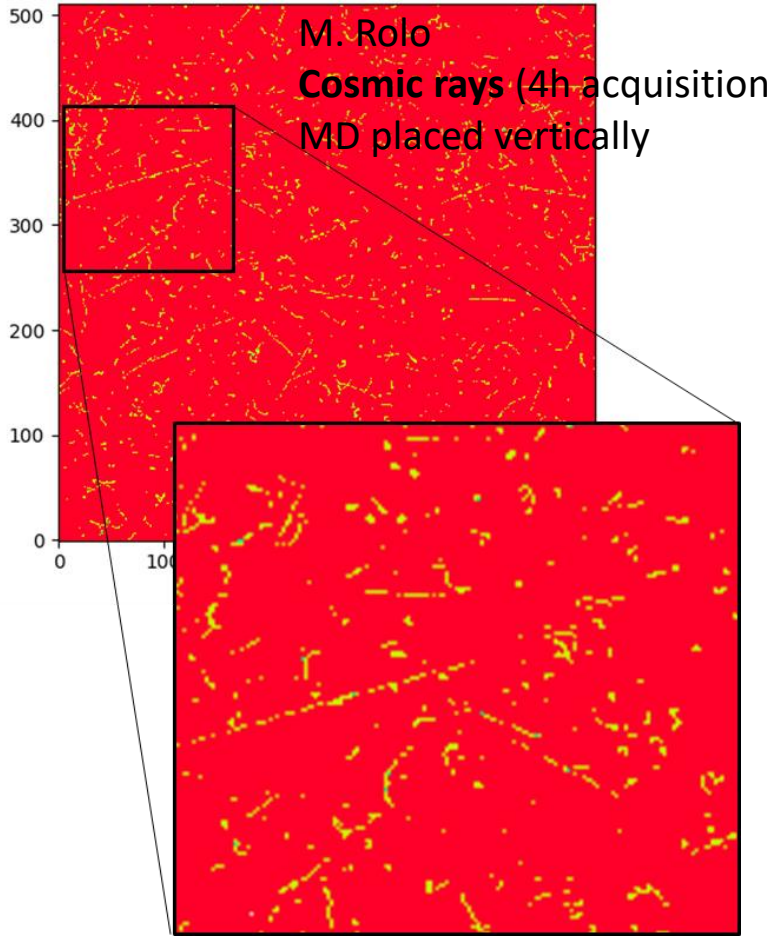
Andrea Paternò, Vertex 2021
ARCADIA MD1 chip



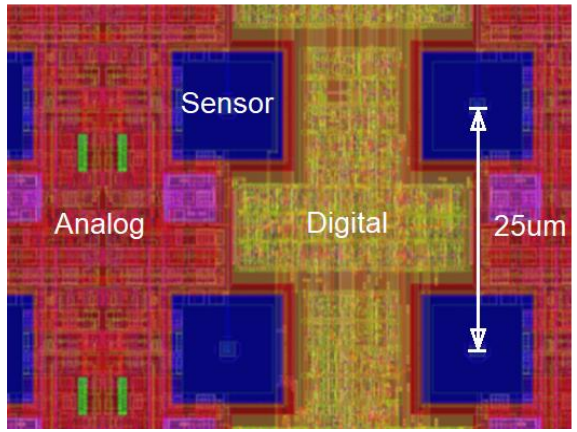


MD1 chip micrograph

- Fully depleted MAPS
- Target applications:
  - medical imaging
  - space applications
  - HEP experiments (ALICE timing layer)



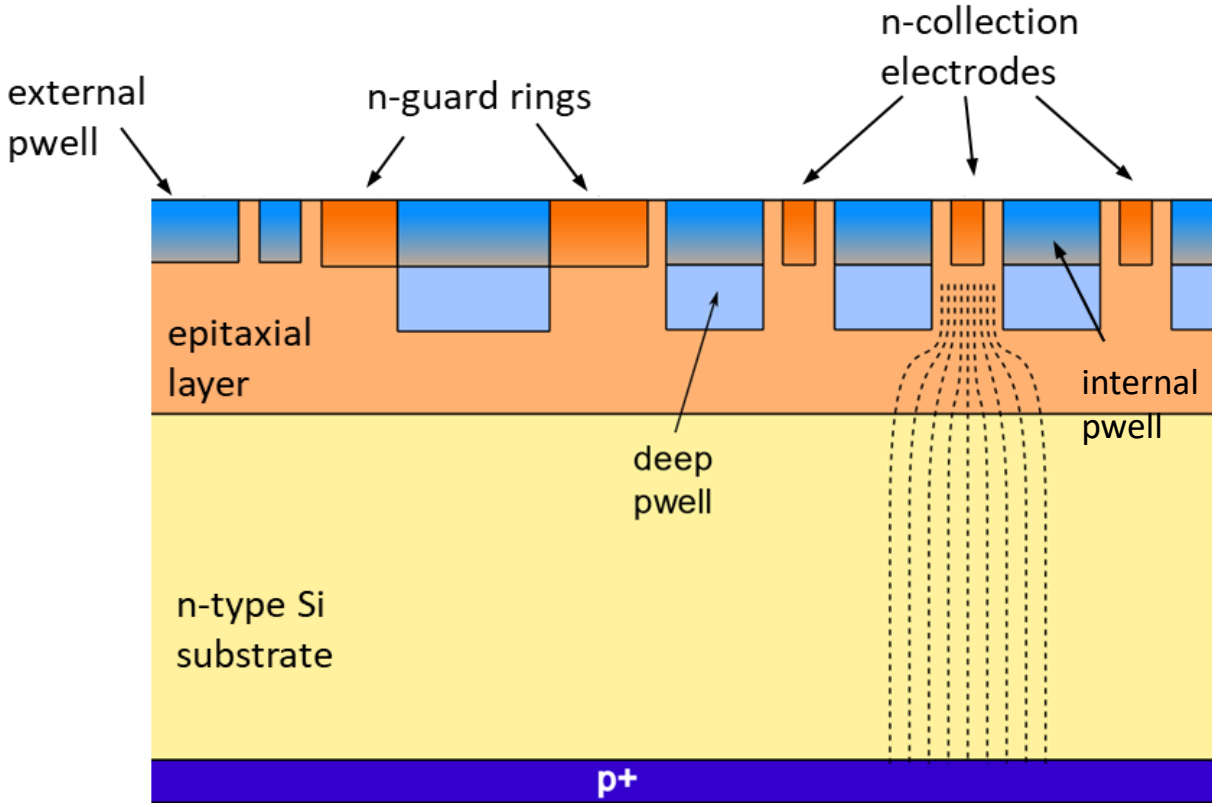
- Main Demonstrator (MD) with sensor array made of 512x512 pixels with 25µm pixel pitch
- Embedded analog and digital frontend electronics
- 3 engineering runs: 1st (mid 2021), 2nd (beginning of 2022), 3rd (beginning 2023)



M. Rolo, **Pixel layout**

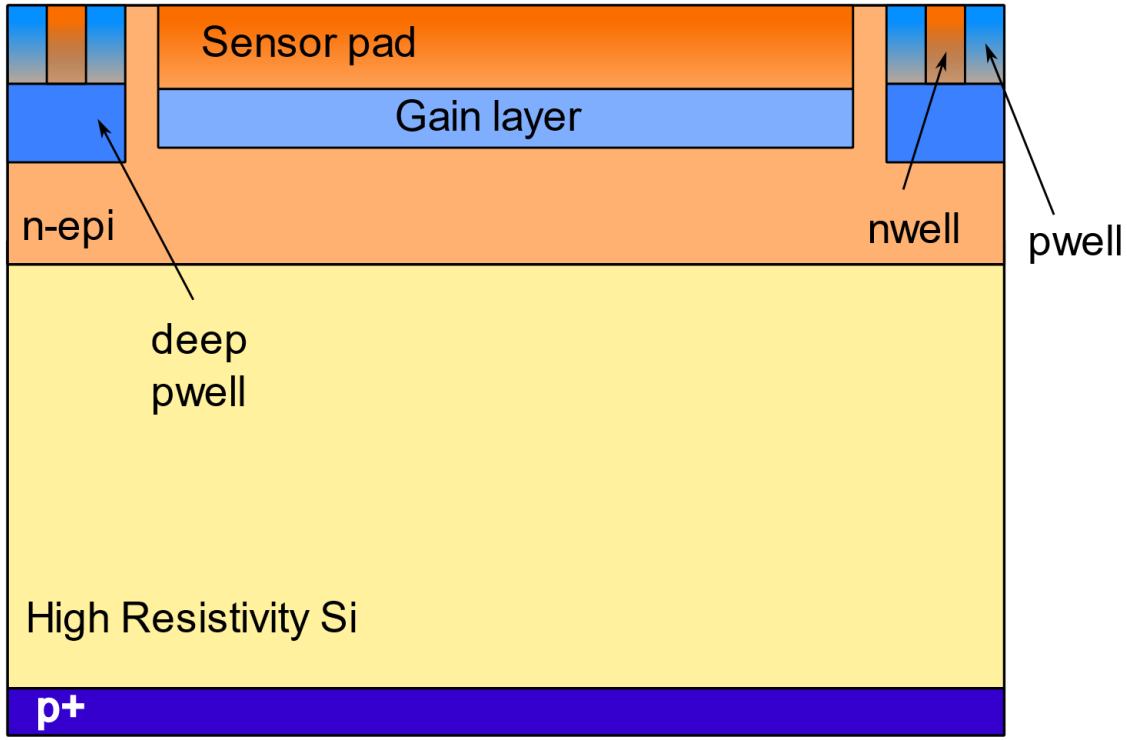
Sensor concept

- Produced with commercial CMOS 110nm process (LFoundry)
- High resistivity silicon substrates
- N-type epitaxial layer to delay the onset of the punch through
- Operation in full depletion condition
- Independent frontside and backside electrodes for the voltage bias



Process add-on for timing

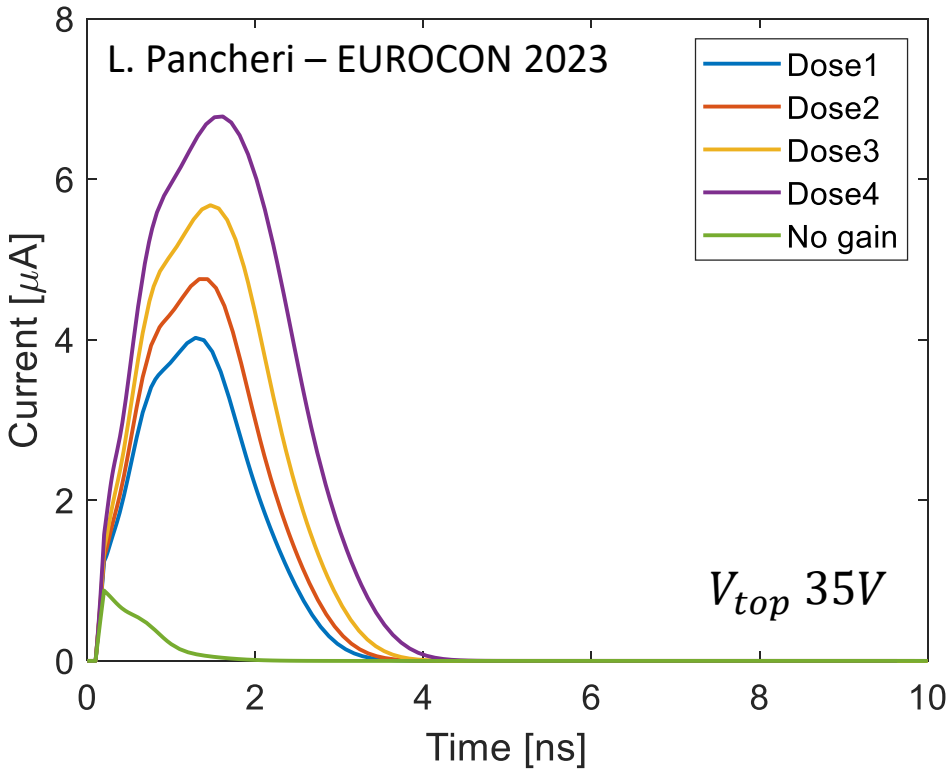
Foreseen V_{top} between 30-40 V



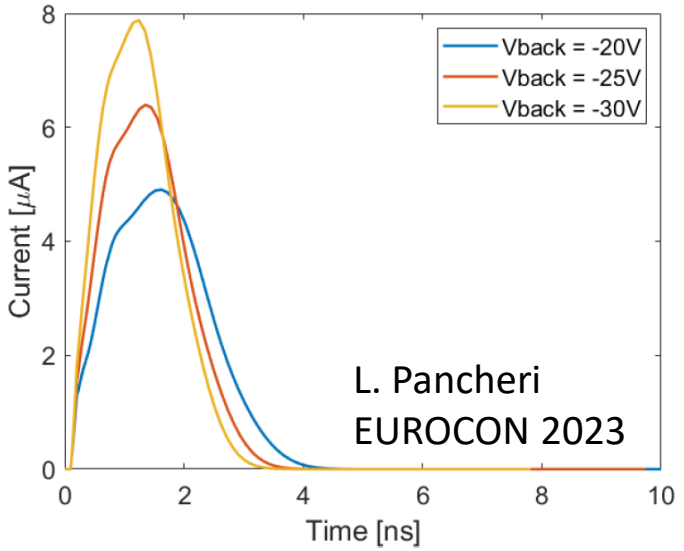
L. Pancheri – EUROCON 2023

- Additional p-type implantation to create the gain layer below the n-type collection electrode
- Preliminary TCAD simulations to tune the gain layer implant
- Four dose splittings for the gain layer with 3 wafers for each dose
- AC-coupled frontend preamplifier
- High voltage on the topside to enable avalanche multiplication

Preliminary TCAD simulations

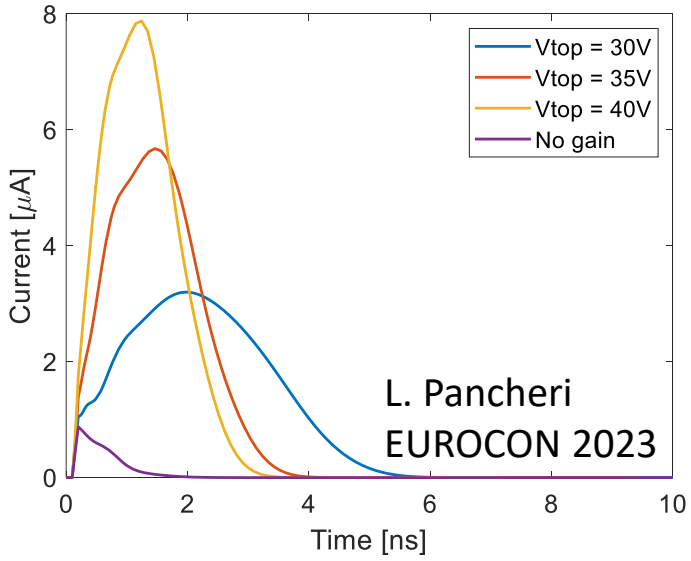


- Increasing gain for higher gain layer doping concentrations

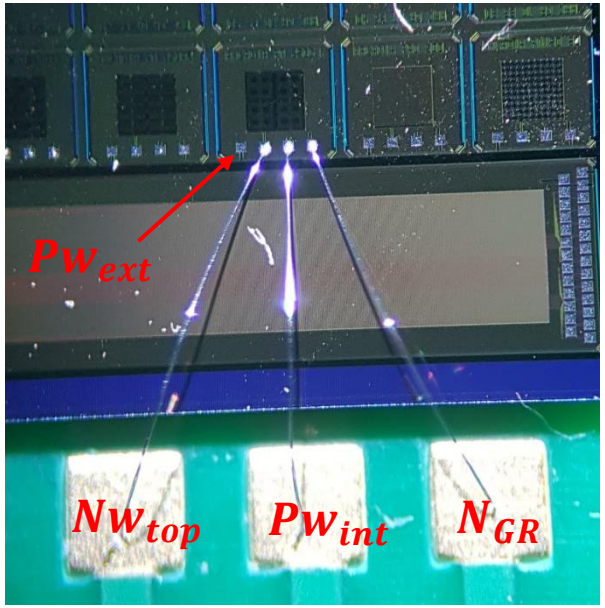


- V_{bias} and V_n limited from punch through and edge breakdown

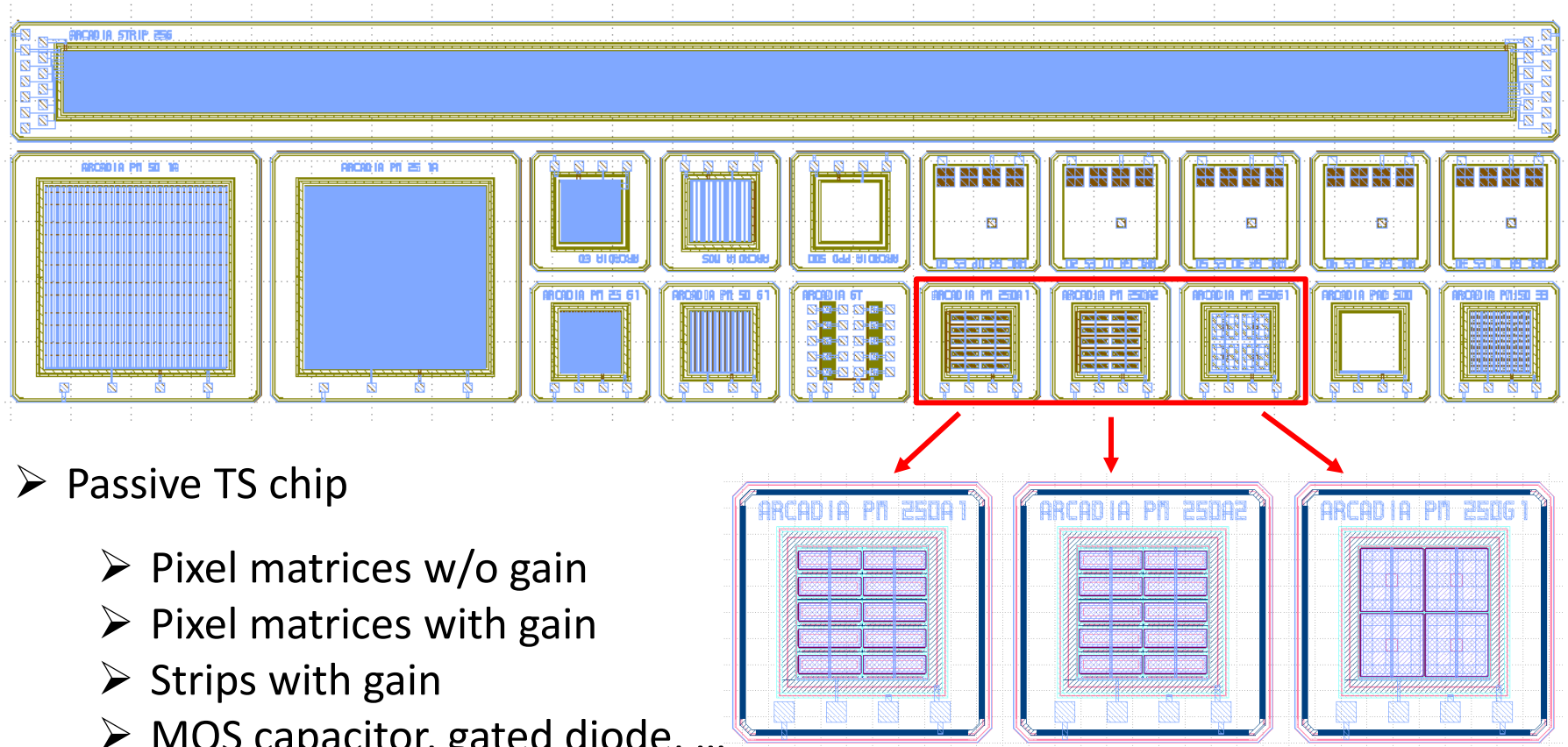
- Control on gain and charge collection dynamics acting on V_{bias} and V_n



Passive Test Structures

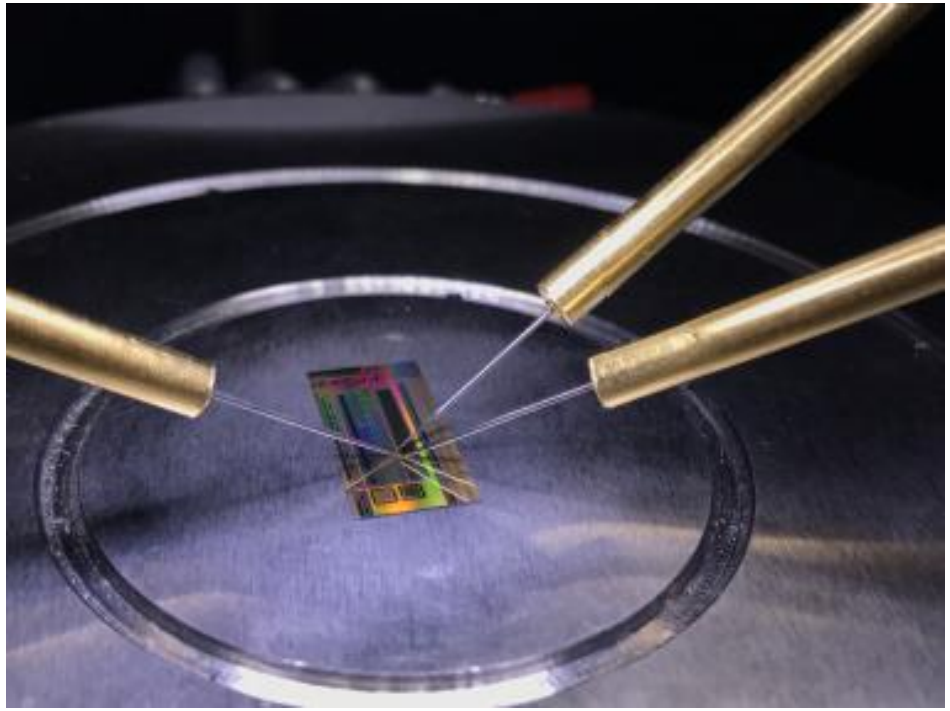


- Chip frontside electrodes
  - External pwell
  - N-type sensor nodes
  - Internal pwell
  - N-guard rings



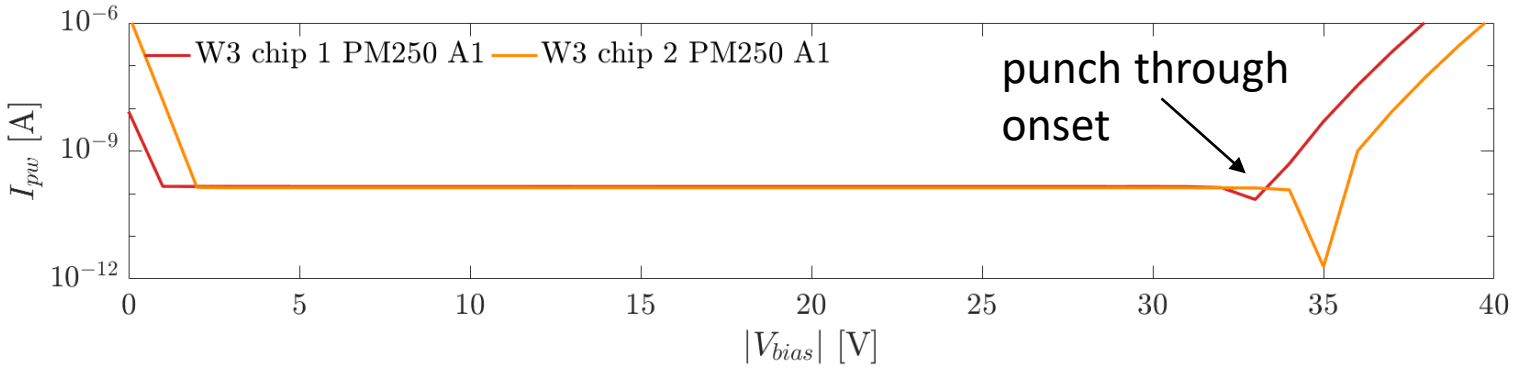
- Passive TS chip
  - Pixel matrices w/o gain
  - Pixel matrices with gain
  - Strips with gain
  - MOS capacitor, gated diode, …

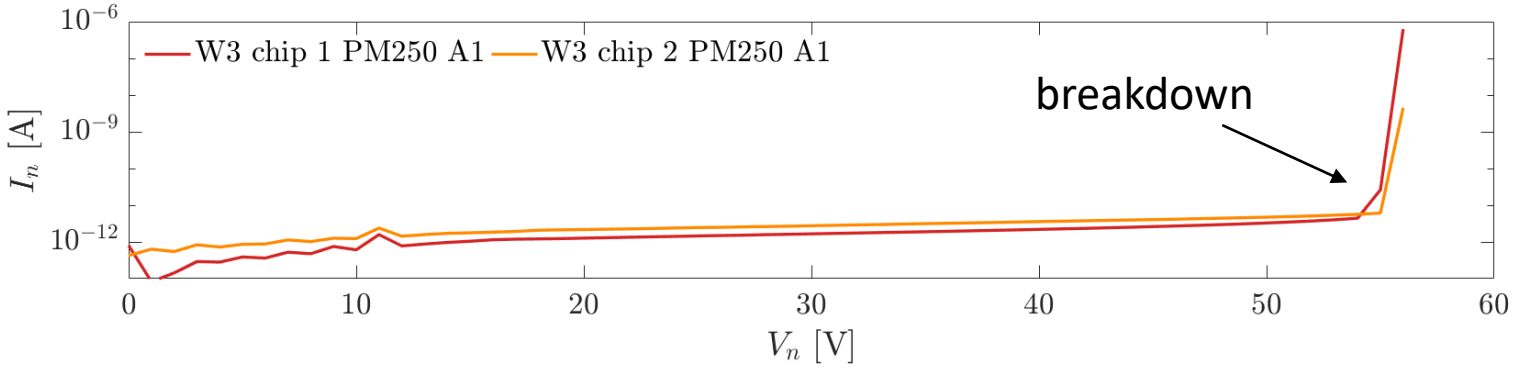
Electrical characterization – IV curves



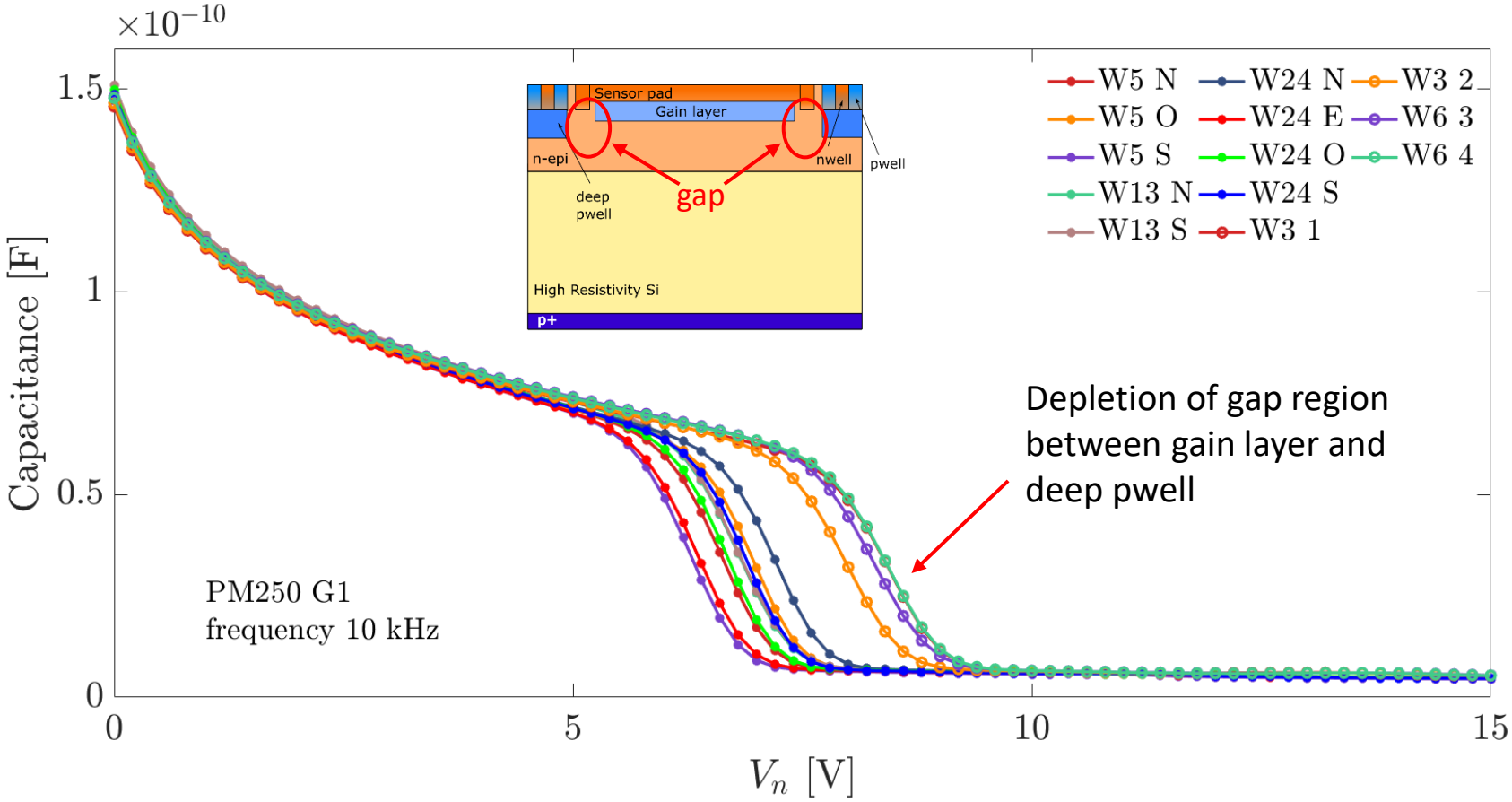
Coralie Neubüser, TIFPA-INFN

- Dips in the pwell current reference to extract V_{PT}
- Evaluate breakdown voltage associated to V_n



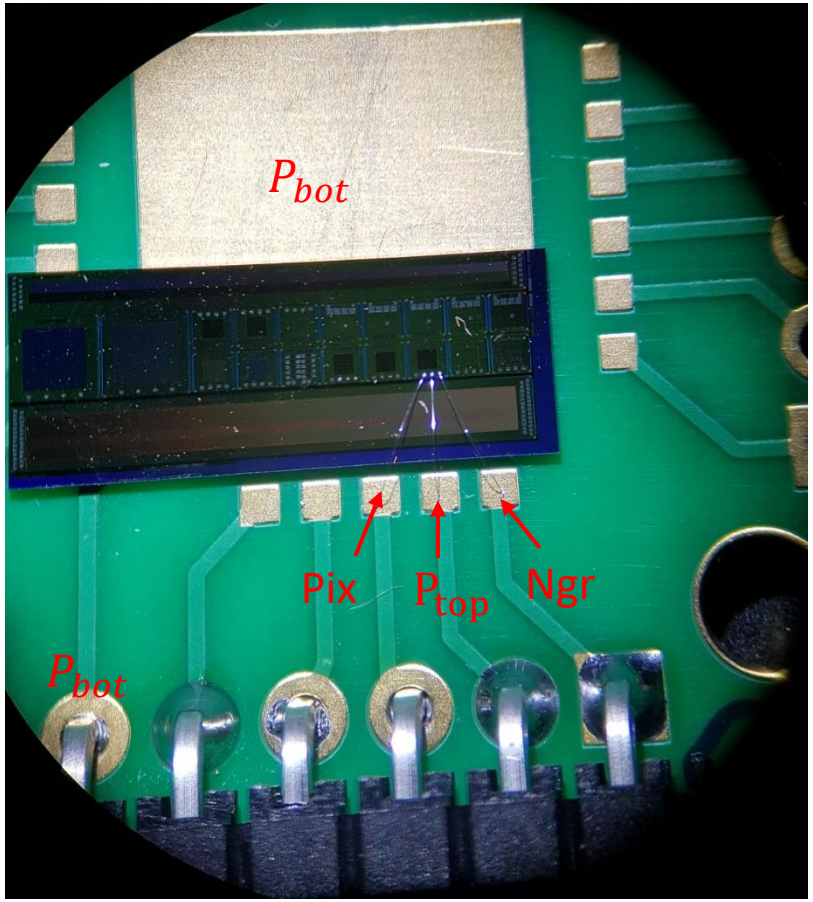


Electrical characterization – CV curves



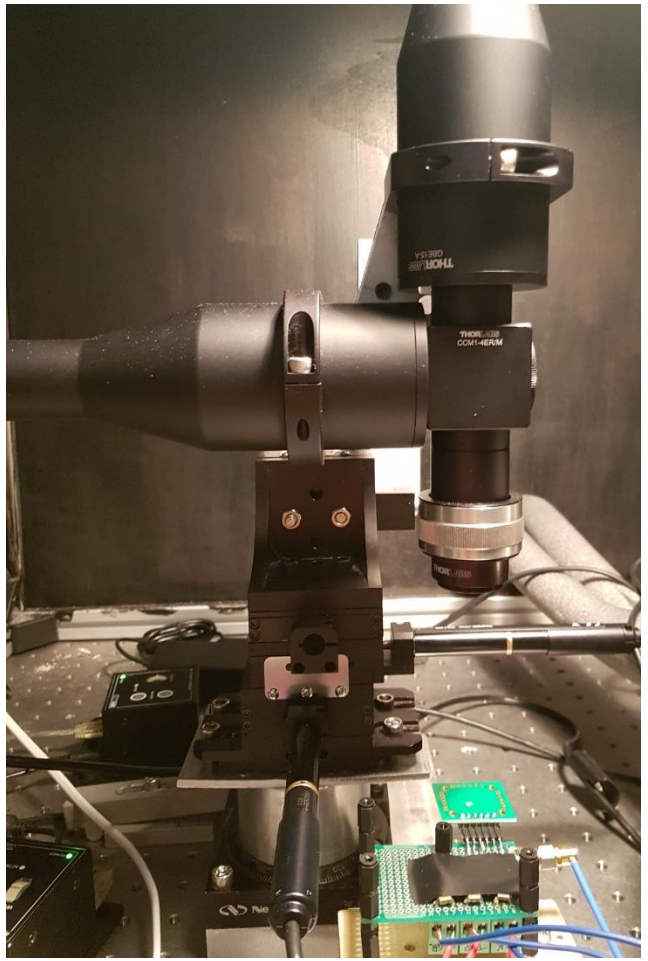
- Pwell voltage set to 0V as ground reference
- Voltage sweep applied to the frontside nwell
- Data proved the gain layer presence
- Gain layer profile cannot be completely evaluated with CV curves

Biasing scheme & Optical setup

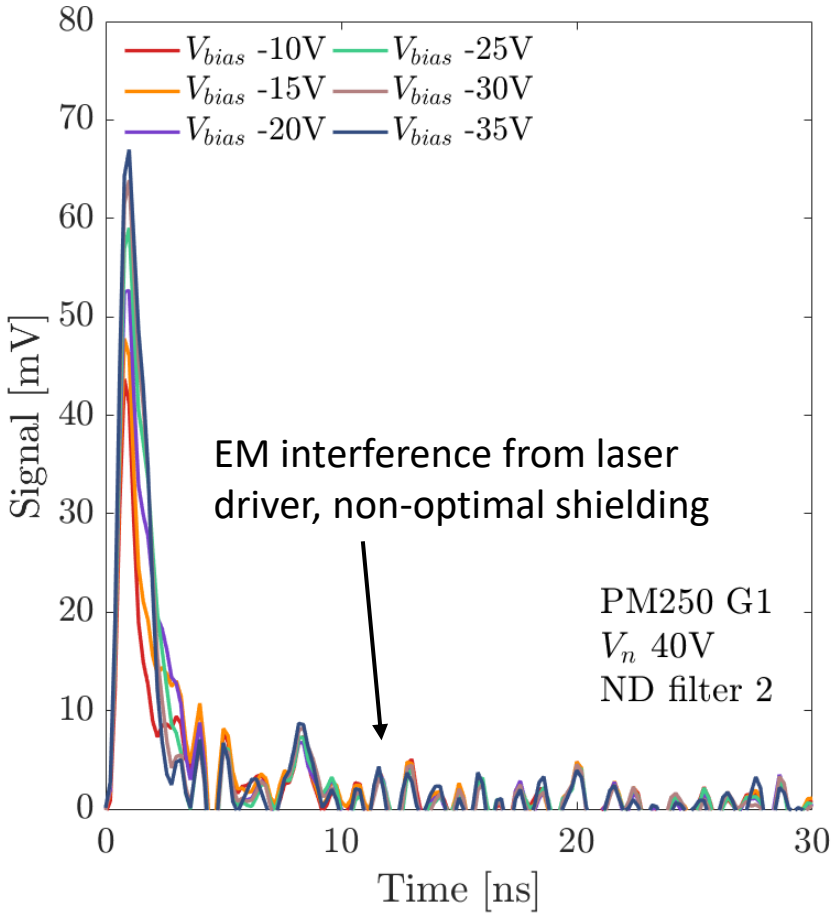


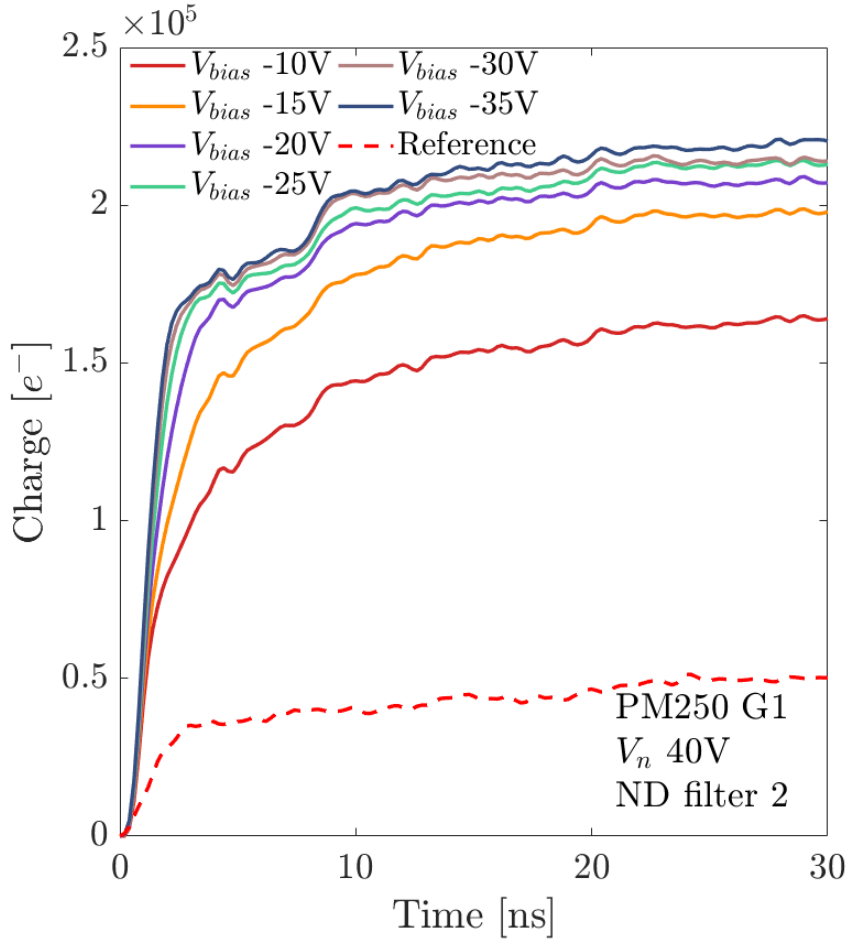
- V_{bias} applied to $\mathrm{P_{bot}}$ electrode through PCB metal pad
- $V_{pix} = V_n$
- $V_{Ngr} = 8V$
- $V_{Ptop} = 0V$

- Infrared laser (1060nm) with < 100ps pulse at FWHM (Alphalas)
- Hamamatsu C5594 external amplifier (50 kHz - 1.5 GHz BW, 36 dB gain)
- Backside illumination through PCB hole



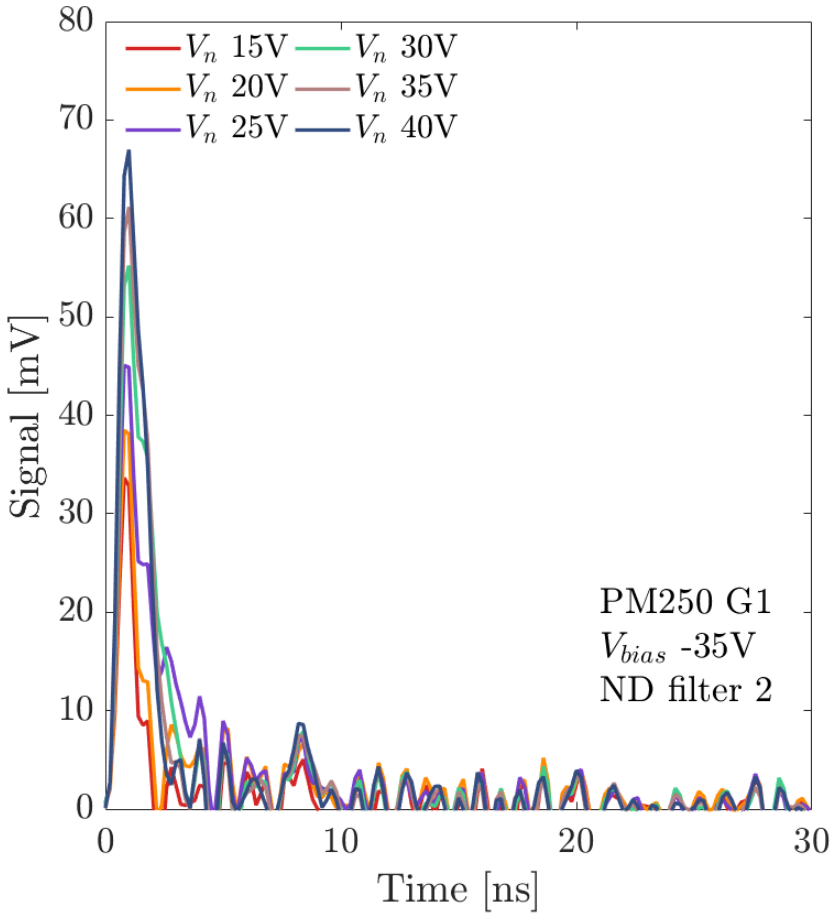
IR laser - PM 250 G1

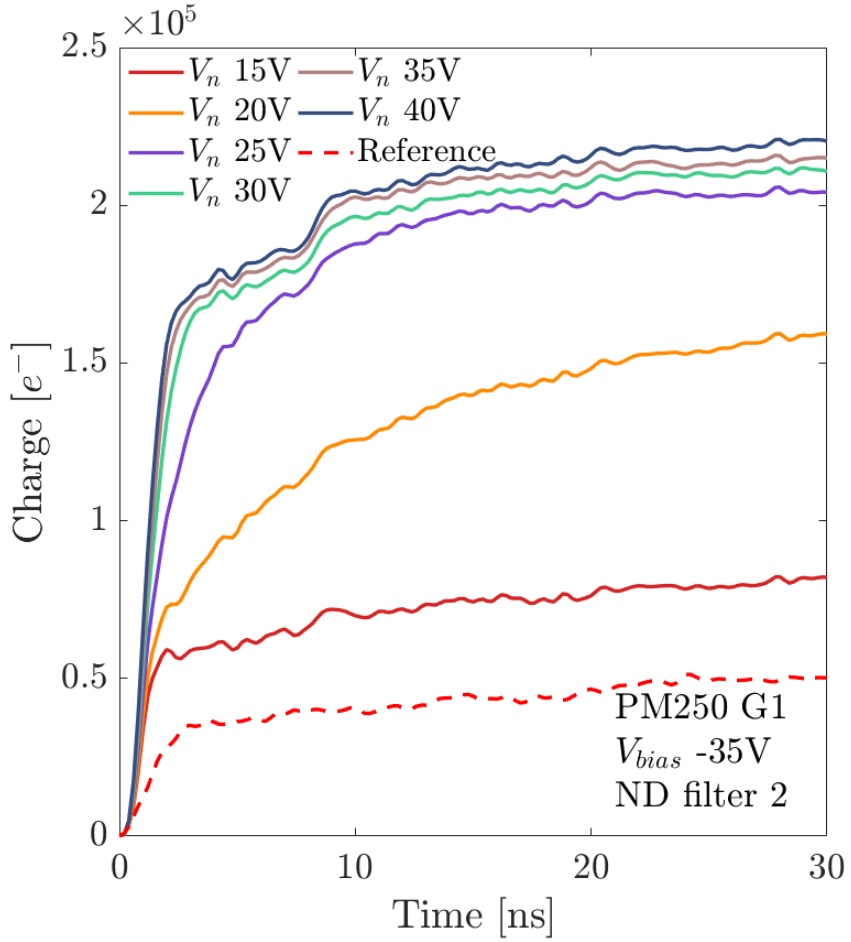




- t_{act} 48 µm
- Backside illumination with a focused IR laser spot
- Digital oscilloscope with 1 GHz bandwidth
- $Gain = \frac{CC_{PM250}}{CC_{ref}} \approx 4$
- Faster charge collection for higher V_{bias}

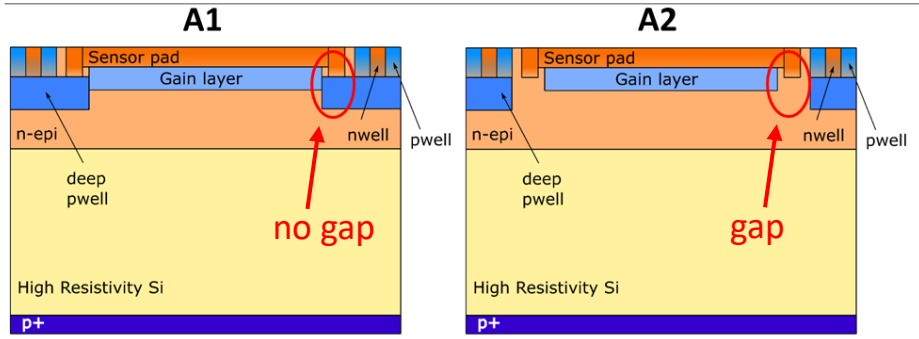
IR laser - PM 250 G1

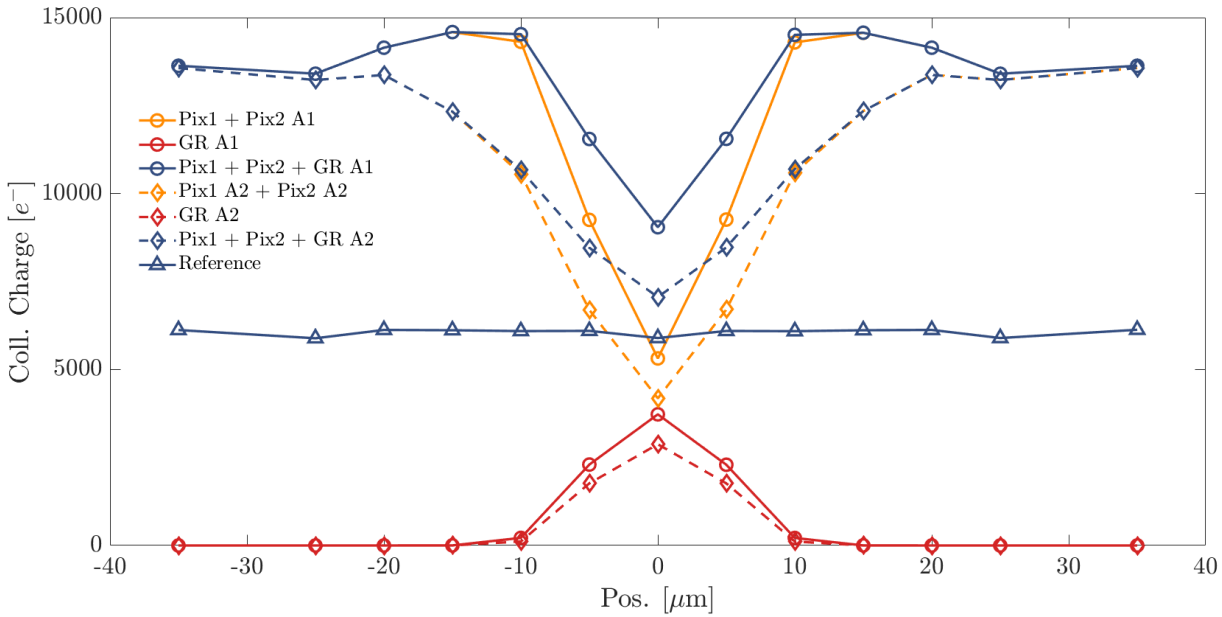




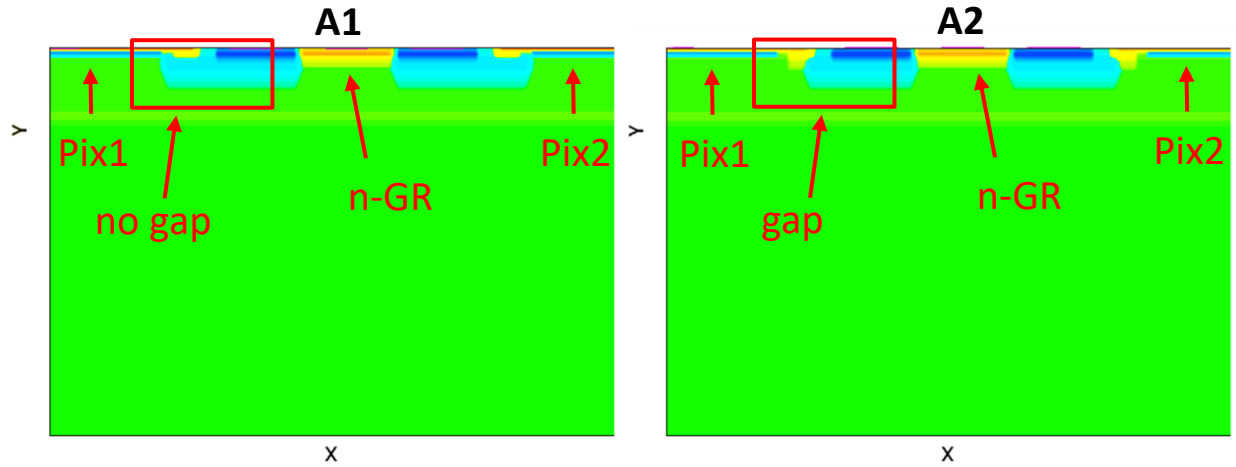
- t_{act} 48 µm
- Backside illumination with a focused IR laser spot
- Possibility to control the gain value acting on V_n

PM250 layout comparison



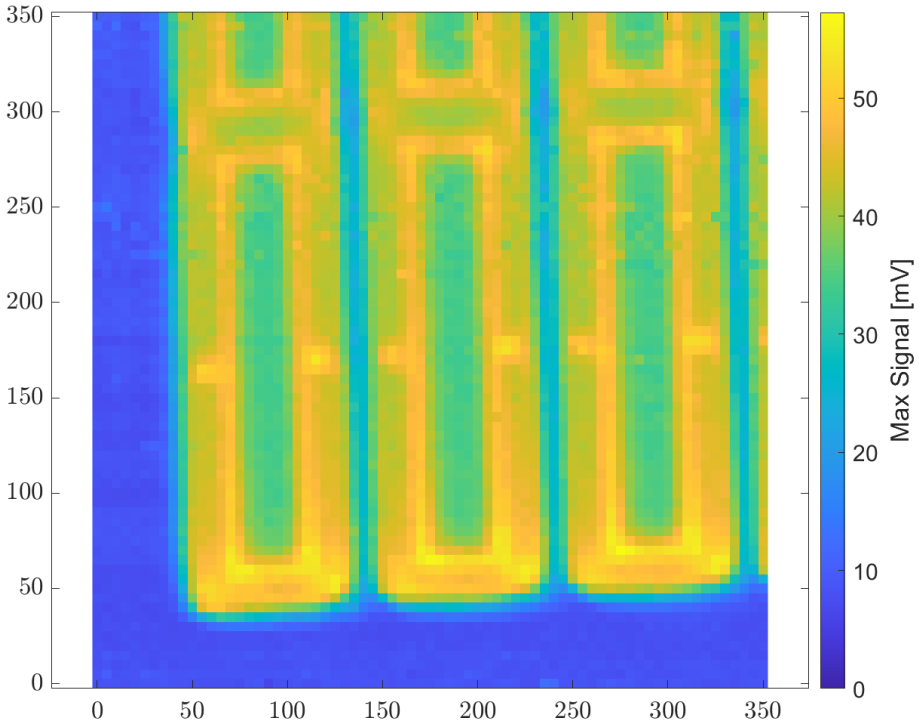


- PM250 with layout A1 and A2 have different terminations at the pad border
- Layout A1 is designed to enhance the charge multiplication also in the inter-pad region
- Layout A2 is designed to provide better timing performance

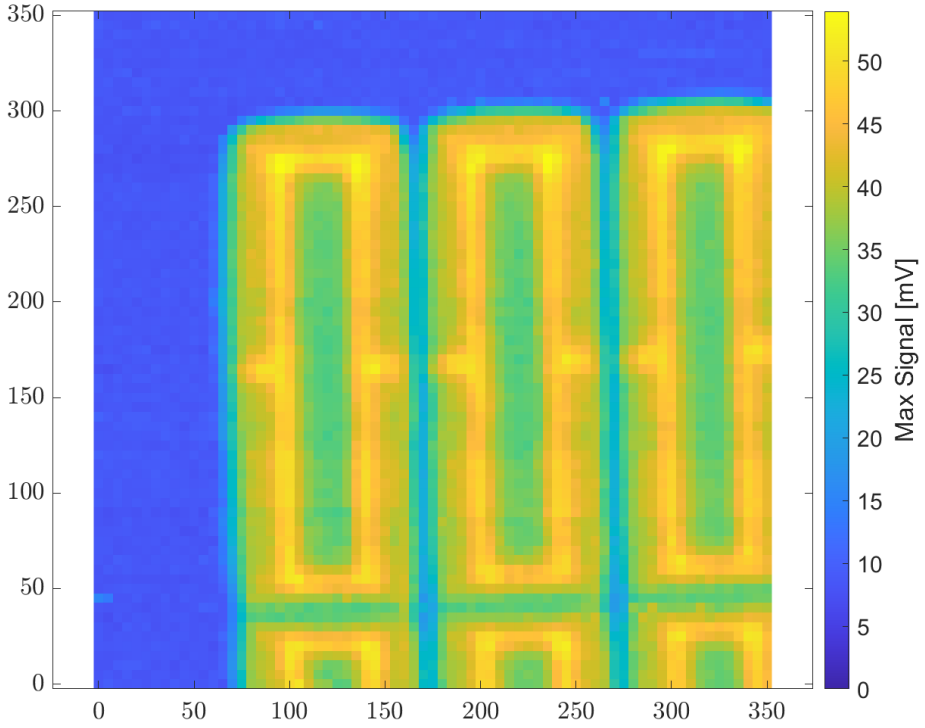


IR laser scan – Signal maximum

PM250 A1



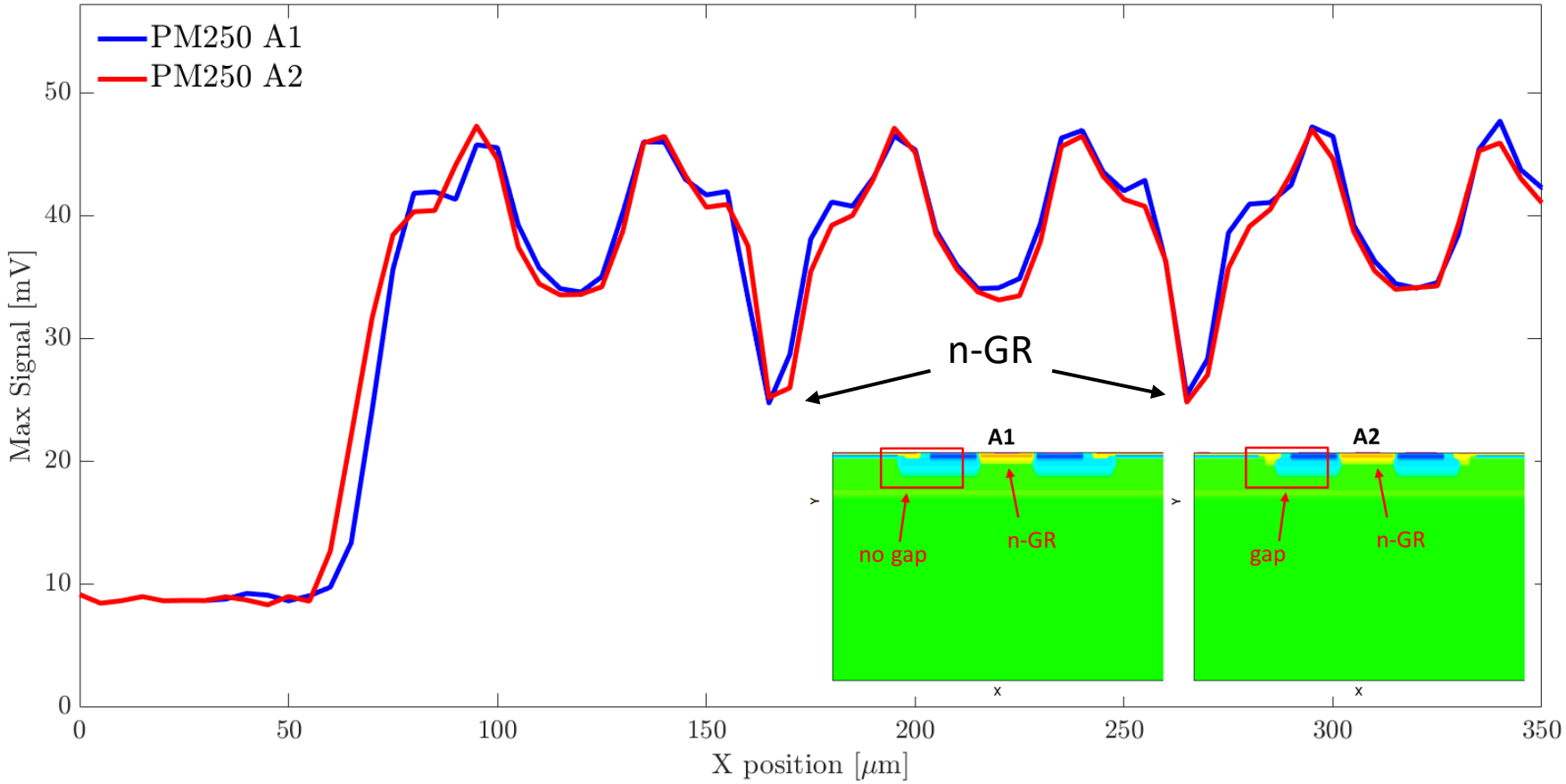
PM250 A2



- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Variation in the measured signal maximum due to reflection in the frontside metal

5 µm motor step

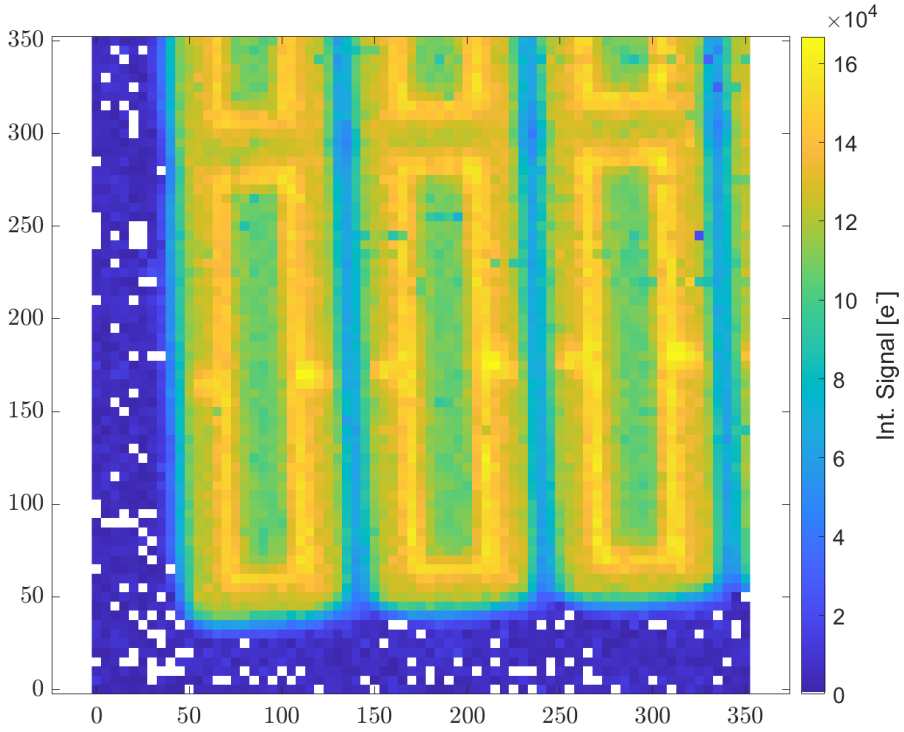
IR laser scan – Signal maximum



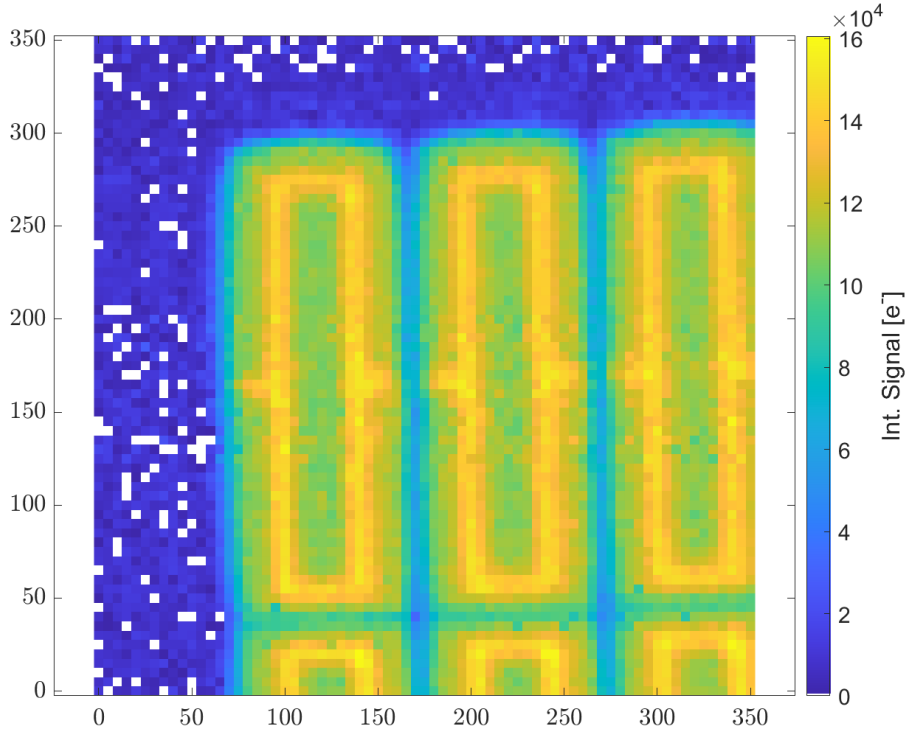
- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Similar maximum signal amplitudes for the two layouts

IR laser scan – Collected charge

PM250 A1



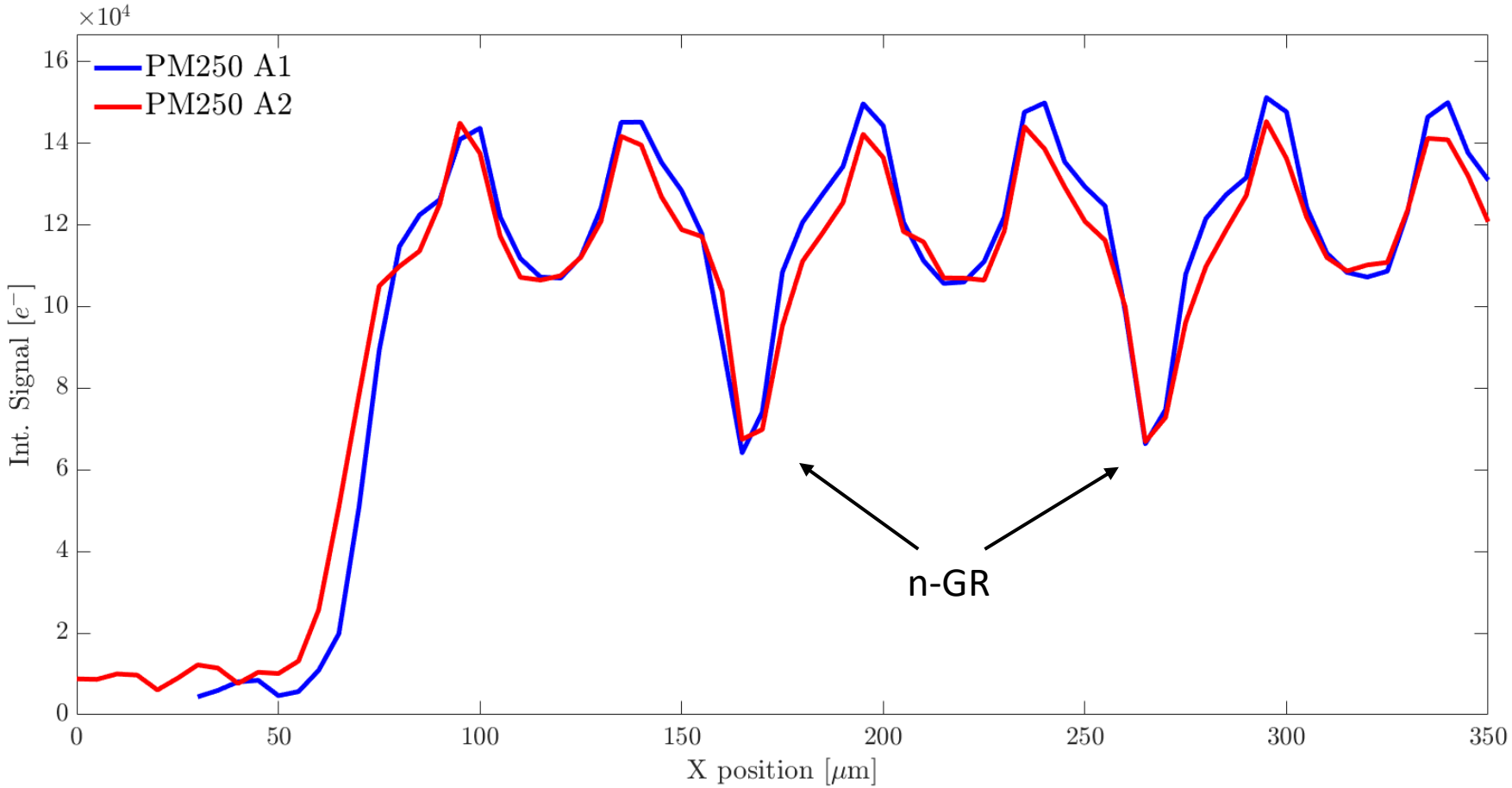
PM250 A2



- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Non uniform charge collection due to effect of frontside metals and contacts

5 µm motor step

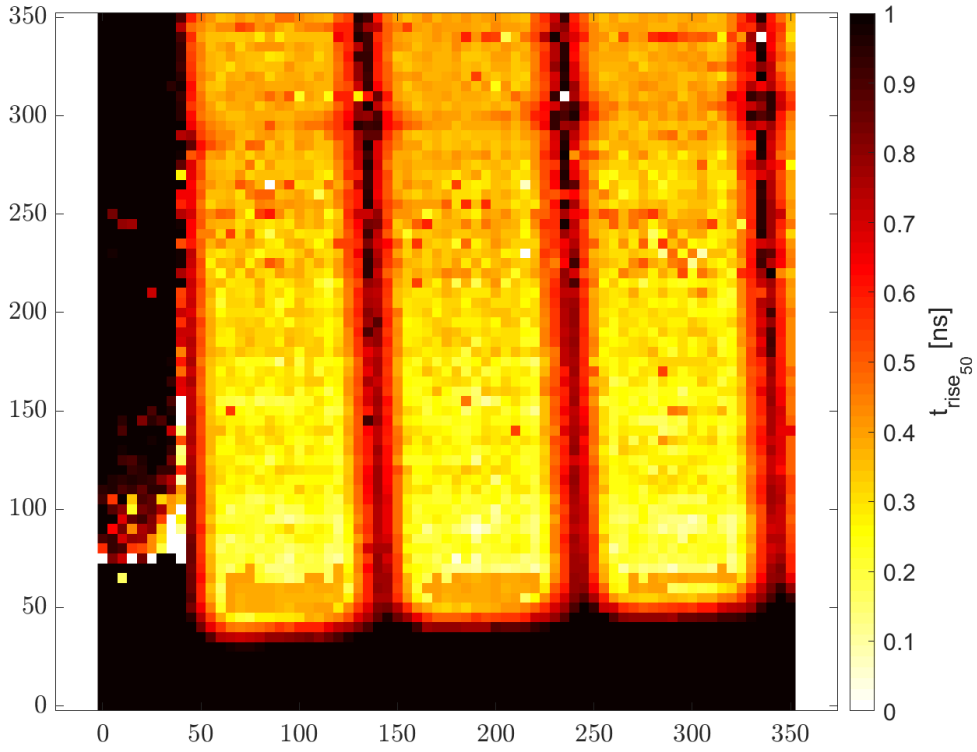
IR laser scan – Collected charge



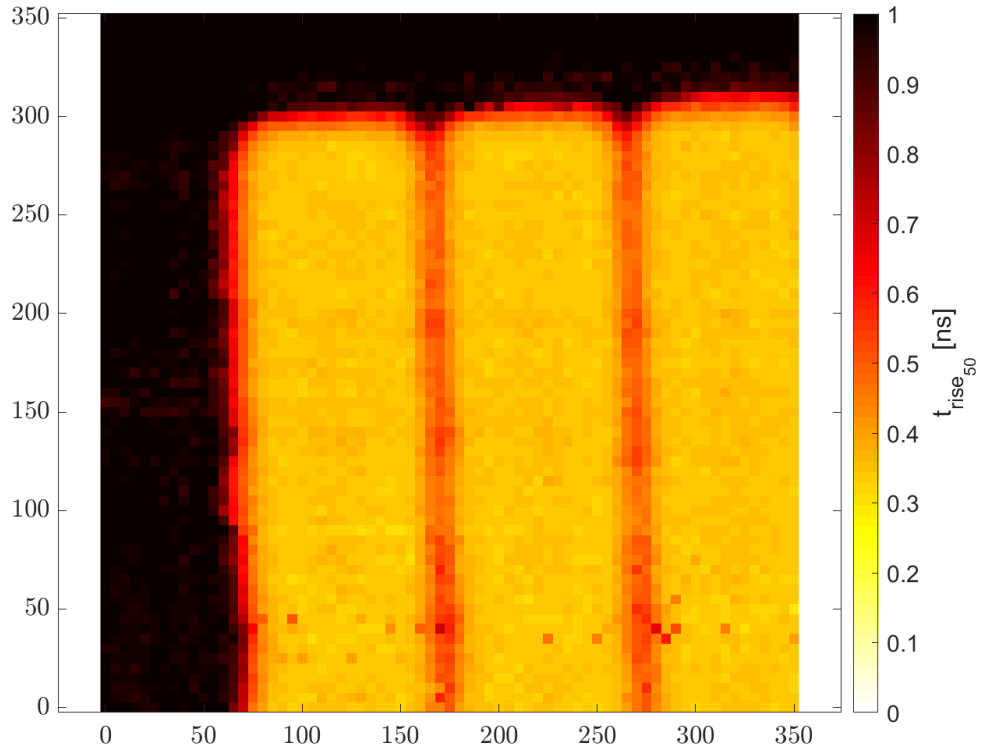
- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- As expected, the layout A1 enables to collect a slightly higher amount of charges at the pad borders

IR laser scan - $t_{rise_{50}}$

PM250 A1



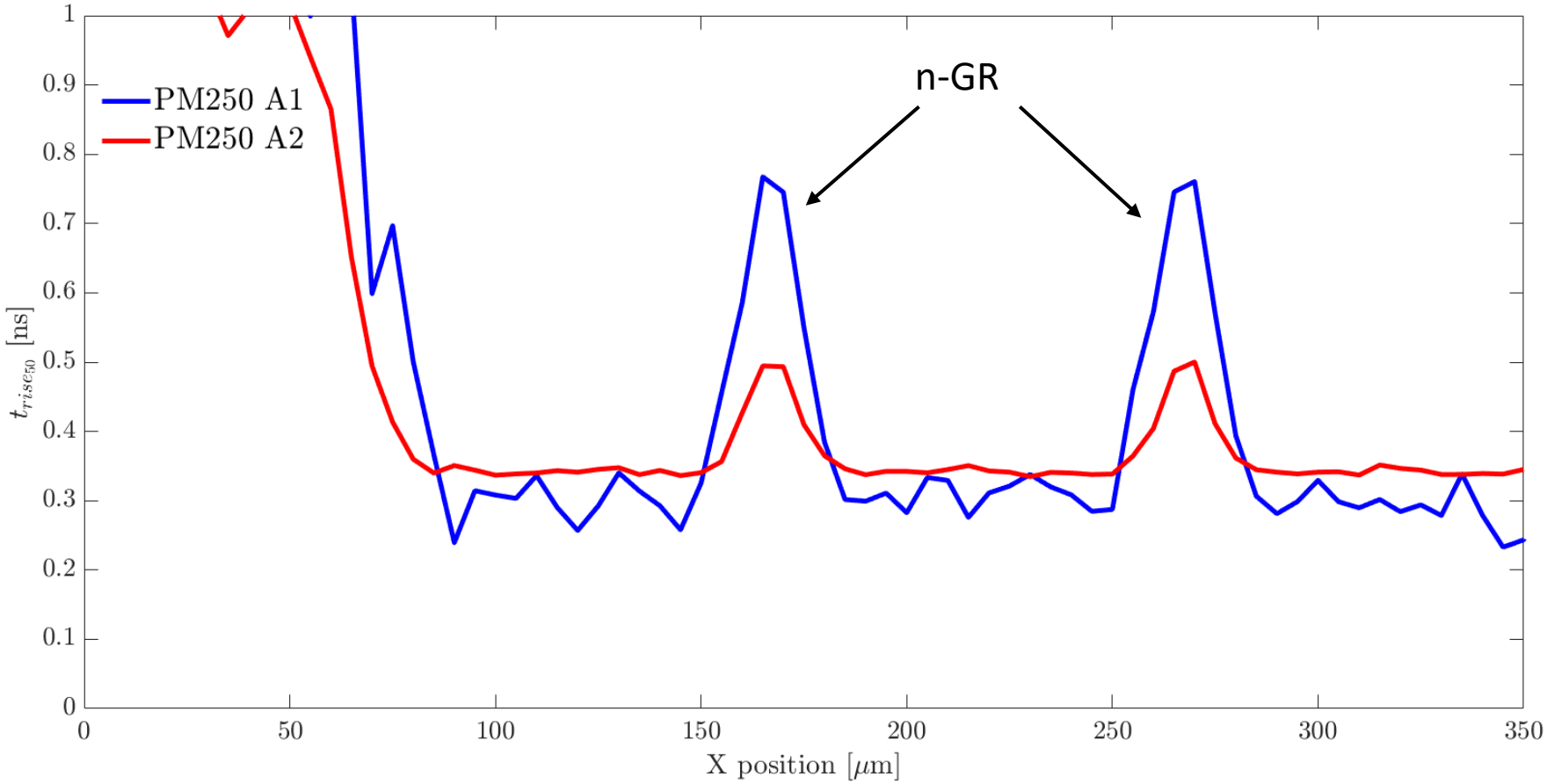
PM250 A2



5 µm motor step

- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Relevant increase in the rise time at the pad border for PM250 with layout A1
- More uniform timing response for layout A2

IR laser scan - $\mathbf{t_{rise_{50}}}$



- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Relevant increase in the time needed to reach 50% of the signal rising edge at the pad border
- More uniform timing response for layout A2

Conclusions

- Demonstrated the feasibility of integrating a gain layer with a process add-on
- Absence of breakdown and punch through issues at the foreseen operating V_n and V_{bias}
- Evaluated effect of the layout of the pad border on timing and collection efficiency performances
- New engineerig run with new gain layer profile will be submitted soon

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The ARCADIA collaboration

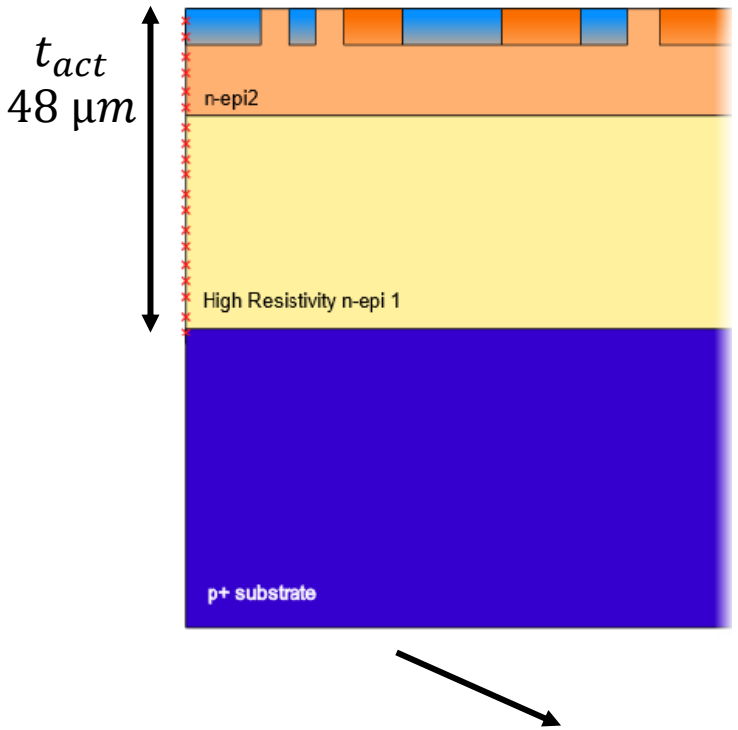
F. Alfonsi, G. Ambrosi, A. Andreazza, E. Bianco, G. Balbi, S. Beolè, M. Caccia, A. Candelori, D. Chiappara, T. Corradino, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, B. Di Ruzza, A. Di Salvo, S. Durando, D. Falchieri, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. Giampaolo, N. Giangiacomi , P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, S. Mattiazzo, C. Neubüser, F. Nozzoli, J. Olave, L. Pancheri, D. Passeri, A. Paternò, M. Pezzoli, P. Placidi, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, H. Roghieh, R. Santoro, A. Scorzoni, L. Servoli, F. Tosello, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, P. Zuccon

Thank you for your attention!

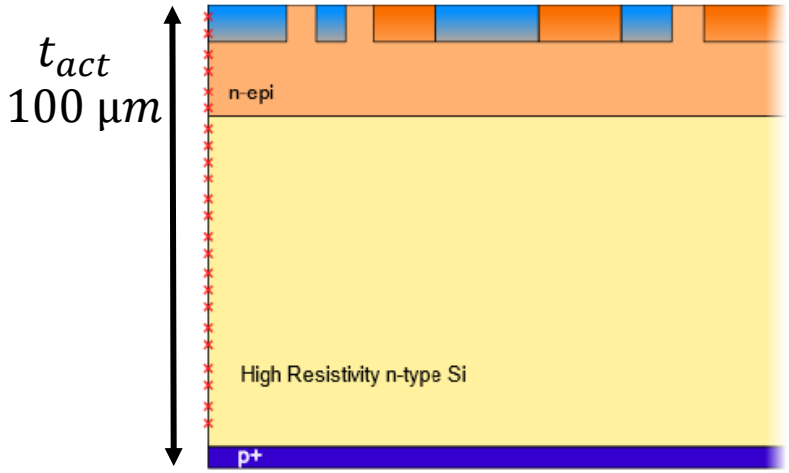
Backup

Substrate types

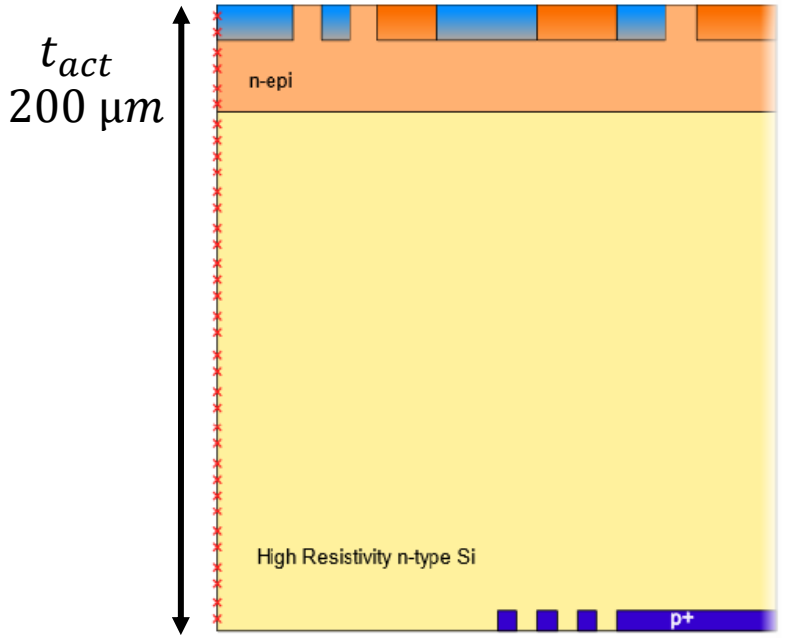
Type A



Type B



Type C

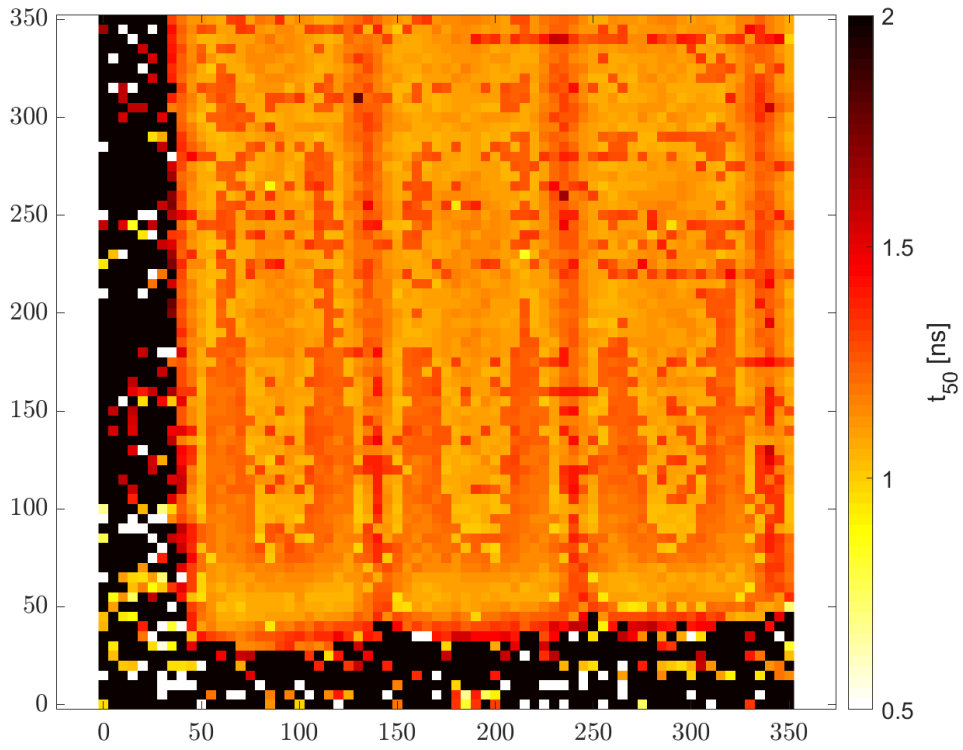


Both frontside and backside bias available

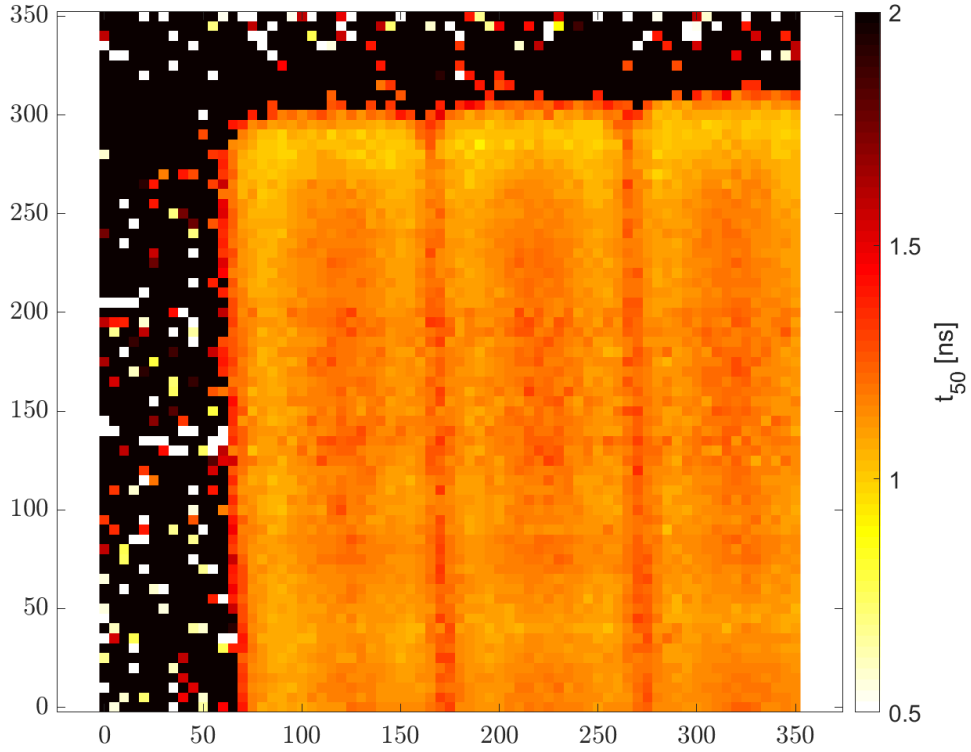
Only backside bias

IR laser scan - t_{50}

PM250 A1



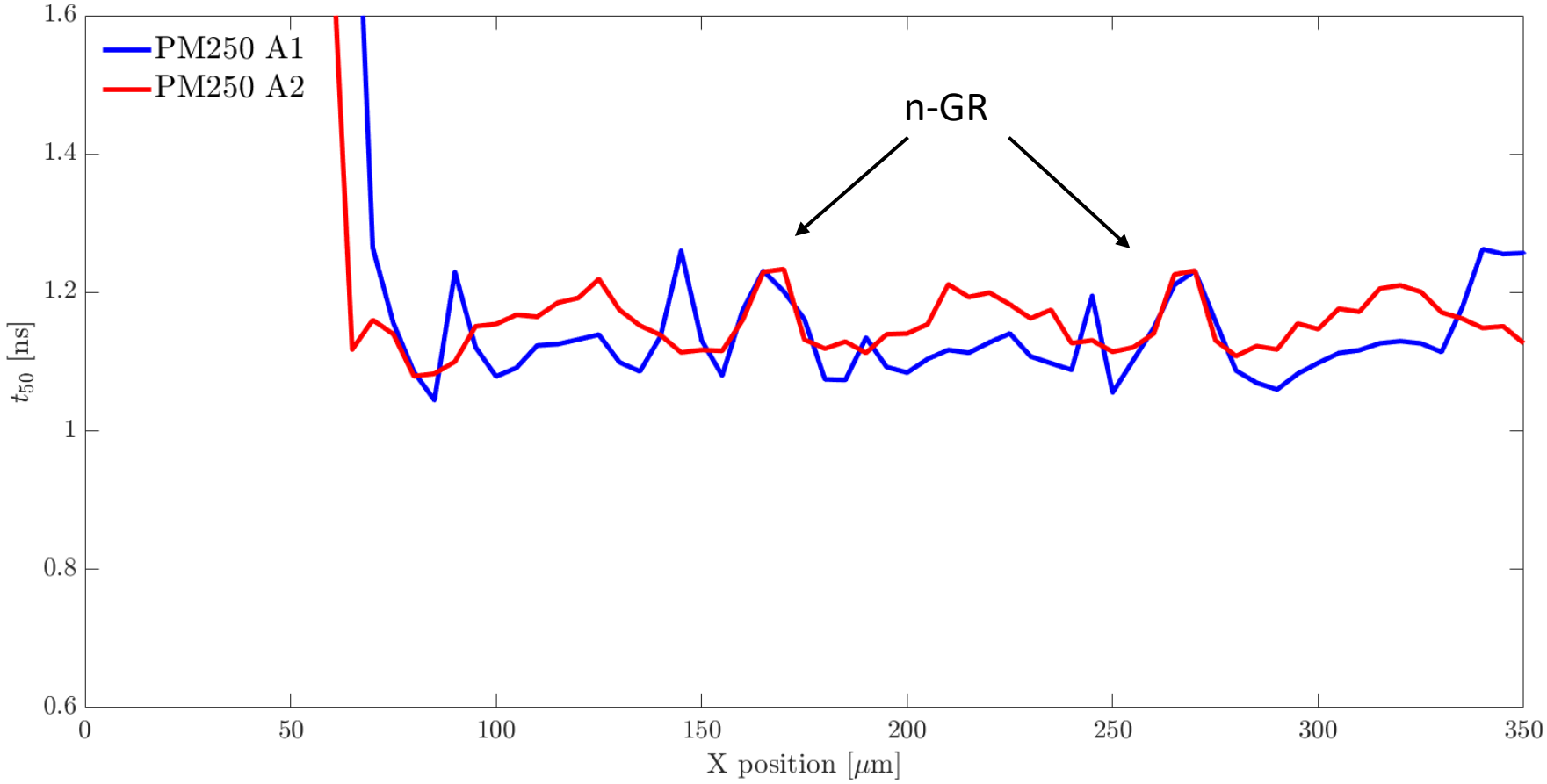
PM250 A2



5 µm motor step

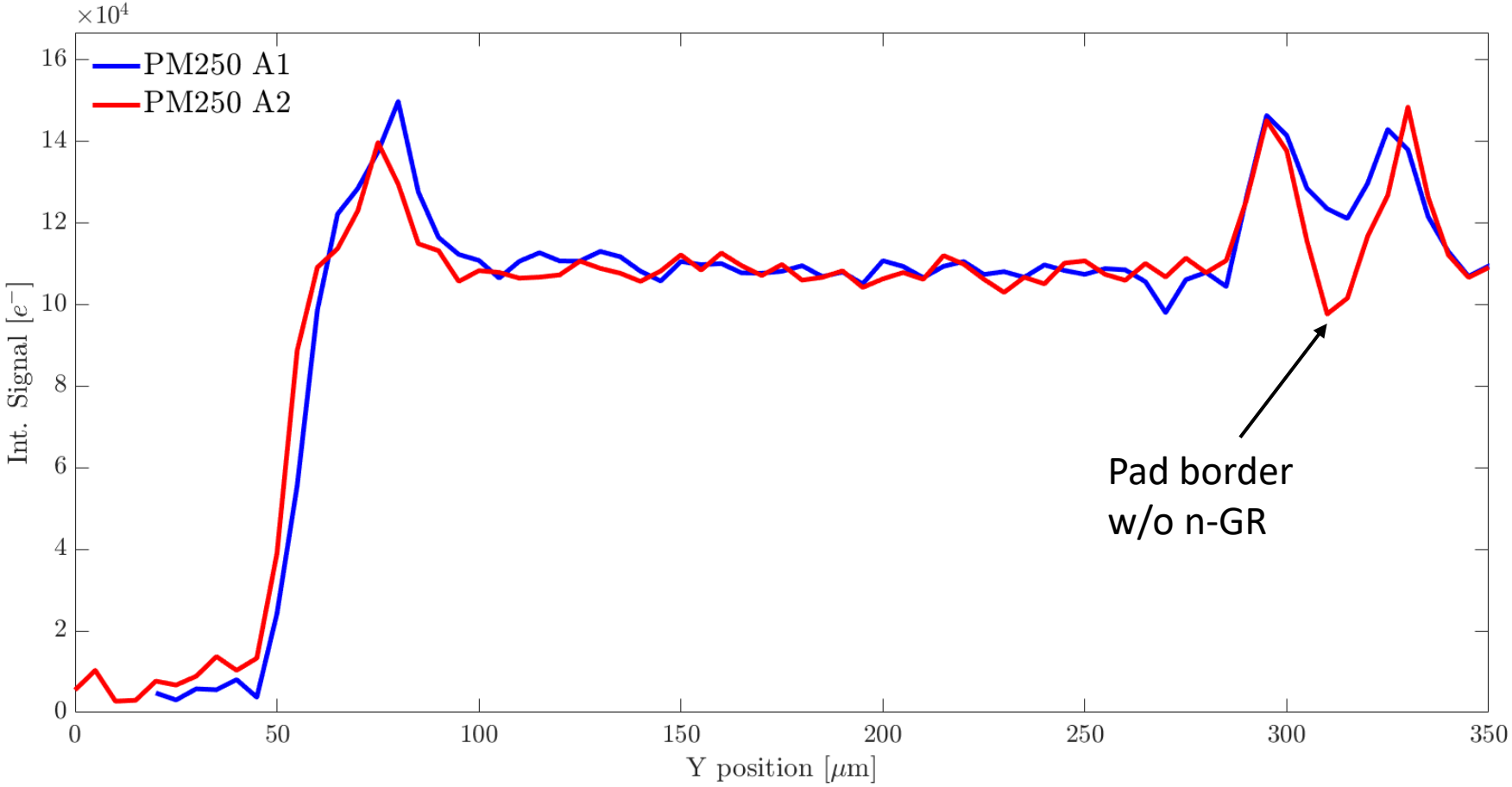
- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Slower charge collection near the frontside n-GR
- Time needed to collect 50 % of the generated charges around 1 ns

IR laser scan - t_{50}



- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Slower charge collection near the frontside n-GR
- Layout A1 results in a slower charge collection at the pad borders

IR laser scan – Collected charge



- $V_n = 40V$
- $V_{bias} = -35V$
- Focused laser spot
- Higher amount of charges collected in the inter-pad region for layout A1