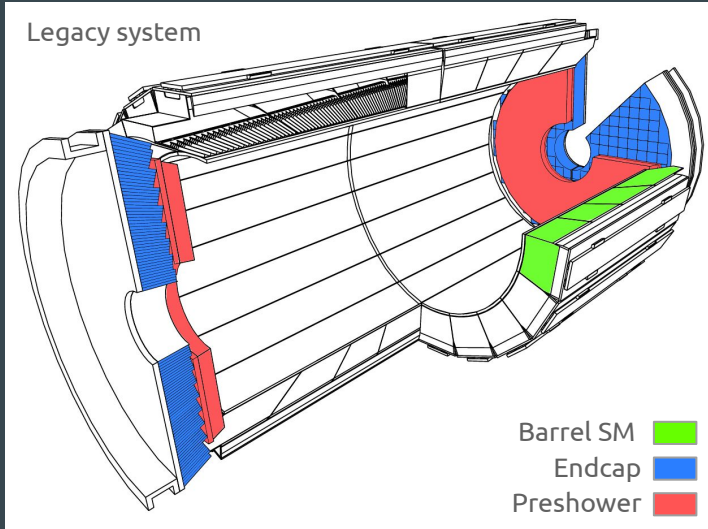# The upgrade of the CMS Electromagnetic Calorimeter for HL-LHC

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IPRD23, 25-29 September, Siena

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on behalf of the CMS Collaboration

CMS ECAL

Legacy system

Barrel SM
Endcap
Preshower

Lead-Tungstate crystals
VFE card   LVRB   FE card
Strip FENIX ASICs
TPG FENIX ASIC
DAQ FENIX ASIC
GOL mezzanines
TP link
DAQ link
Slow / fast control
APDs   MGPA   ADC

CMS Electromagnetic Calorimeter:

- Barrel
  - $|\eta| < 1.48$
  - 61200 $PbWO_4$ crystals
  - Light collection: avalanche photodiode (APD)
- Endcap
  - $1.48 < |\eta| < 3.0$
  - 14648 $PbWO_4$ crystals
  - Light collection: vacuum phototriode (VPT)
- Preshower
  - 4288 silicon sensors
  - $1.65 < |\eta| < 2.6$
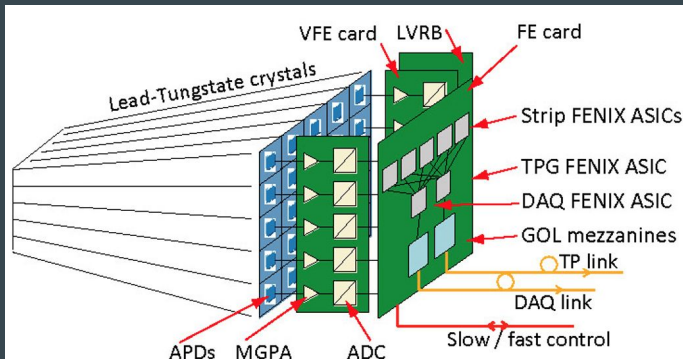
The barrel is divided in 36 supermodules (SM)

Electronics readout unit: 5x5 crystals

- strip of 5 crystals read by a Very Front End card
- 5x VFEs read by a Front End card
- a FE communicates with off-detector electronics (data/triggers/clock/commands)

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ECAL Upgrade differences due to HL-LHC

Barrel APDs and crystals will stay in place thanks to their limited radiation damage

Main differences from legacy system

- Endcaps and Preshower will be replaced by highly granular silicon calorimeter (HGCAL)

- Operating temperature from 18 °C to 9 °C

- New on-detector electronics with faster signal shaping and sampling

- New off-detector electronics

Why?

- Endcap crystals would not sustain the HL-LHC radiation levels

- Dark current reduction in APDs to mitigate effects on time and energy resolution

- Improved time resolution (30 ps for energy > 50 GeV)
- Improved recognition of **signals from direct ionization of APD (spikes)** -> expected 1 MHz rate above 20 GeV!

- 750 kHz trigger rate + ~12 µs of L1 latency
- Single crystal Trigger Primitives for pileup mitigation and spike reduction

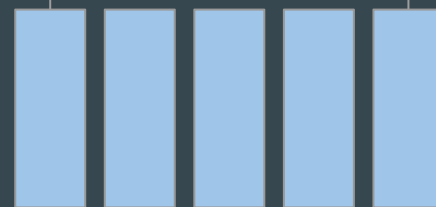# Very Front End Card

Main components

- **x5 CATIA Asics:**
  - Two gains amplification (x1-10)
  - Dynamic range: 50 MeV - 2 TeV energy deposition
  - Faster signal forming and higher bandwidth: 0-50MHz
  - Technology: CMOS 130 nm

- **x5 Lite-DTU Asics:**
  - Two 12 bits 160 MS/s ADCs (vs 40 MS/s of the legacy system)
  - Data Compression with low energy signals and Transmission Unit
  - Fast command and lock control units
  - Technology: CMOS 65 nm
 - 1.28 Gb/s serializers
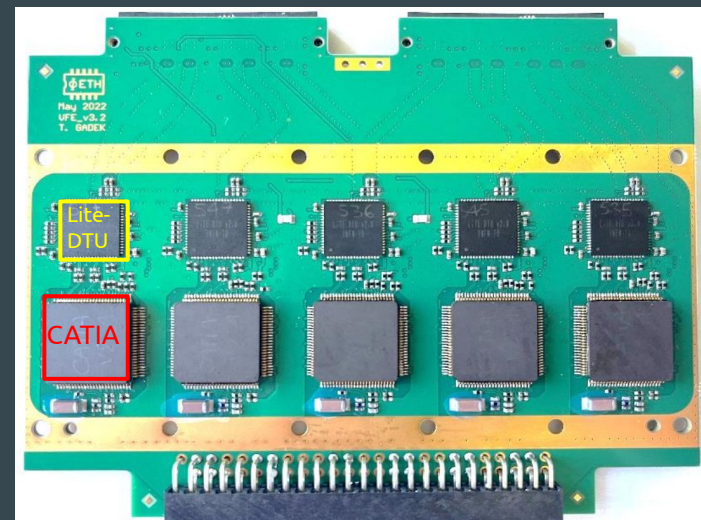
...x5 crystals...

Front End Card

Main differences from legacy system

- No Trigger Primitives Generator or Spikes Killer algorithm
  - moved to off-detector card
- The card collects data from 5 VFEs and sends them "immediately" to the off-detector card (limited FIFO buffering)

Main components

- **4x LpGBTs [2]:**
  - Readout of Lite-DTUs data via e-links at 1.28 Gb/s
  - Configuration of the VFE devices via I2C
  - Clock distribution via e-clocks

- **1x GBT-SCA [3]:**
  - collecting temperature values
  - readout of APDs dark current

- **1x VTRx [1]:**
  - 4x uplink 10.24 Gb/s fibers for data transmission
  - 1x downlink 2.56 Gb/s fiber for clock, fast and slow commands
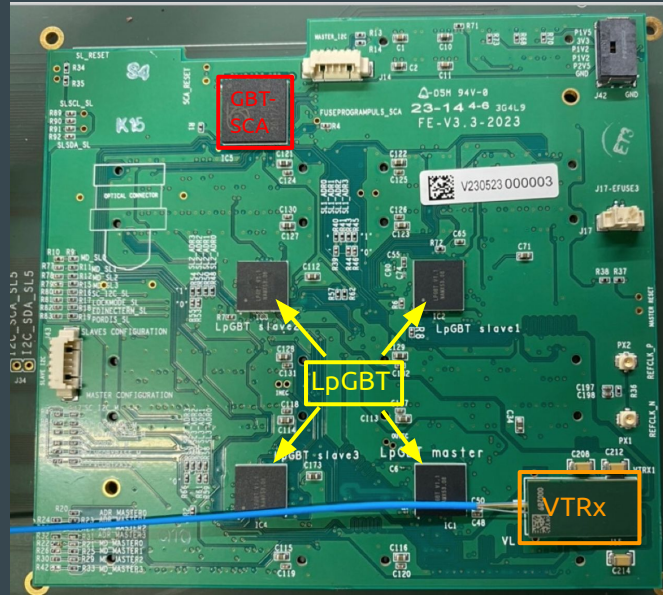
...x25 elinks, x25 eclocks and more...

Barrel Calorimeter Processor Card (v1)

Main differences from legacy system

- One single card for data, trigger and control functionalities
- Buffering for L1 latency **only** at this level
- From VME to ATCA standard

Main components

- Intelligent Platform Management Controller (IPMC)
  - Power controller and card monitor
  - ZYNQ7000 ARM/FPGA
- Embedded Linux Mezzanine (ELM)
  - Service environment and fast FPGA access
  - ZYNQ7000 ARM/FPGA
- Main FPGA
  - XCKU115 FPGA
  - control and clock distribution system for on-detector electronics
  - **trigger primitives generation from single crystals signals**
  - data acquisition from detector and cDAQ transmission
- MTPs + Firefly for Readout Towers and TCDS/DTH communication
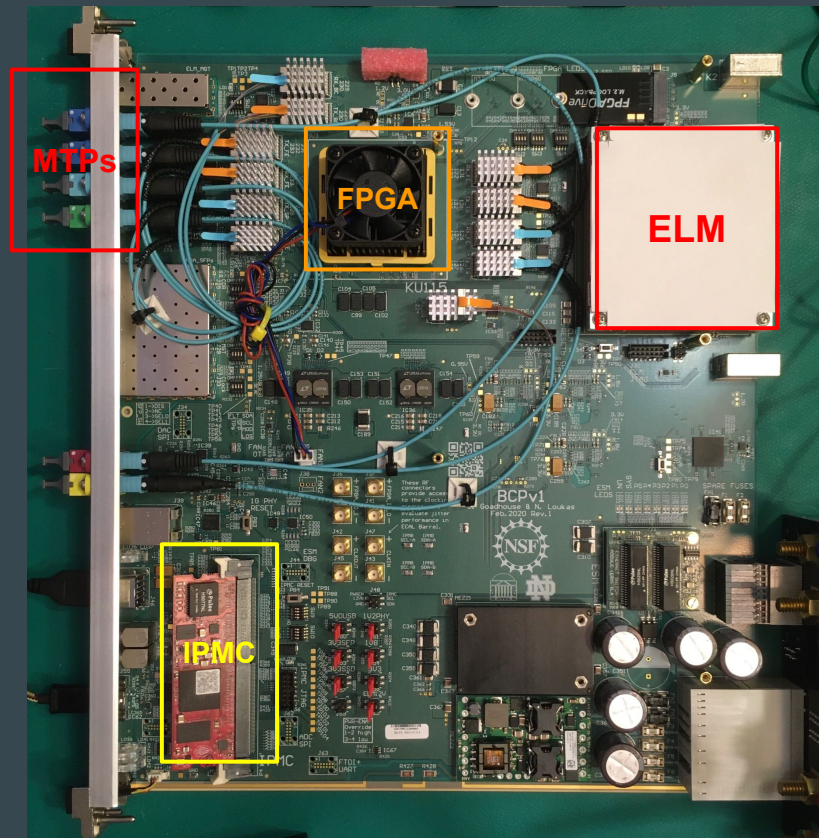
Prototype of ECAL/HCAL BCP card (v1)

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Barrel Calorimeter Processor Card
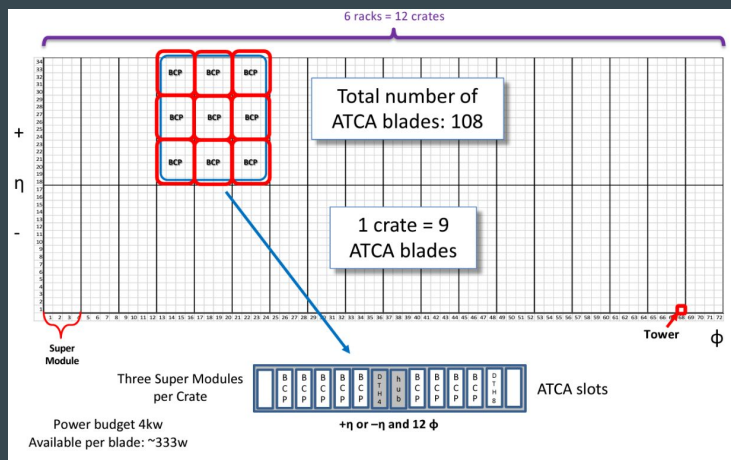
- One BCP card will be in charge of controlling up to 24 towers
- 3x BCPs to cover one SM
- 108x for the full Barrel
- 1x ATCA crate:
  - 9x BCPs
  - 1x HUB for ethernet connection
  - 2x DTH for data sending and clock/commands receiving
- BCP will support shared links among neighbor BCP processors boards:
  - It will allow to run algorithms requiring multiple crystal signals like "swiss cross" spike rejection or cluster TPs generation
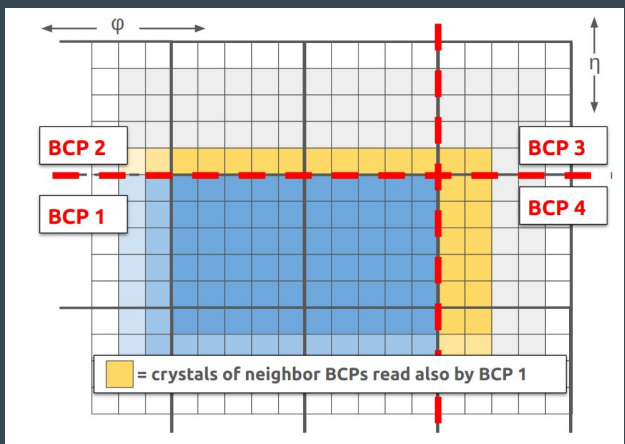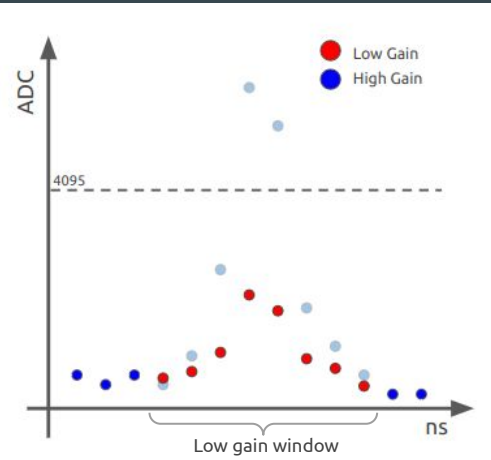
BCP trigger primitives algorithm

The Trigger Primitives generation will be one of the main activity of the BCP FPGA. Three main algorithms will be applied to the data extracted:
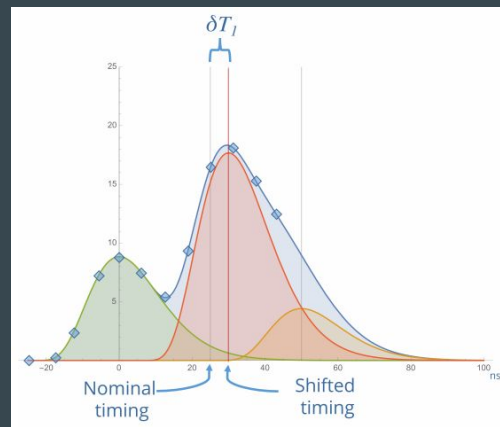
Linearization:

Digitized samples are subtracted by the baseline pedestals and multiplied by their gain

Amplitude and Timing Reconstruction

Based on **predetermined pulse shapes of crystals**, the amplitude and the arrival time of a pulse with respect to the LHC clock are extracted with a **linear least square method**, taking into account the ±1 bunch crossings pulses overlayed
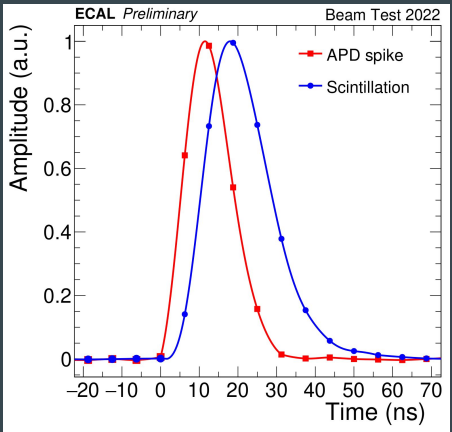
Spike rejection

Thanks to:
- sampling rate at 160 MHz
- shorter pulses
- single crystal information

spikes could be distinguished with a discriminant, built from the ratios of three consecutive linearized samples
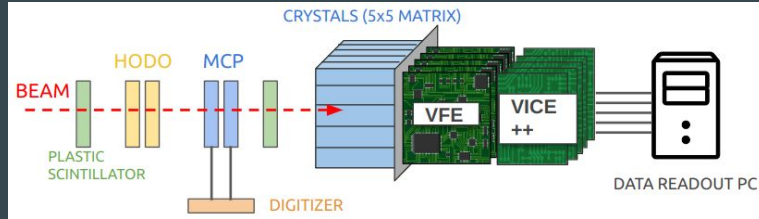
Test Beam

- Several campaigns have been performed to test the electronics prototypes under realistic conditions
    - Used the test beam facility of H4 Beamline at CERN
    - Very pure $e^{\pm}$ beam, pion beam
    - Energy from 20 to 200 GeV
- Performed energy scans to measure energy and time resolutions
- Hodoscope planes for beam position monitoring
- MCP detectors for time reference (read by 5 MS/s CAEN V1742 digitizer)
- Plastic scintillators to trigger the readout
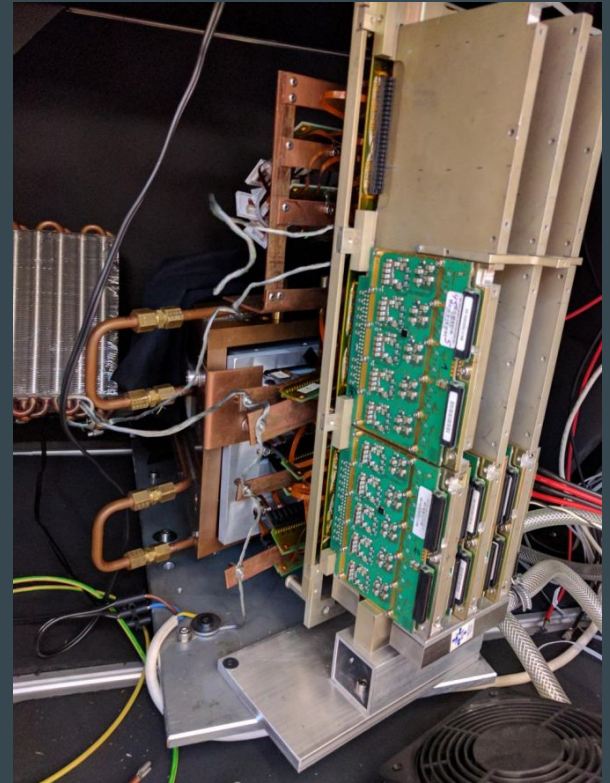
Test Beam

2018 - 2021 campaigns

- First VFE prototypes read individually by custom readout boards (VICE++)
- Single matrix of 5x5 crystals in a temperature controlled box


2022 and 2023 campaigns, used the full DAQ chain:

- 9x towers in a real spare SM have been equipped with new VFEs and FEs
- Readout performed by two BCP cards v1
- Trigger logic and modes handled by a CAEN DT5495 board

Beam direction
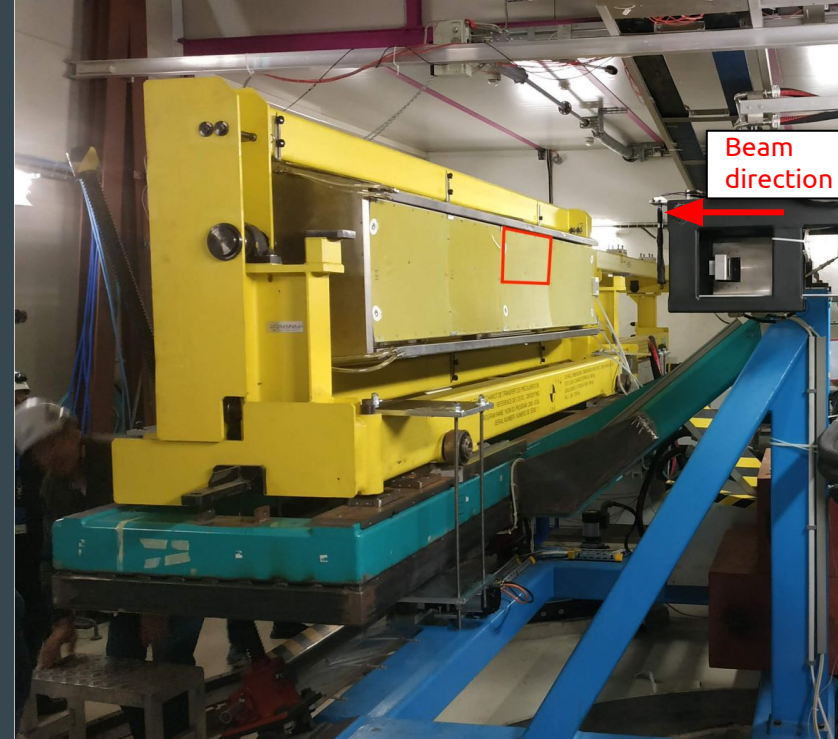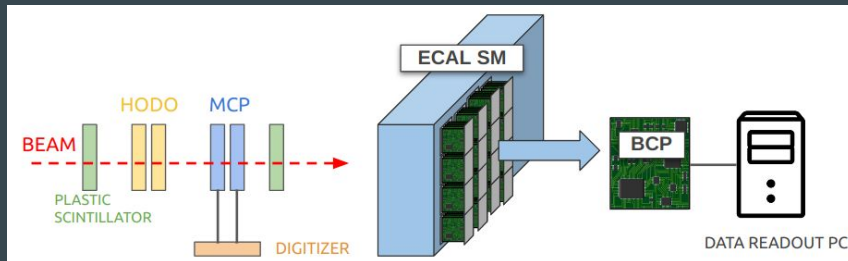
Test Beam and results from Nov 2021

Time resolution:

- Signal maximums aligned (neglecting the chance of loss of sync)
  - t from template fit to pulse shapes
- Templates from pulse shapes oversampled in the frequency domain
- Run with beam across 2 channels on the same VFE

ECAL Test Beam 2021

• ECAL Single channel

$\frac{N}{E} \oplus C$

N = 0.92 ± 0.02 ns

C = 12.9 ± 0.4 ps
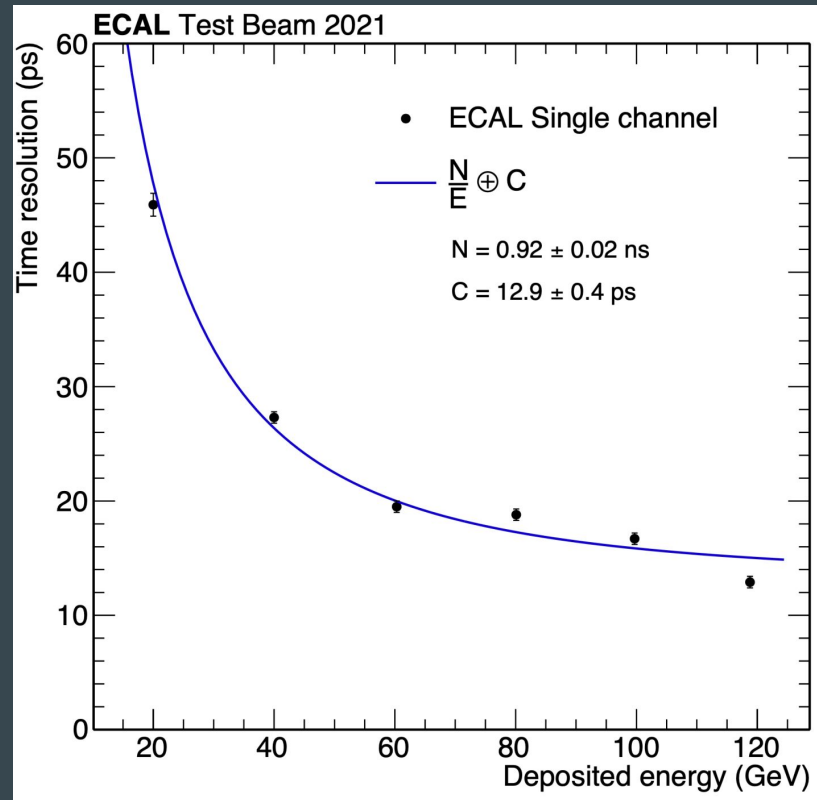
Irradiation and Ageing tests

- Irradiate one full tower close to future CMS conditions

- CERN Mixed-Field irradiation Facility (CHARM) in July 2023

- Got 67.7 Gy/day accumulated doze by the mixture of 41.3%n, 19.5%p, and 35.6% pion

- Obtained TID at CHARM: ~ 1.4 kGy (correspond to ~24% of HL-LHC runtime)

- Future second irradiation: PSI proton beam >200% dose

During irradiation:

- Data readout via BCP card
- Periodic reconfiguration of the electronics
- Dark current measurement and spikes
- Data under studying
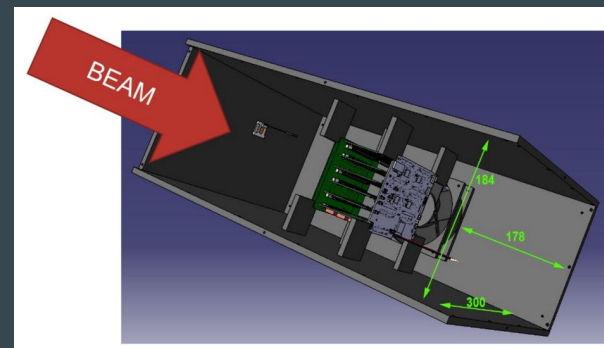
Timeline and summary
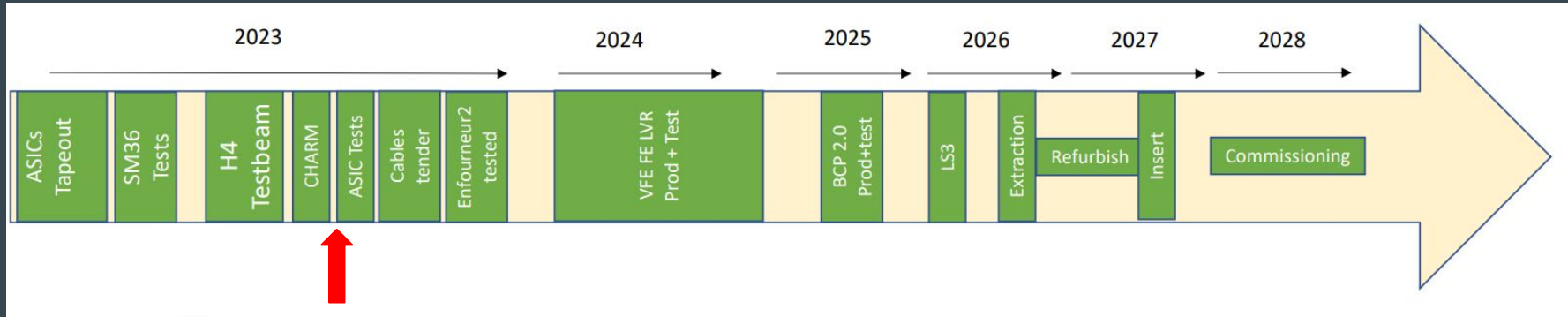
- The CMS Electromagnetic Calorimeter will go under a major upgrade of the electronics (on and off detector) to fulfill new HL-LHC requirements
  - 750 kHz trigger rate and 12 μs of L1 latency
  - ~200 pileup
- New electronics has been developed and ASICs (CATIA and Lite-DTU) are under production
- Trigger algorithms are under development
- DAQ chain tests (in lab or under beam condition) have already produced promising results
- **Final aim of 30 ps of timing resolution for energies above 50 GeV can be achieved**

Backup slides

Sources:
1) VTRx: Versatile Link PLUS
2) LpGBT: Low Power Giga Bit Transceiver
3) GBT-SCA: *Caratelli, A., Bonacini, S., Kloukinas, K., Marchioro, A., Moreira, P., De Oliveira, R. and Paillard, C., 2015. The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments. Journal of Instrumentation, 10(03), p.C03034.*

Spikes

- isolated large signals with equivalent energies that can exceed 100 GeV in CMS
- proportional rate to the collision rate of the proton beams
- particles (produced in pp collisions) striking the APDs and very occasionally interacting to produce secondaries that cause large anomalous signals through direct ionization of the silicon
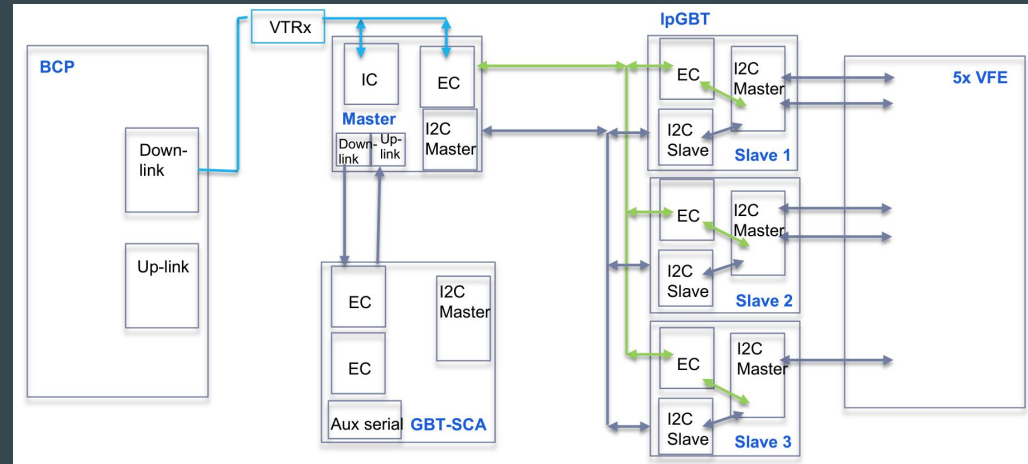- they will often satisfy the conditions for triggering electrons and photons in CMS
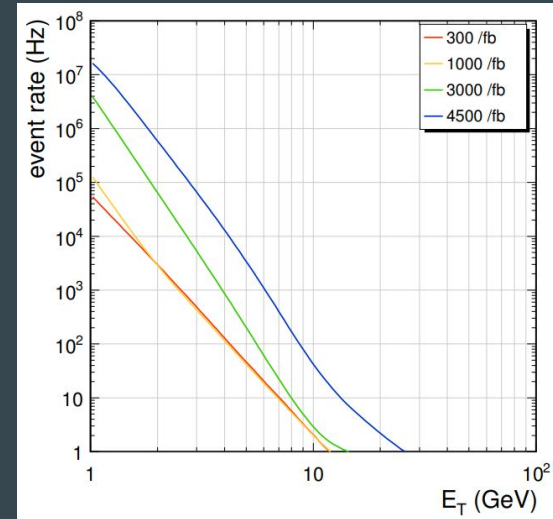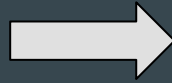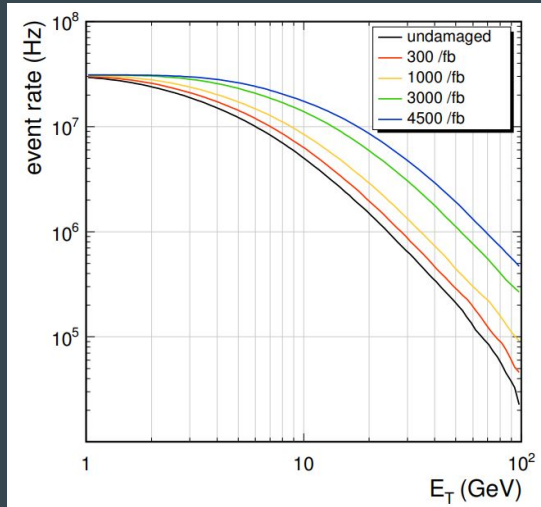
Expected rate of events with PU = 200 for Phase-2 with ECAL energy deposits above specific ET thresholds after 300, 1000, 3000, and 4500 fb−1 , assuming 2800 colliding bunches per LHC orbit. The contribution of ECAL spikes is included in this plot.

Event rate of EB energy deposits with spike hits above a specific ET threshold for Minimum Bias interactions at PU = 200 assuming 2800 colliding bunches per LHC orbit. This plot is produced assuming spike rejection using a pulse shape discriminating variable

Front End Card - Slow control

- One BCP card will be in charge of controlling up to 24 towers:
  - Configuration of the FE and VFE devices
  - ~4000 registers per tower
- BCP contacts Master LpGBT via IC protocol
- BCP contacts Slave LpGBTs via EC with M-Lpgbt in transparent mode
- Slave LpGBTs contact VFE devices via I2C
- Slave LpGBTs can also be contacted via Master I2C (but slow)
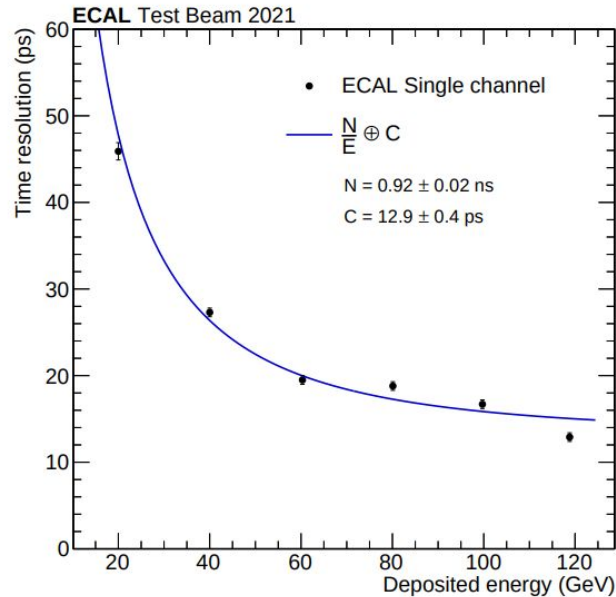
Aiming to a configuration time of 60-90 seconds

- 24 towers are configured in <u>series</u>
- BCPs can work in <u>parallel</u>
- Configuration software running on the ELM for fast FPGA memory access

Slow control schema of FE v3.3

Time resolution vs. deposited energy

ECAL Test Beam 2021

- ECAL Single channel
- $\dfrac{N}{E} \oplus C$

$N = 0.92 \pm 0.02$ ns
$C = 12.9 \pm 0.4$ ps

Time resolution (ps) vs. Deposited energy (GeV)

Time resolution as function of the deposited energy obtained in 2021 test beam data. The test was carried out using ECAL crystals equipped with prototypes of the Phase 2 upgraded Very Front End (VFE) electronics, and exposed to electron beams in the energy range between 25 and 150 GeV. The VFE prototypes embed the Phase 2 TIA and ADC ASICs. The time resolution is performed by comparing the time measurement over a single channel to that of an external timing reference detector placed along the beamline. The solid blue line represents the fit with the resolution function $\dfrac{N}{E} \oplus C$, where N denotes the noise, C the constant term, and E the deposited energy. The constant term of about 13 ps meets the requirements for the Phase 2 design.