Tools for Discovery

Multichannel Digital Readout Strategies for Next-Generation Physics Experiments

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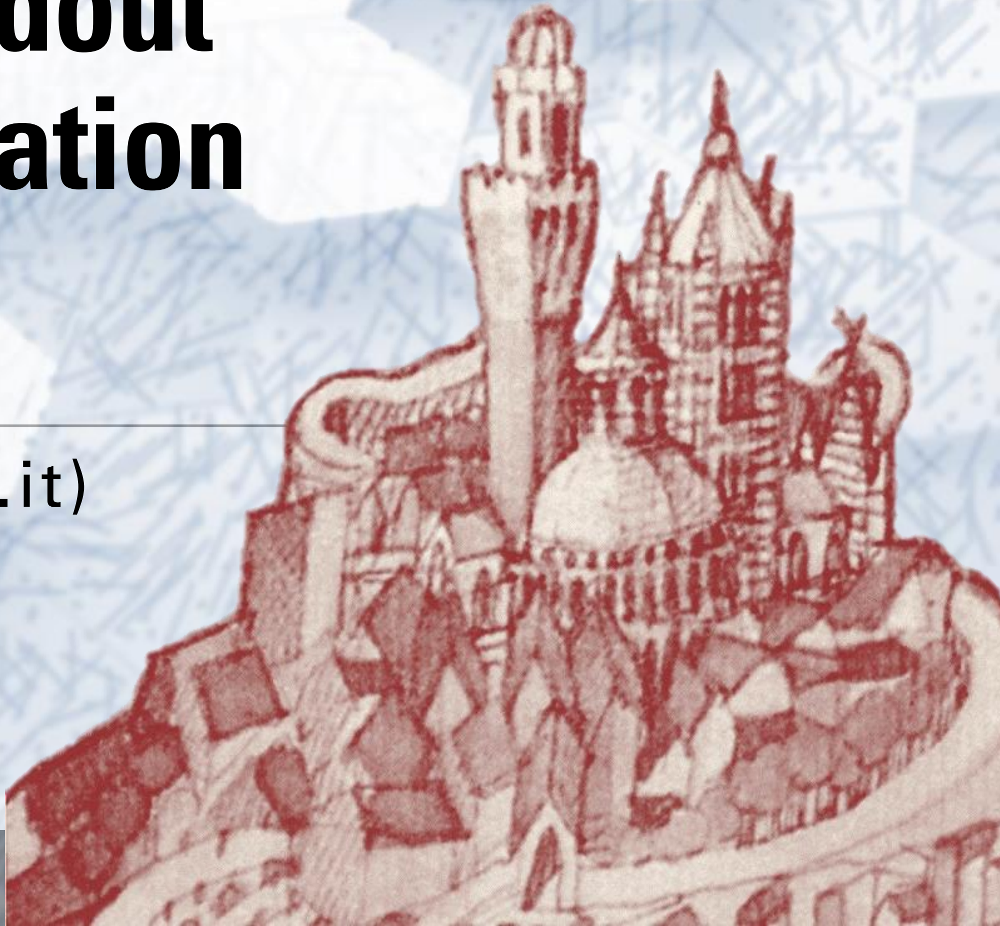
Siena - Italy



Overview

- **Next-Gen experiments** general architecture
- New electronics for new requirements
- **Digitizers 2.0** series
- **Frontend Readout Systems**
- Possible **future paths** for readout

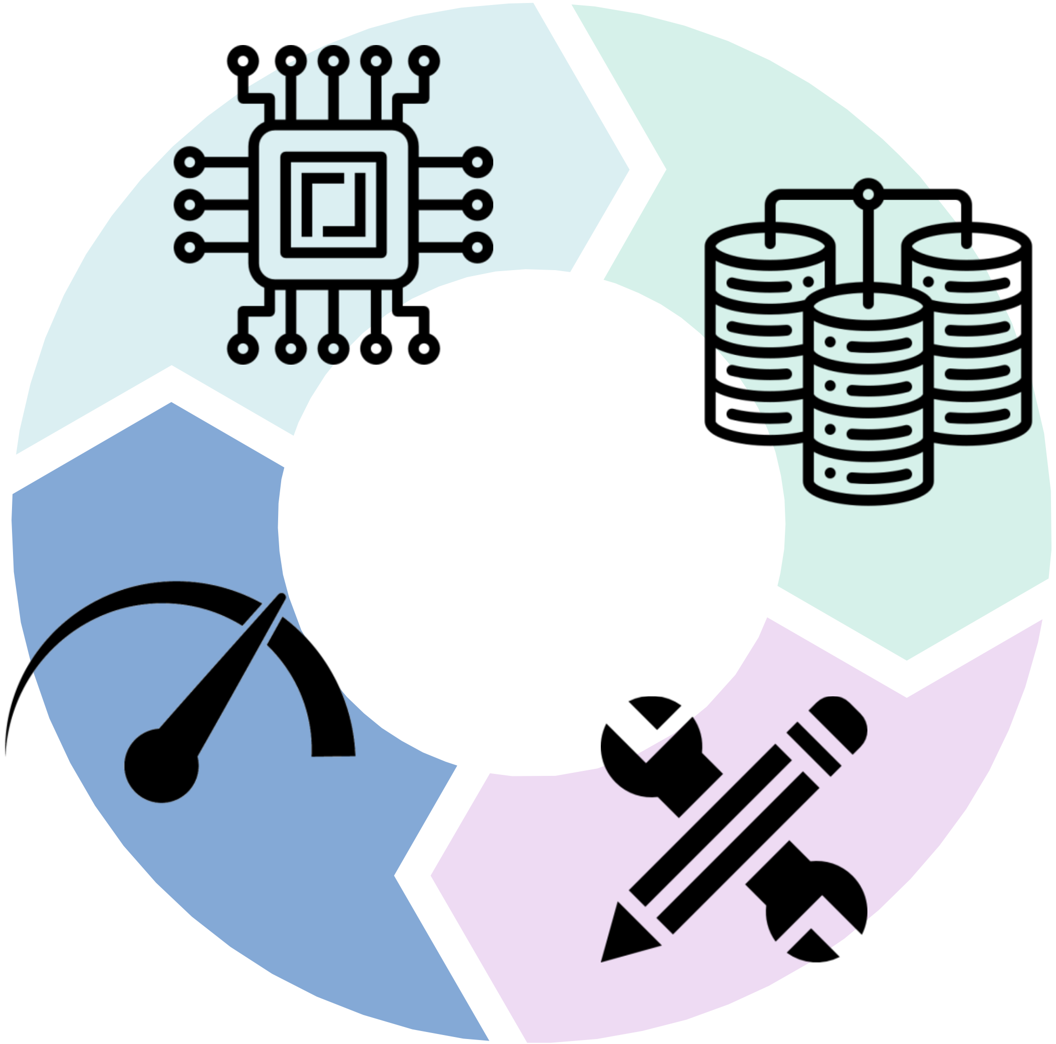
Challenges of new experiments

Miniaturization

Scale down in cost and high channel count → ~ 10,000 ch.

Big data

How to reduce storage cost?



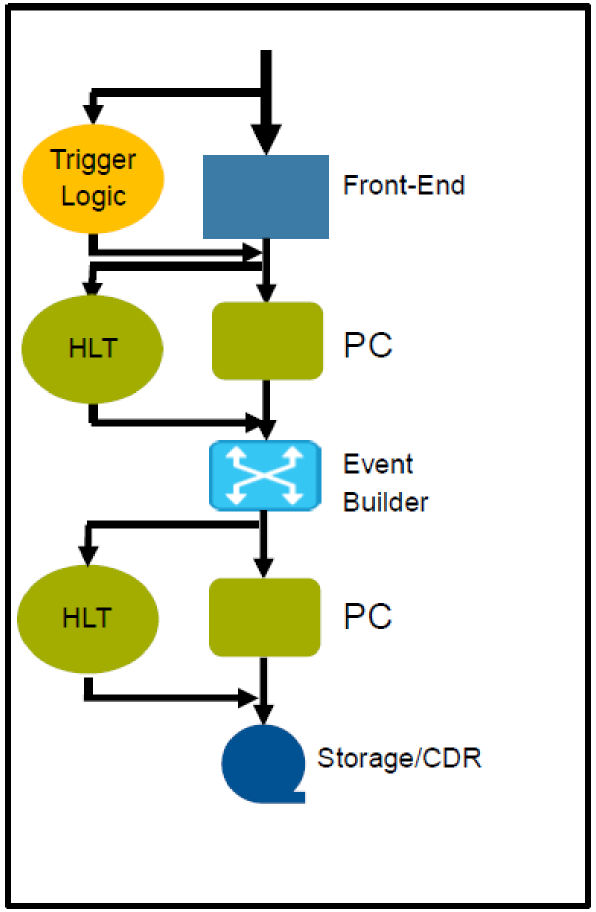
Triggerless

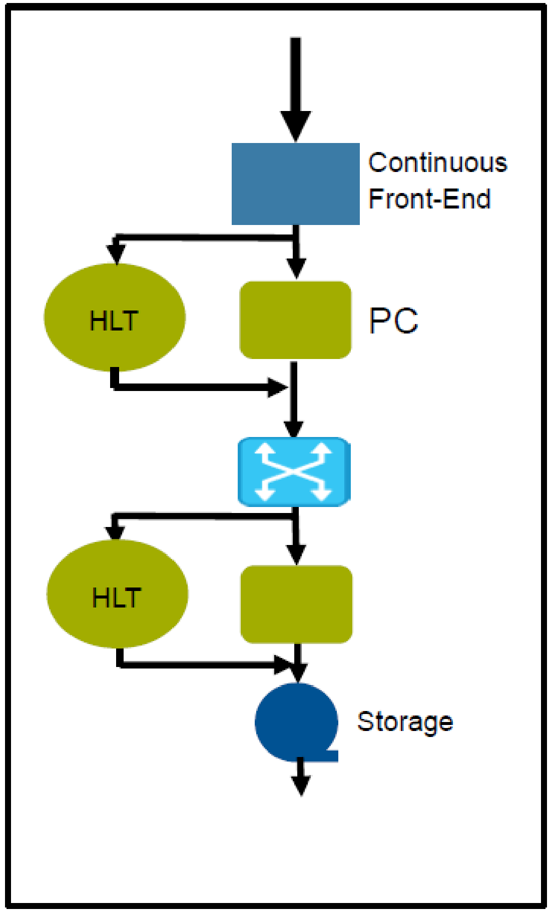
High data throughput

Customization

Implementation of specific processing algorithms

Evolution of pulse processing DAQ architecture



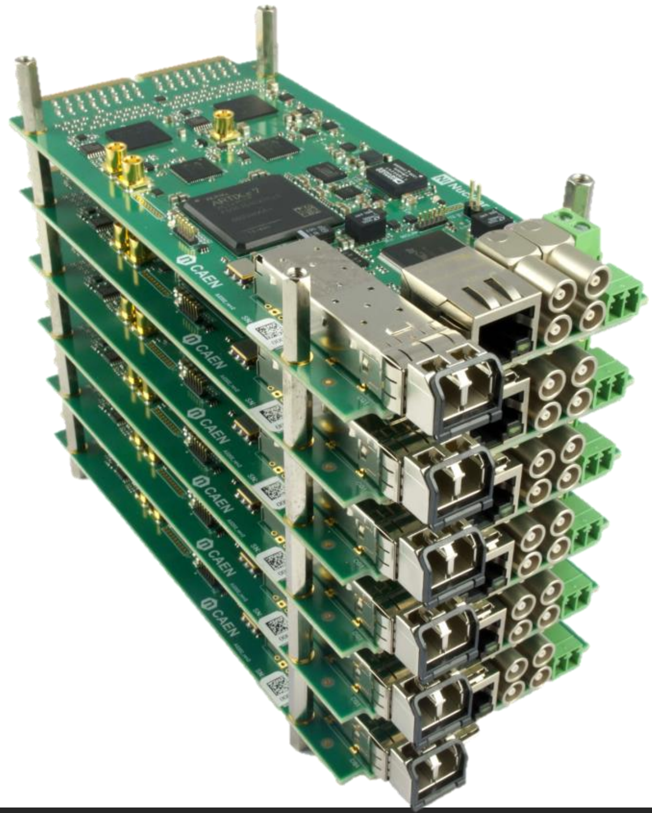


- Digitize continously
- Digital Pulse Processing
- Trasmit lot of data
- Event building and selection
- Online storage decision: no external big storage needed

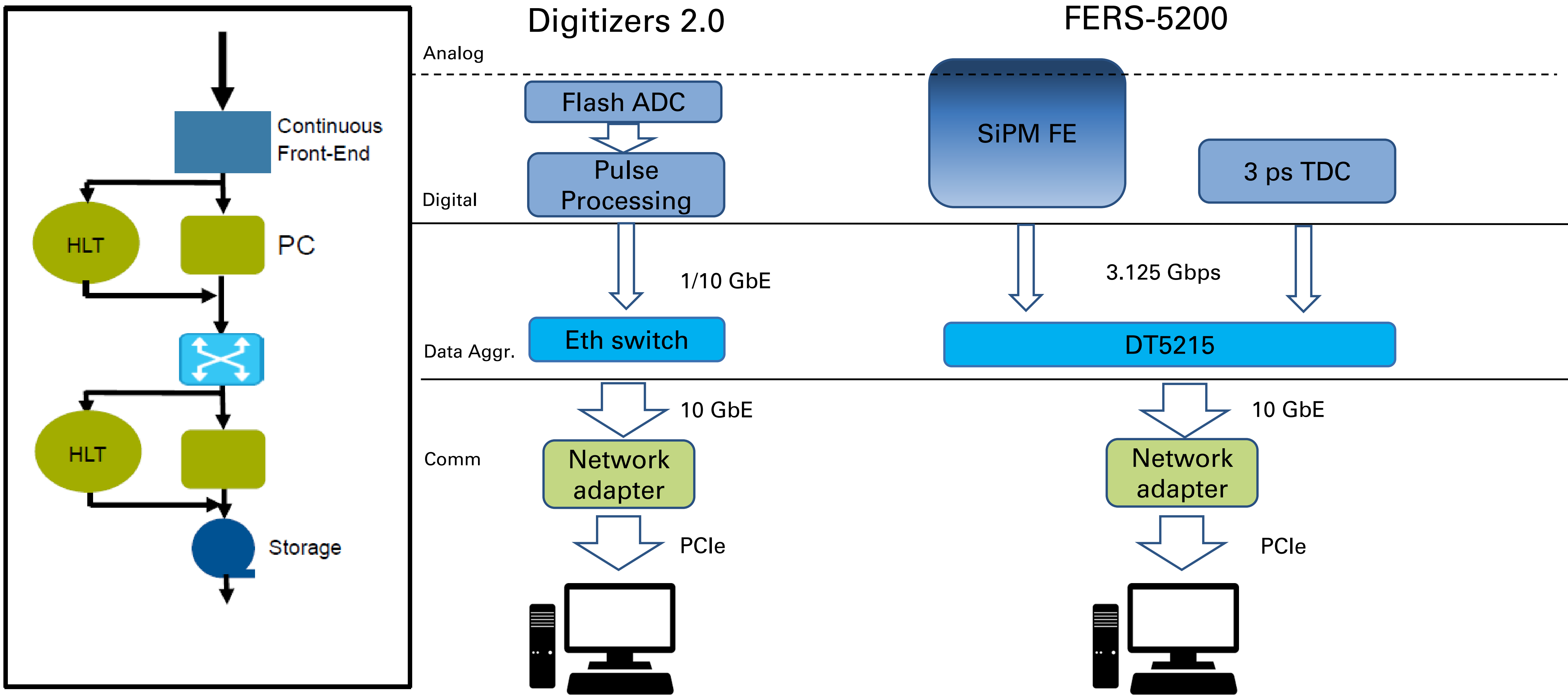
I. Koronov, TU Munich, Advanced Workshop on Modern FPGA-Based Technology for Scientific Computing, 2019

A new generation of digital electronics

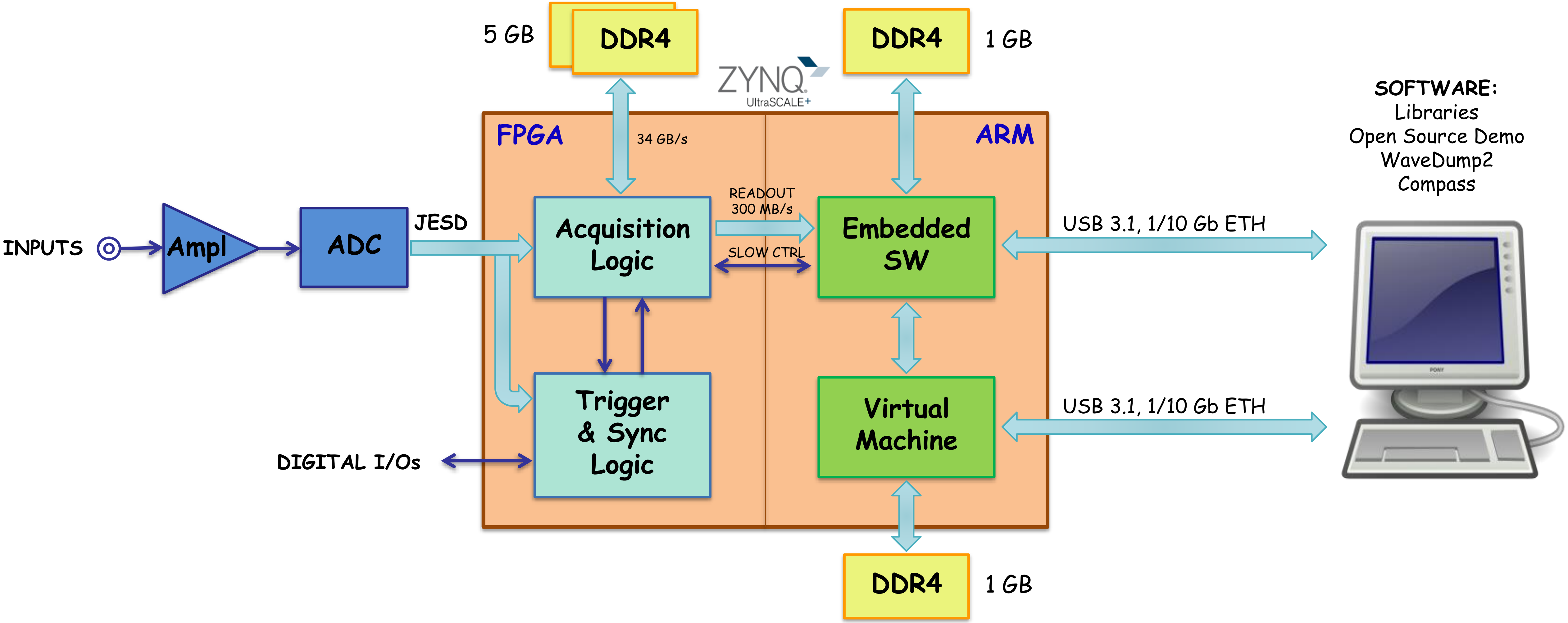
- Miniaturization → **dense/compact** solutions based on frontend ASICs
- High-data throughput → **fast communication links**
- **Custom pulse processing** → Open FPGA
- **Big data** → event building onboard



Experimental architecture



The Digitizer architecture



Digitizer 2.0 flavours

Available

VX2740/45

64 channels
125 MS/s
16 bit

Q4 2023

VX2730/25

32 channels
500/250 MS/s
14 bit

Q4 2024

VX2751

16 channels
> 1 GS/s
14 bit

and others…

Currently used by:

- *Numen (SSD, SiC, $LaBr_3$)*
- *Dark Side (Argon TPC)*
- *Tristan (multi pixel SDD)*
- *Agata 2π (SSD)*

Already requested by:

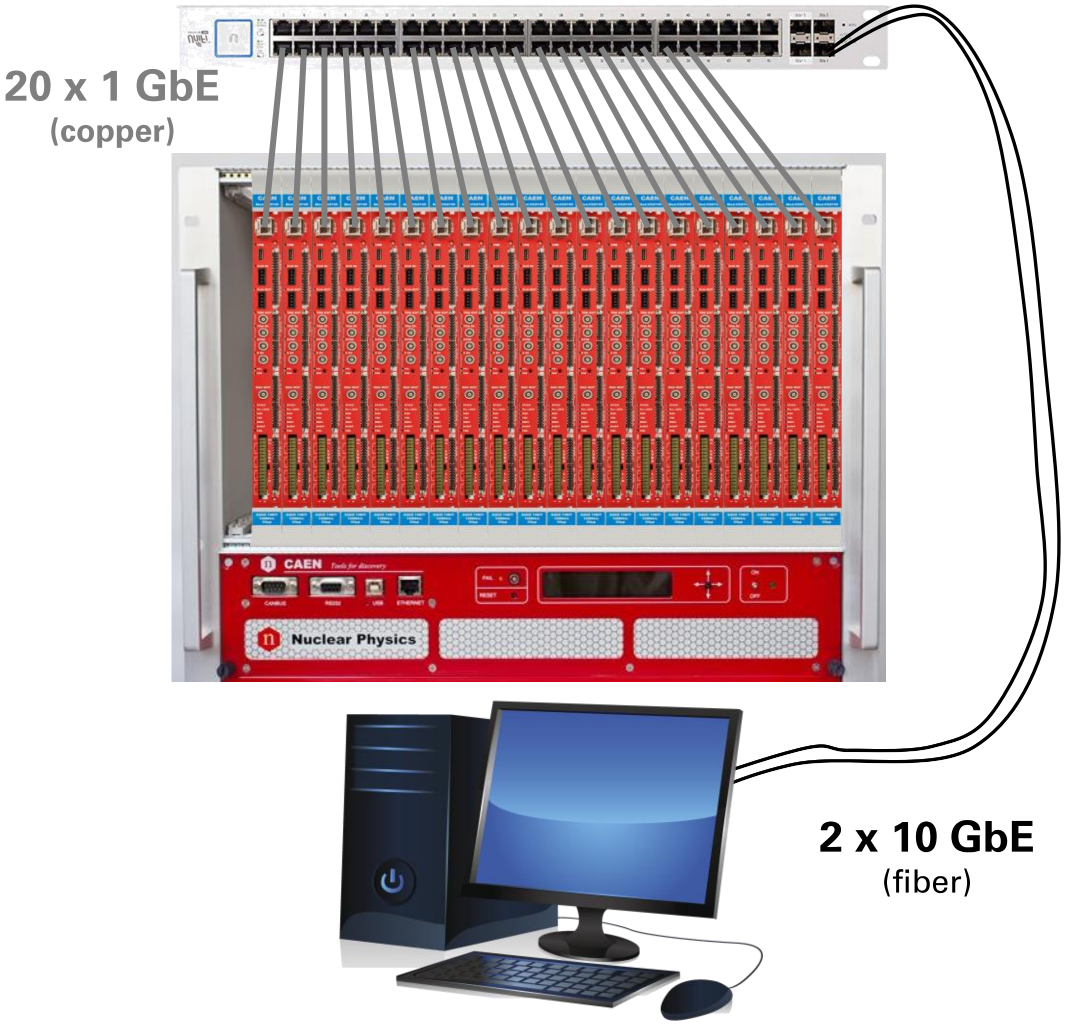
- *OakRidge*

Good fit for fast detector readout and PSD applications

Targeted for:

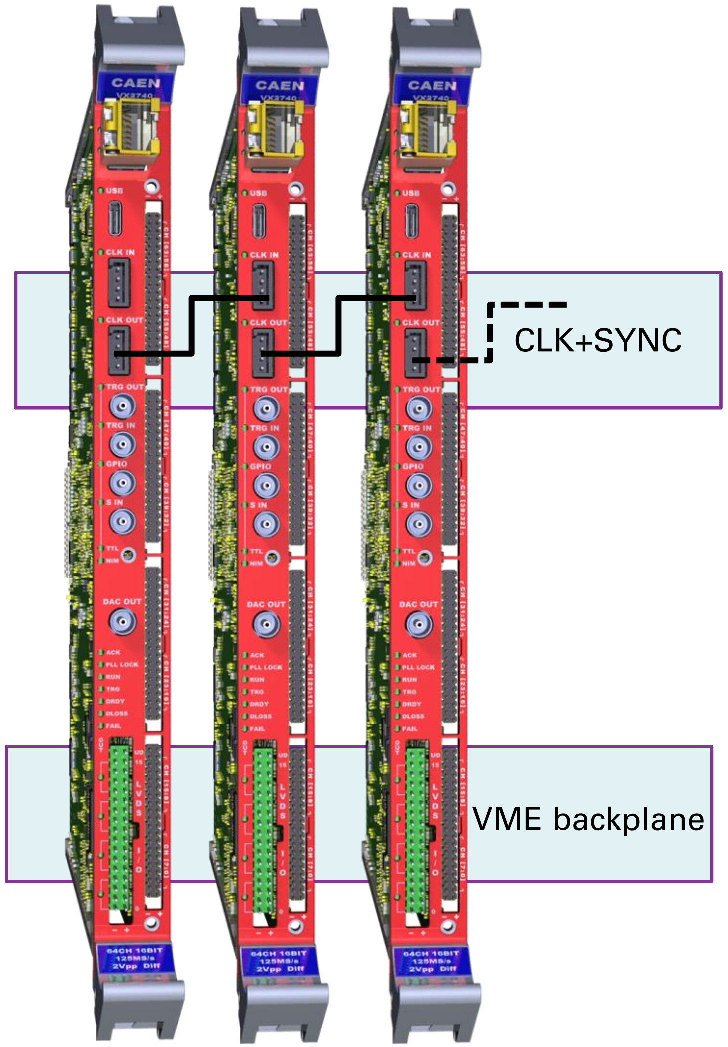
- *Plasma Diagnostic*
- *Nuclear Fusion*
- *Dark Matter*

Multiboard Readout – 10 GbE example



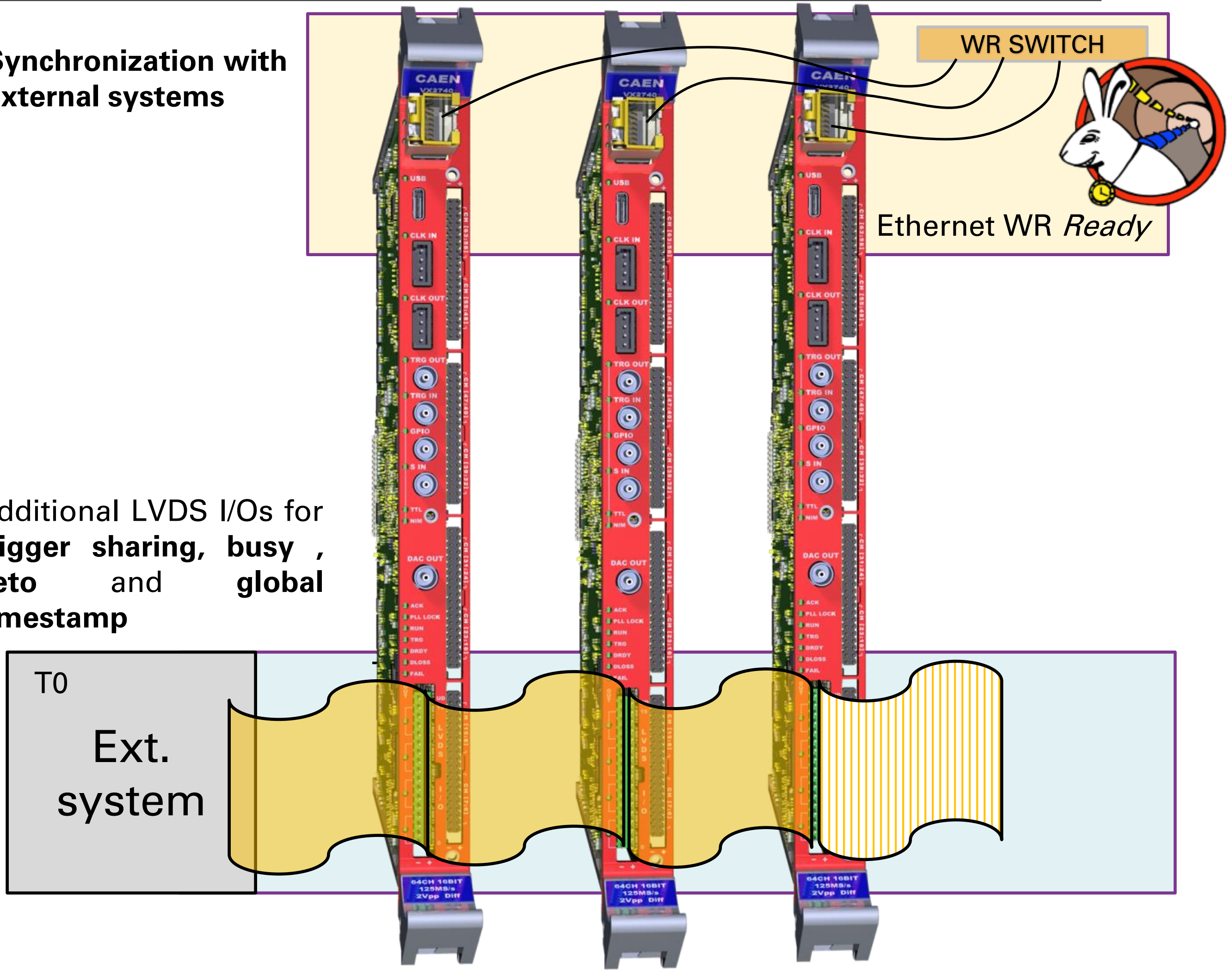
- TCP/IP allows PCIe readout with COTS board
- 1 GbE Tested up to ~**100 MB/s**
- 10 GbE Tested up to ~**300 MB/s → *Optimization***
- Fibers avoid noise pick up and signal loss on big distances

Digitizers Synchronization



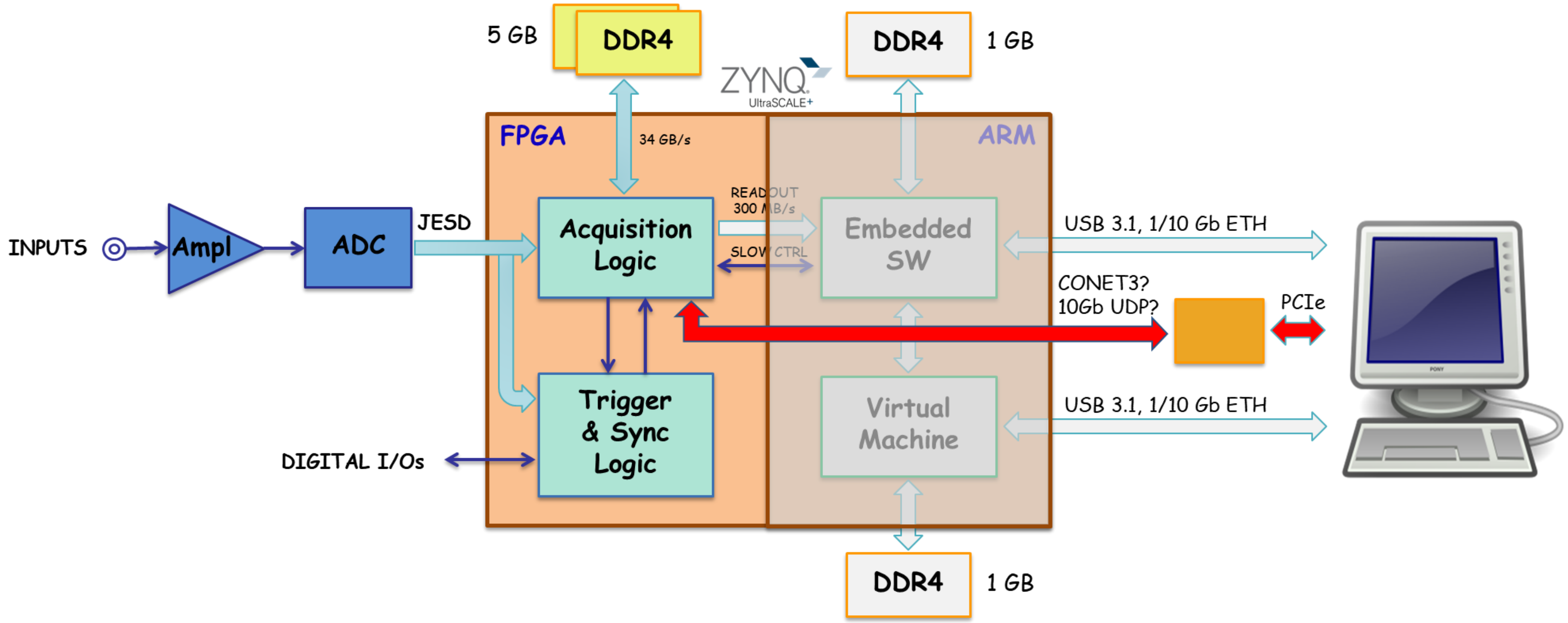
Synchronization with external systems

Additional LVDS I/Os for **trigger sharing, busy , veto** and **global timestamp**



Something else is needed?

Deterministic latency protocol→ Better for high-level/software trigger lines



COMING SOON 10 GbE UDP → unlike TCP, no issues with latency and bandwidth near the physical limit ~ 800 MB/s

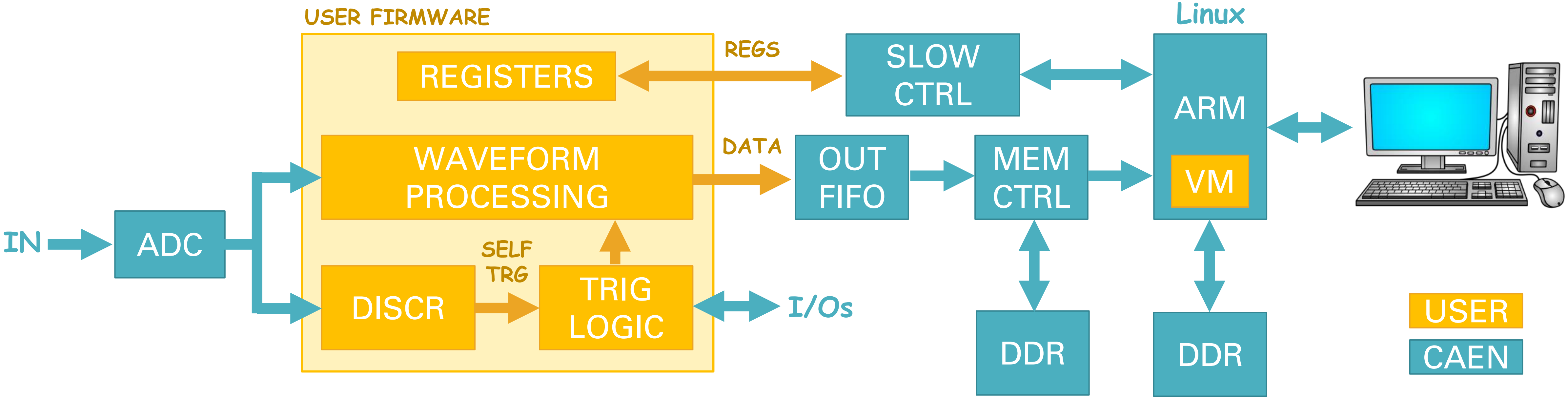
Open FPGA

We provide infrastructure: ADC data flow, data buffering and transfer, slow control

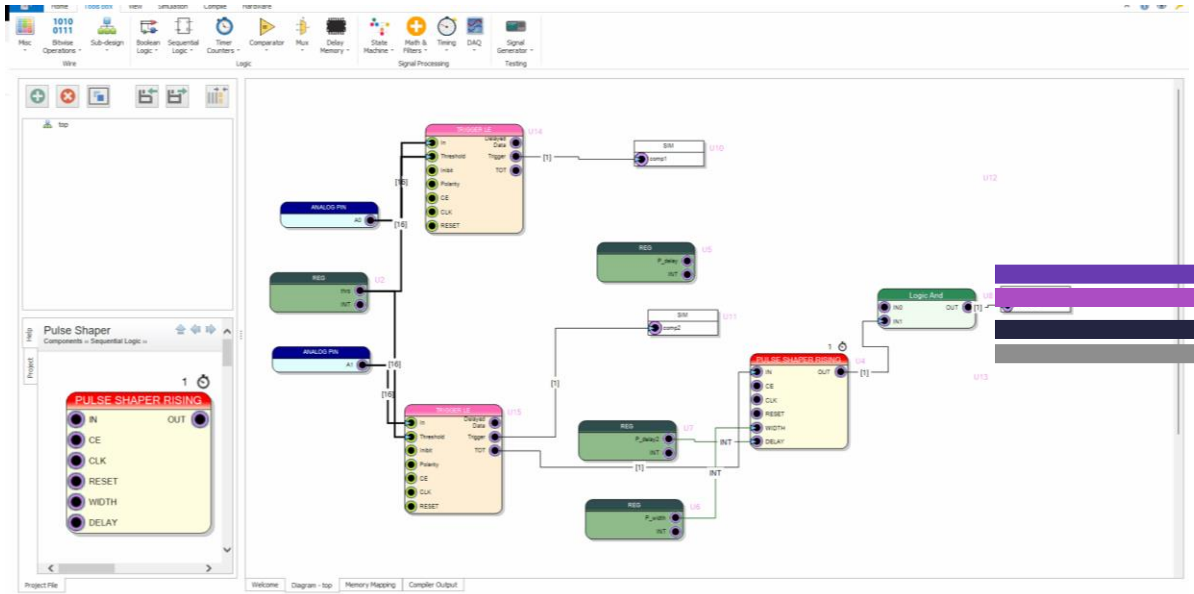
You implement your algorithms for data processing, parameter extraction and trigger logic

Sci-Compiler: graphical FPGA programming tool with precompiled modules (logic, filters, ...)

side option FDK: FW development kit with VHDL templates, simulation models, signal inspection, etc.



Sci-Compiler for FPGA programming



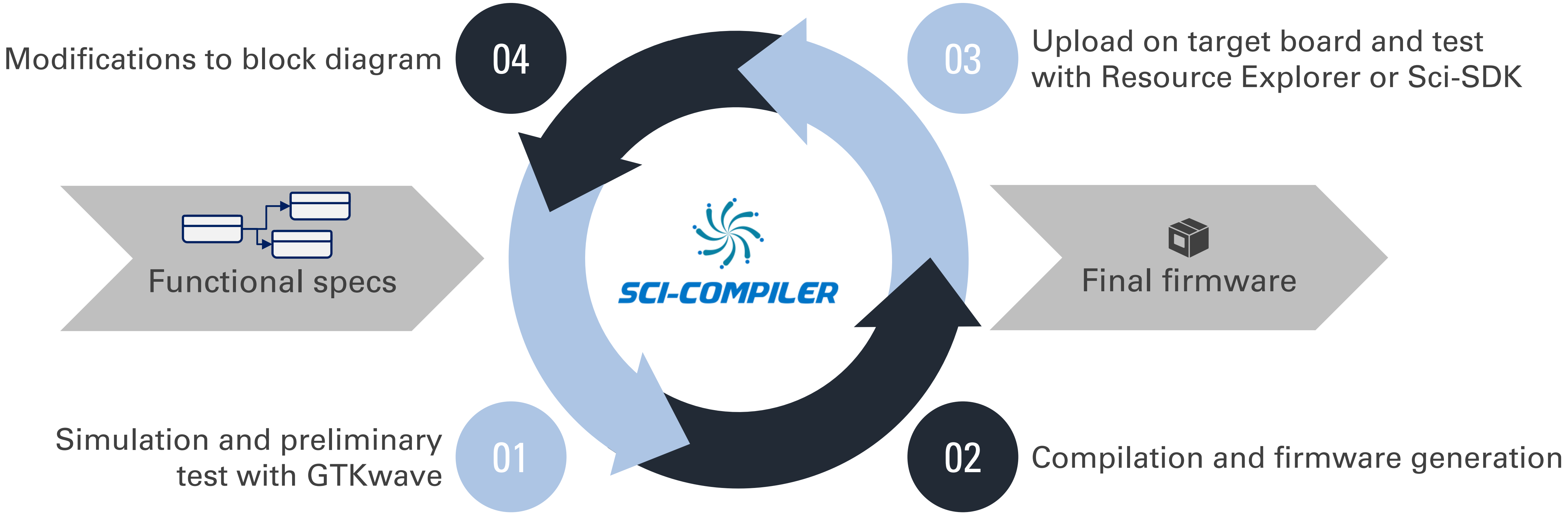
Block diagram — Define the functionalities of the firmware

Function blocks — Build the diagram relying on a wide library of blocks for physics and nuclear engineering

Firmware — Automatic generation of VHDL and bitstream. No coding expertise required

Testing — Easy-to-use embedded tools for debugging

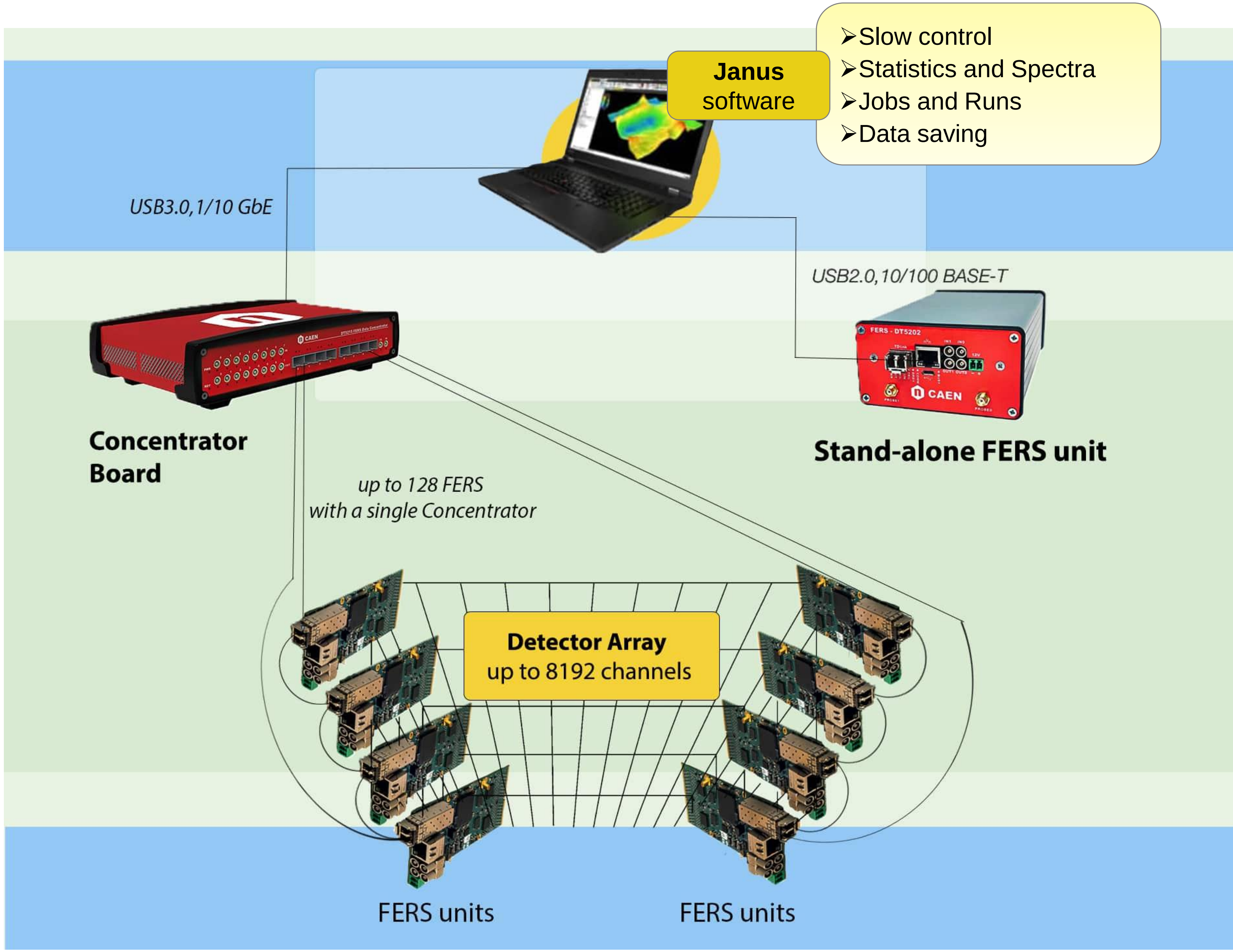
Design flow



Modifications to block diagram
04
03
Upload on target board and test with Resource Explorer or Sci-SDK
Functional specs
SCI-COMPILER
Final firmware
Simulation and preliminary test with GTKwave
01
02
Compilation and firmware generation

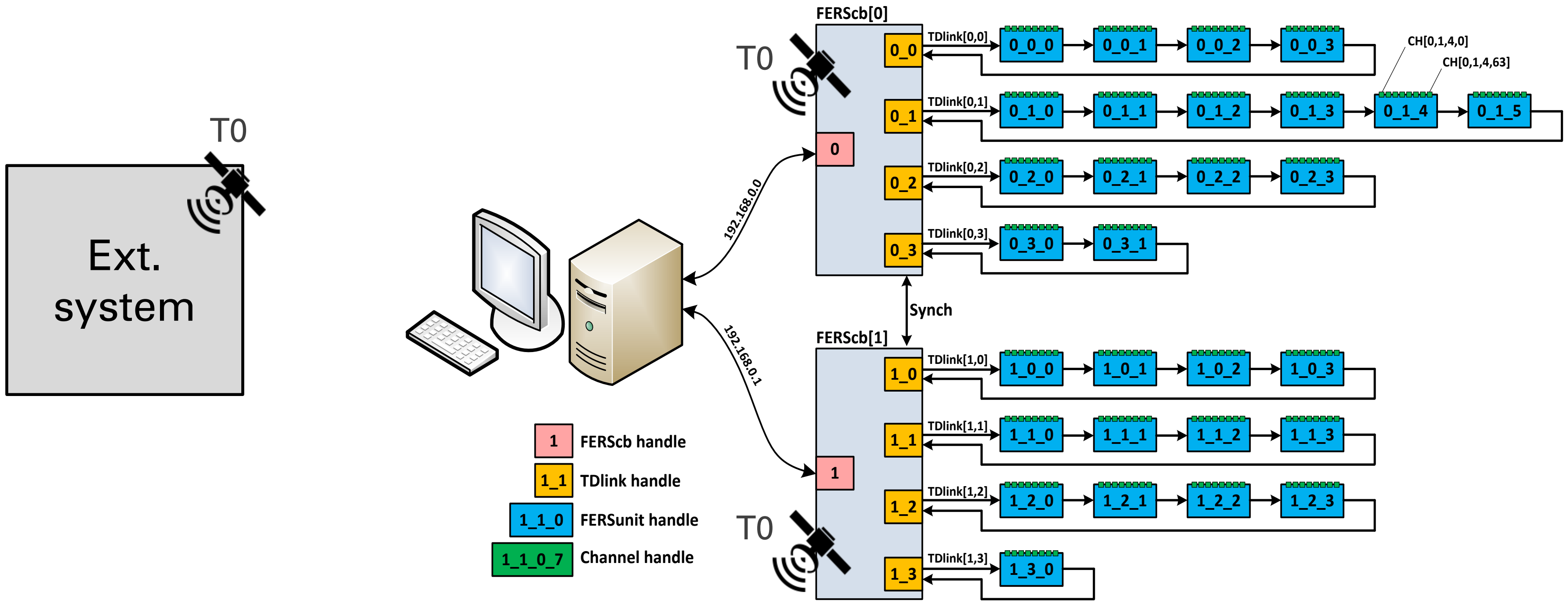
FERS-5200

- **Modular and Distributed** readout of large arrays of detectors
- **Compact** FERS units based on *ASICs* → front-end + digital
- **Concentrator Board** to manage multiple FERS units
- **TDlink**: 3.125 Gb/s Optical link providing Readout, Slow Control, Synchronization → **Easy-scalability**
- **Janus** software to control the whole system and make standard DAQ



TD Link for scalability

- **Proprietary protocol TDlink**: 3.125 Gb/s **over fiber** providing *Readout*, *Slow Control*, *Sync* and *Clock* at once
- Sync among FERS units at ~**20 ps** precision
- Allows **alignment of the timestamps with external systems** too – for example GPS, external clocks ,…



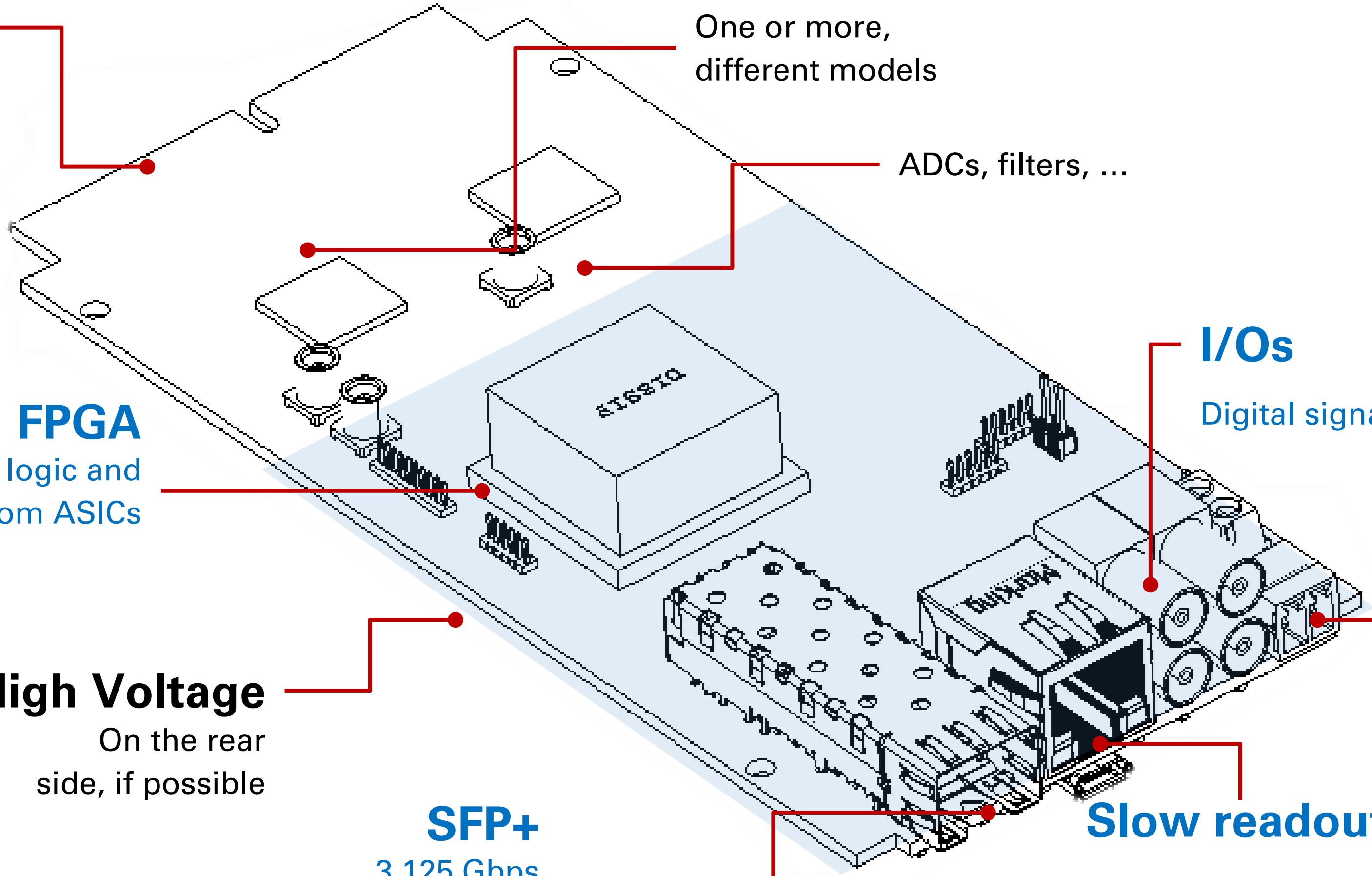
FERS unit

APPLICATION SPECIFIC

Input
64/128 ch. on fine pitch edge connector

ASICs
One or more, different models

ADCs, filters, …



FPGA
Triggering logic and data taking from ASICs

I/Os
Digital signals on LEMO

COMMON INFRASTRUCTURE

High Voltage
On the rear side, if possible

+12V

SFP+
3.125 Gbps
TDlink protocol

Slow readout
USB 2.0 and 10/100 Mb/s

FERS flavours

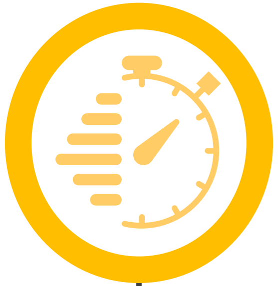
- *SiPM γ – spectroscopy*
- *Muon tomography*
- *SiPM-based calorimetry*
- *Cosmic-rays veto*
- *Medical imaging*

Weeroc Citiroc

A5202

SiPM

3 ps TDC



A5203

CERN picoTDC

- ToF-PET
- Typ. res. 20 ps RMS with walk correction

Weeroc Radioroc + CERN picoTDC

A5204

COMING SOON

SiPM high-res.

GEMs, Si strip

and other low gain detectors

COMING SOON

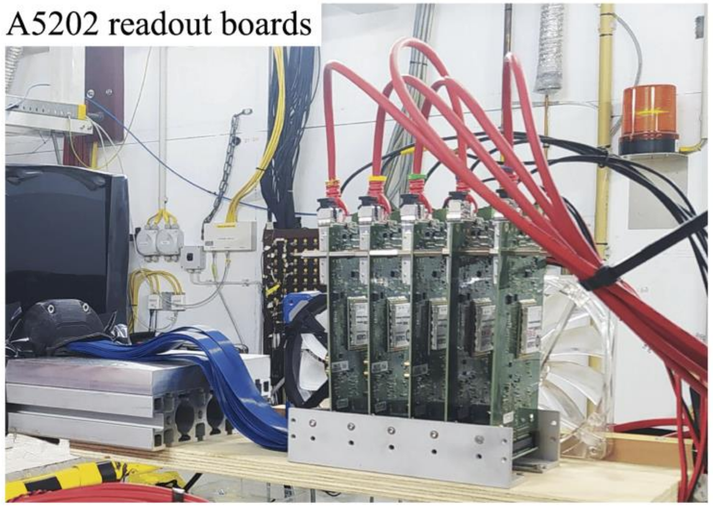
A5205

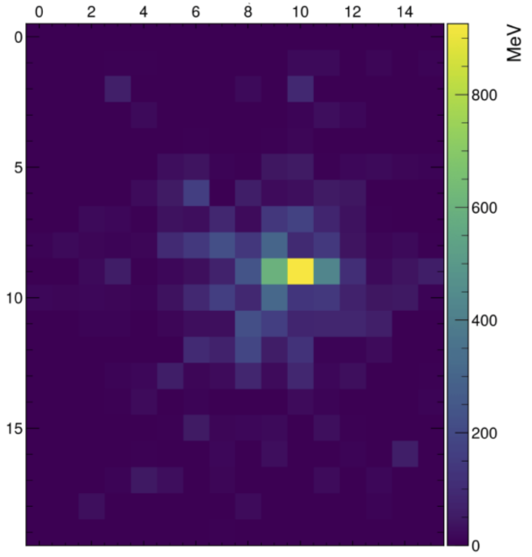
Weeroc Psiroc + CERN picoTDC

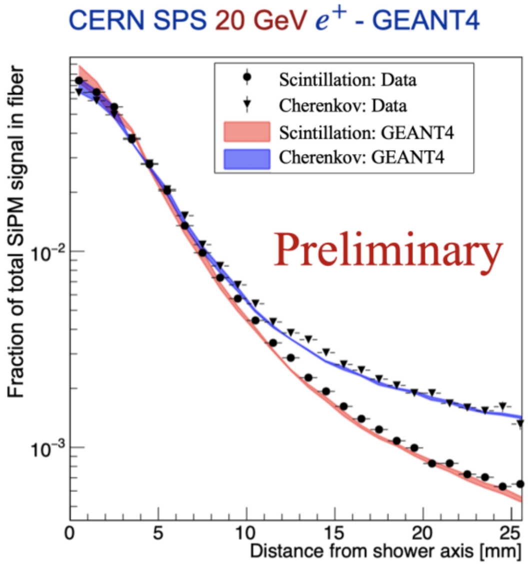
- *Candidate for ESS*

IDEA – dual calorimetry

320 SiPM calibration. Excellent results in the linearity of the calorimeter response and EM shower reconstruction



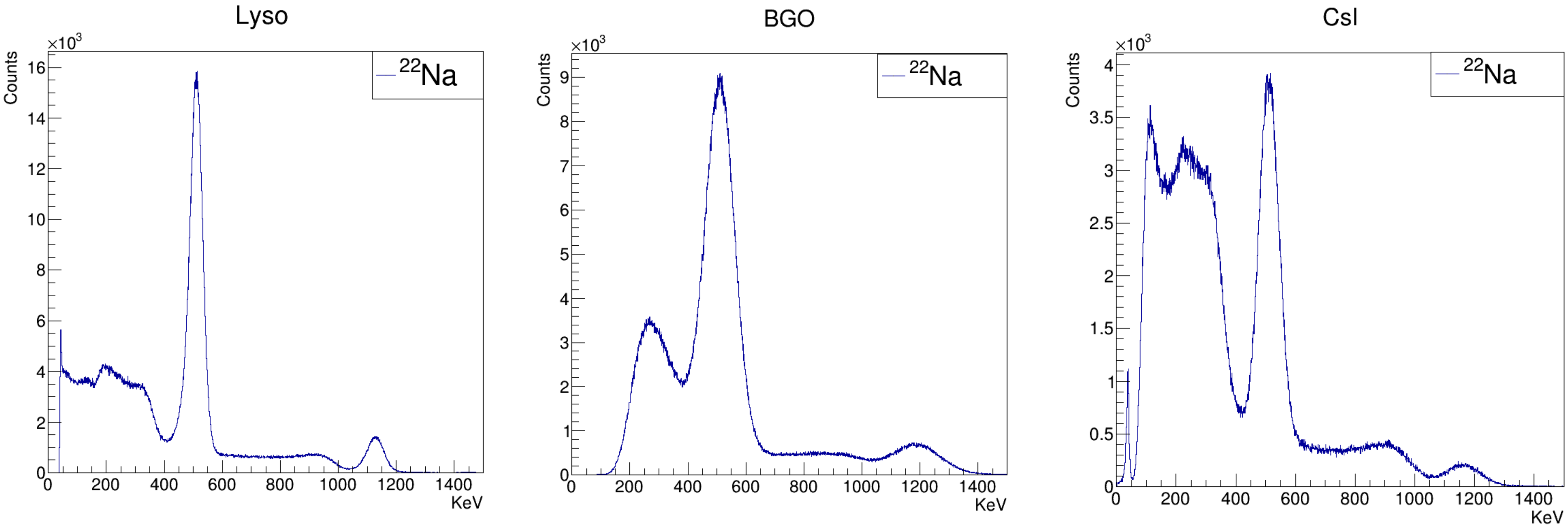




FERS units ca be synchronized with LEMO I/Os daisy chain (no concentrator board) with a precision of few ns

SiPMs for Dual-Readout Calorimetry
R. Santoro *on behalf of the IDEA Dual Readout Group*
Instruments **2022**, *6(4)*, 59;
https://doi.org/10.3390/instruments6040059

Gamma spectroscopy



Short shaping time (less than 100 ns) are not affecting much energy resolution even in the CsI case

Amplitude Measurements with SiPM and ASIC (Citiroc 1A) Front-End Electronics
M.Perri *et al*.
Nuclear Inst. and Methods in Physics Research, A
https://ieeexplore.ieee.org/document/10092191

Ideas for the future: high sampling rate SCA

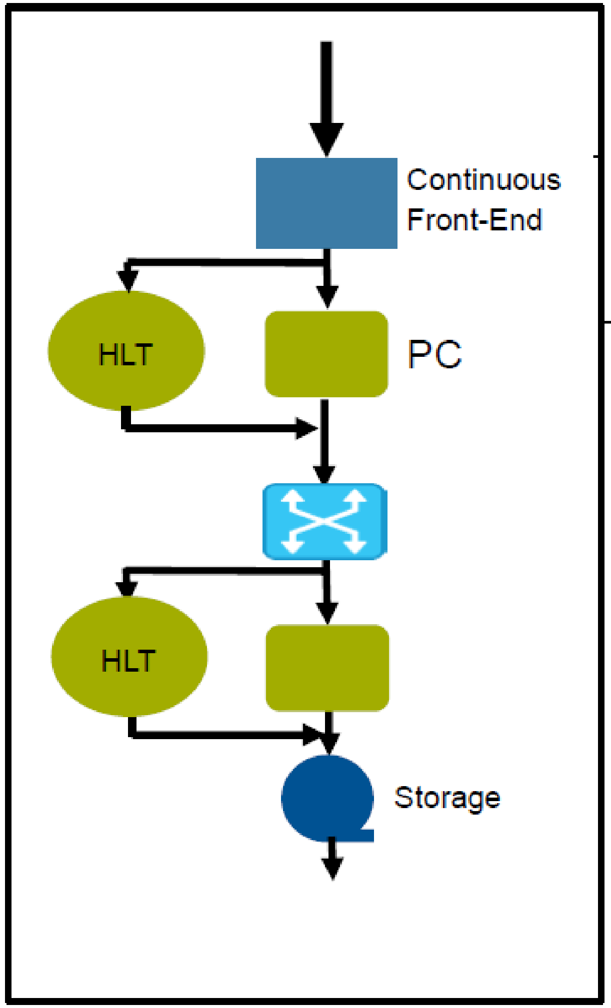
NALU SCIENTIFIC

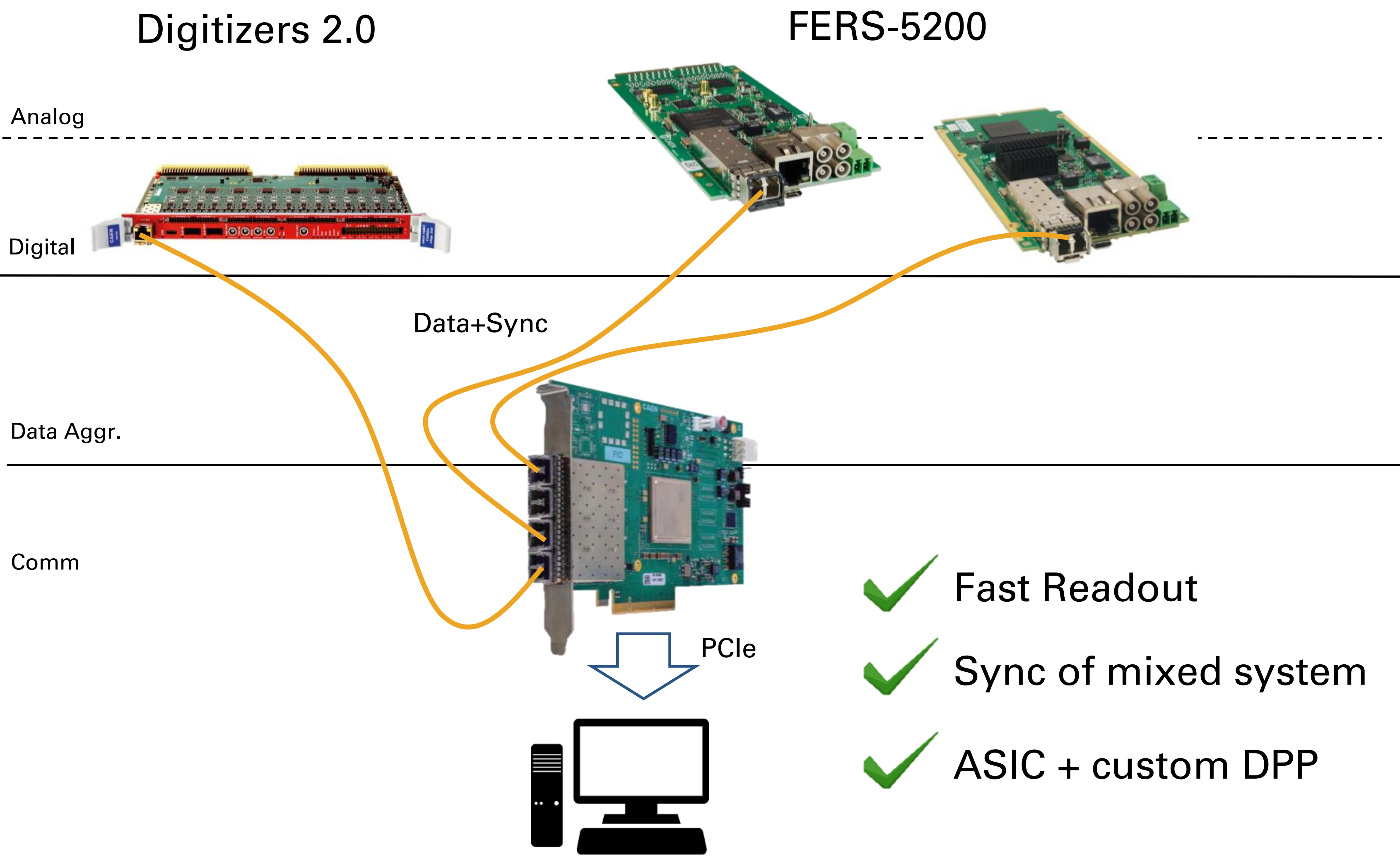
FEATURES	ASOC V3 [1]	AARDVARC V3 [1]	AODS V1 [1]	HDSOC V1 [2]
SAMPLE BUFFER	16 k	32 k	16 k	2k
CHANNEL	4 CHANNEL	4-8 CHANNEL	1-4 CHANNEL	32/64 CHANNEL
BANDWIDTH	0.8 GHZ ANALOG	2 GHZ ANALOG	0.5 GHZ ANALOG	1 GHZ ANALOG
TIMING RESOLUTION	35 ps	4-8 ps	<100 ps	<100 ps
SAMPLE RATE	2.4-3.6 GSa/s	10-14 GSa/s	1-2 GSa/s	1-2 GSa/s
APPLICATIONS	General purpose time of flight measurements	Accurate timing measurements	High dynamic range Sparse detectors	High density (SiPM) readout
FEATURES	Low cost	High performance High timing resolution	Variable gain stages Flexible serial interface	Internally configurable triggering schemes

Readout?

PSD

The future?





- Fast Readout
- Sync of mixed system
- ASIC + custom DPP

Summary

- Solutions with **high channel count** and **plenty of resources** are now available
- Digitizers 2.0 with **Open FPGA** are the forefront technology for waveforms acquisition with **high data throughput** and custom Digital Pulse Processing
- FERS-5200 offers **frontend + digital** accompanied by **compactness** and **easy-scalability**
- Exploration of new technologies and protocols to meet the evolving needs of readout systems.
- Future is more and more integration between FERS and Digitizers in terms of functionality (SCA chips) and readout protocols (data+sync)

Thank you for your attention

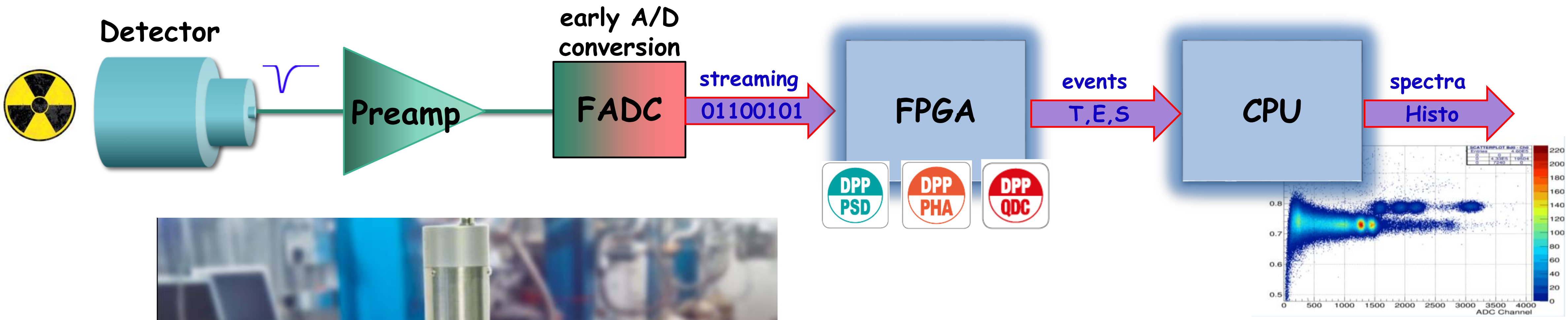
Any question/curiosity?

Backup slides

Modular Electronics readout systems – 1970s

- ✔ No programming skills required
- ✘ Limited functionalities
- ✘ Difficult Debug
- ✘ Cost
- ✘ Size
- ✘ Power

All-in-one Digital Readout – 2000s

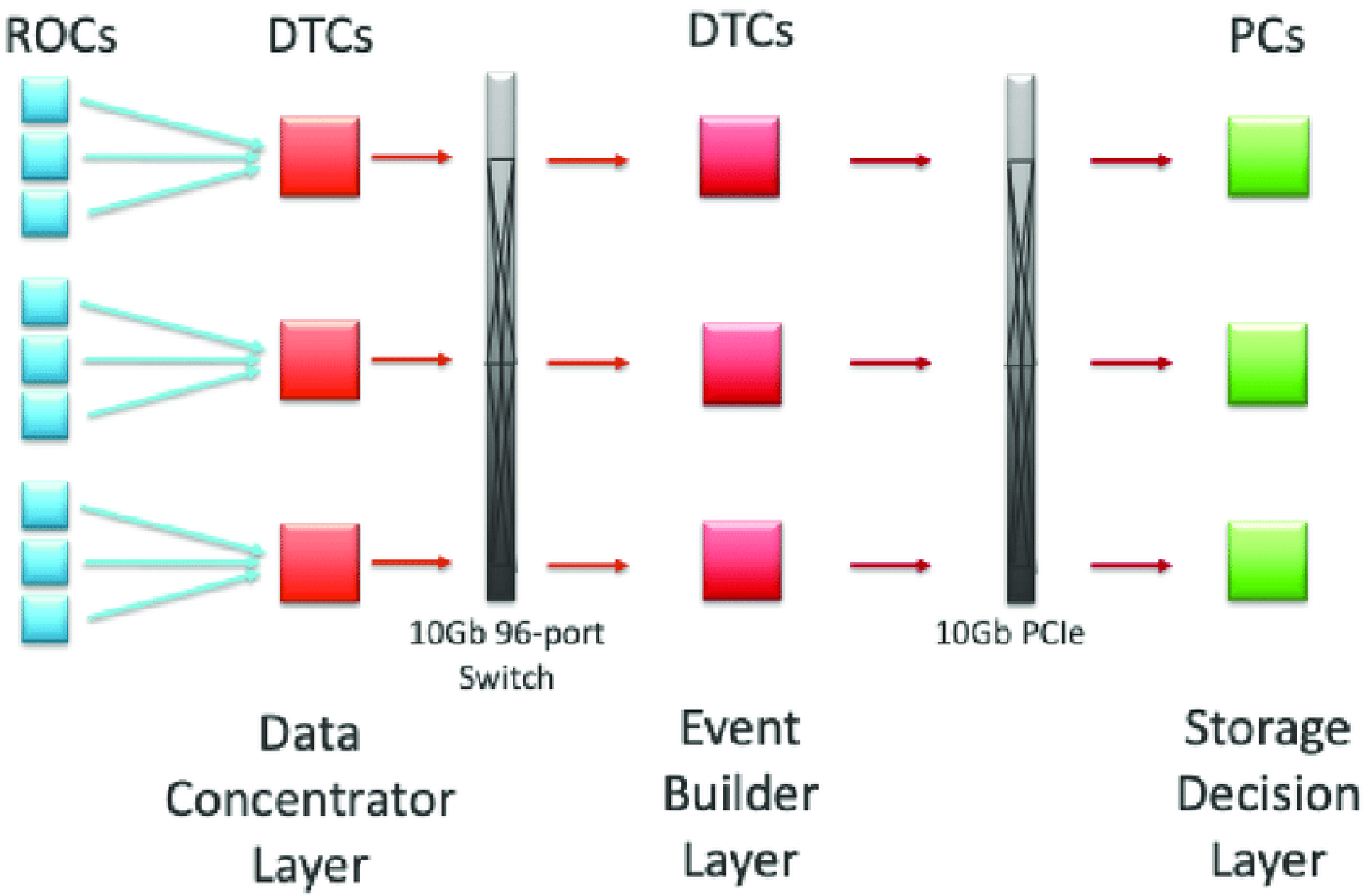


- All-in-one hardware with Pulse Processing
- Tstamp, Energy, PSD, Counts, Waveforms
- Remote configuration and readout
- Minimal analog conditioning

Challenges of new experiments

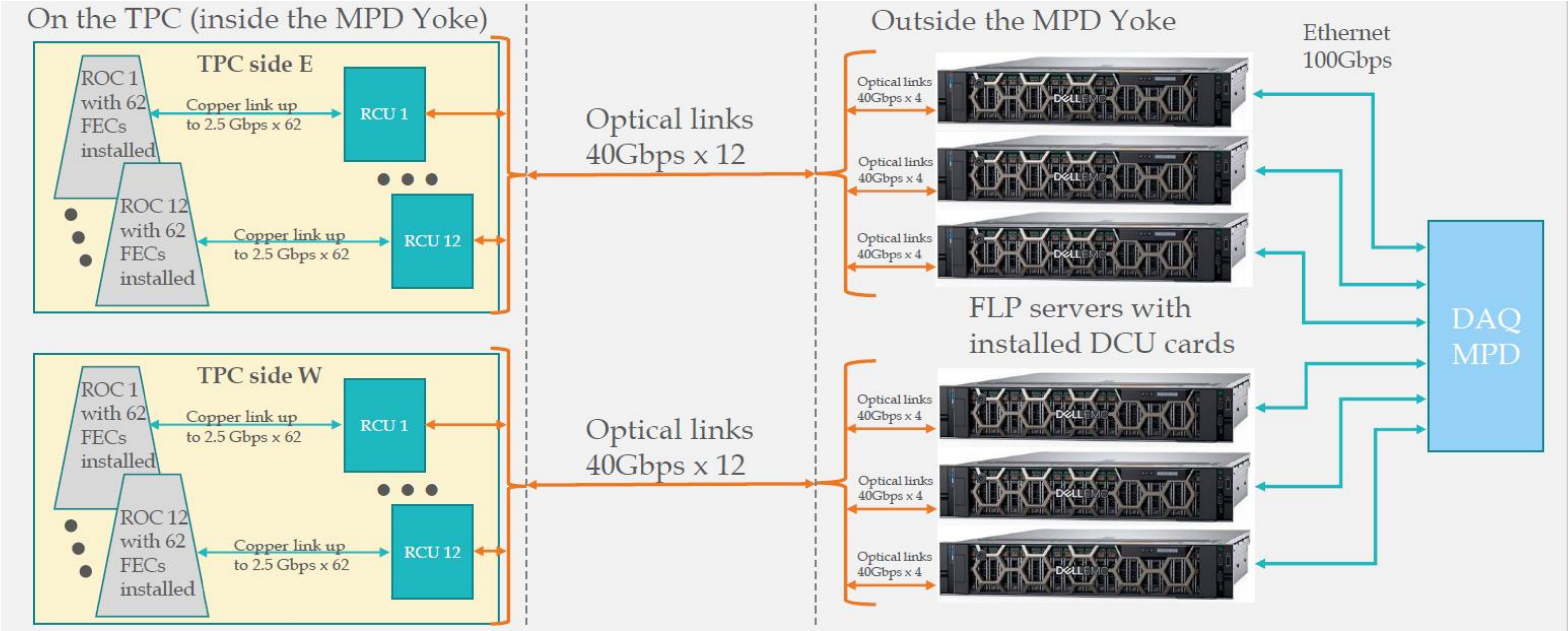
- **Miniaturization** of detectors and scale down in cost → demand for more compact systems
- **Low power ASIC** available → **denser** systems are now affordable ~ **10.000 ch.**
- New technology → **Triggerless DAQ** → **High data throughput**
- Storage, middleware running onboard, complex online analysis
- Online **customizable** data processing
- **Event building** on board (not on PC/server) avoiding lines congestion

Example : Mu2e data readout



A.Gioiosa et al., EPJ Web of Conferences 262, 01011 (2022)

Example 2 : TPC/MPD detector for NICA



S. Vereschagin, JINR, ICPPA 2022

2740/2745 Digitizers

<u>**64 channel, 125 MS/s, 16 bit waveform digitizer**</u>

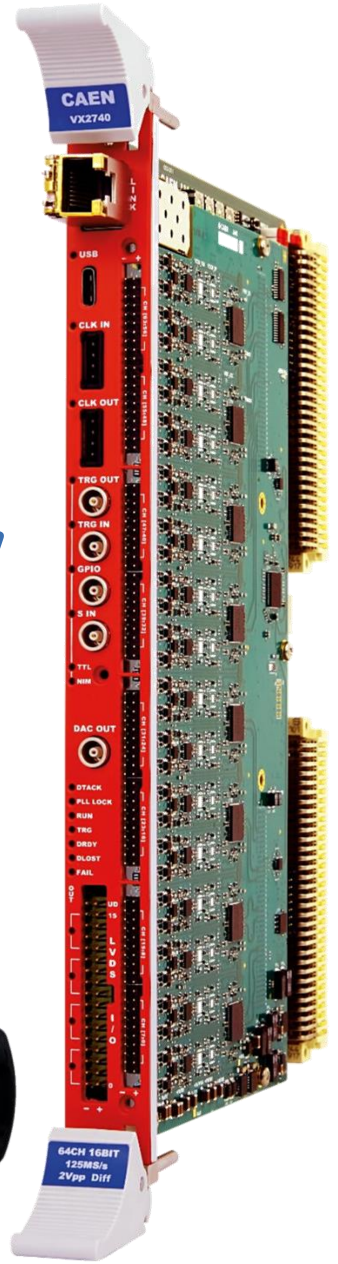
- Single Ended of Differential inputs (2 mm header connectors)
- **Dynamic Range**:
  - V2740 → 2 Vpp fixed
  - V2745 → 40 mV ÷ 4 Vpp (Gain from 0 to 40 dB in steps of 0.5 dB)
- Individual DC offset adjust over the full dynamic range
- Multiple **readout** interfaces: 1/10 GbE, USB 3.1, Optical Link
- **Open FPGA** to provide flexibility in the pulse processing algorithm
- **DPP** functionalities: PHA, QDC, PSD, CFD, Zero Suppression
- Embedded Linux **ARM**
- Form factors: VME64X, VME64 and Desktop

Good fit for:

- *neutrino and dark matter experiments*
- *high channel density spectroscopy with Silicon and HPGe detectors*

Currently used by:

- *Numen (SSD, SiC, LaBr$_3$)*
- *Dark Side (Argon TPC)*
- *Tristan (multi pixel SDD)*
- *… and others…*

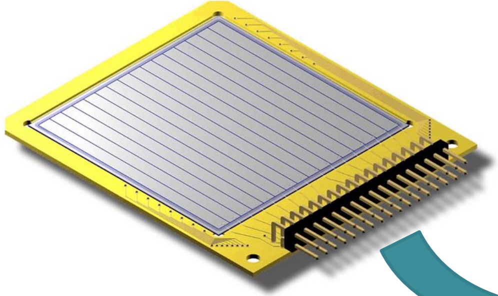


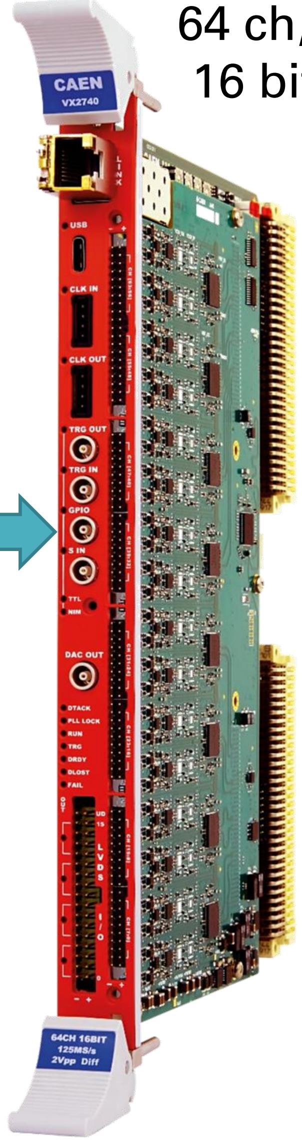
SSD readout @ Numen (LNS)

A1429
64 ch Charge Sensitive Preamplifier

4 Vpp differential signals
2.54 mm Ribbon Cable

VX2745
64 ch, 125 MS/s
16 bit Digitizer





DPP PHA

List Mode Streaming Readout

ERCD
MicroCoaxial Cable

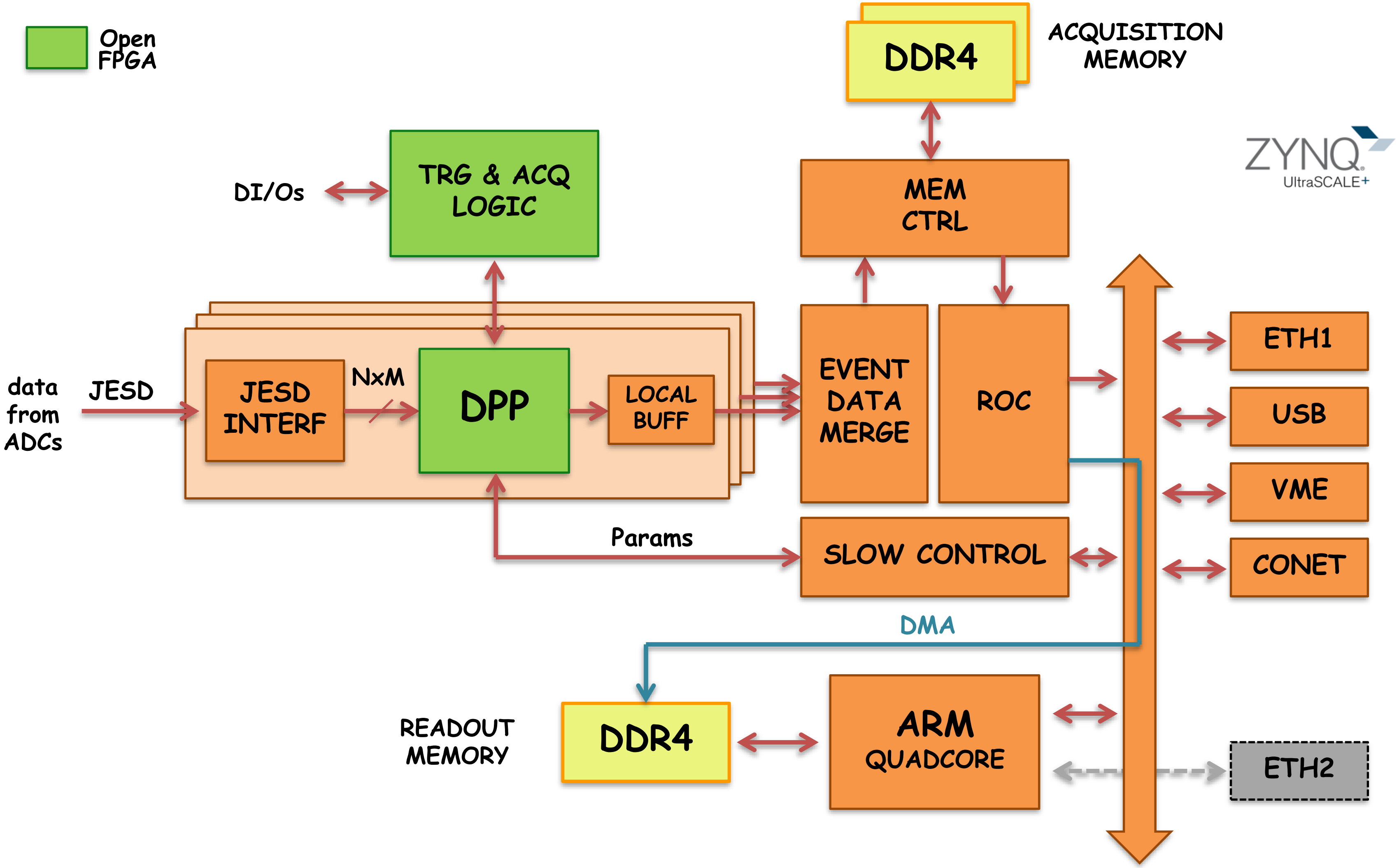
A372F
Cable Adapter

VX2730: the must-have for fast detectors

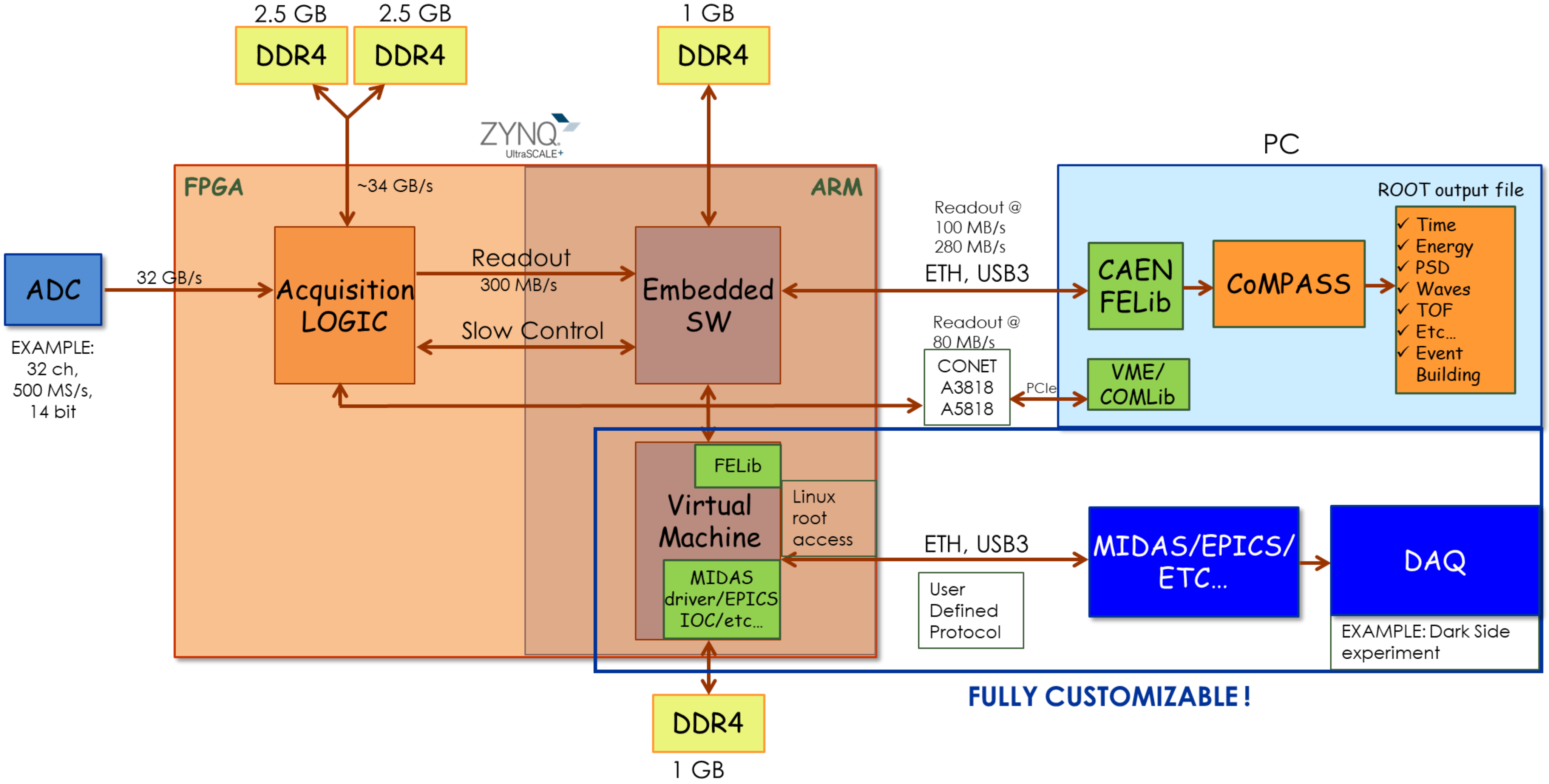
<u>**32 Channel 14 bit 500 MS/s Digitizer with programmable Input Gain**</u>

- 32 single-ended analog inputs on MCX connectors
- 4Vpp input range with software selectable analog gain
- **Open FPGA** programming through the graphical tool SCI-Compiler
- Wide range of applications (from Nuclear and Particle Physics to High Timing Resolution, Fast Neutron Spectroscopy, and Homeland Security)
- Suited for signals from liquid or inorganic scintillators coupled to PMTs or SiPMs, or Silicon and HPGe detectors.
- **1 GbE, 10 GbE, USB 3.0** and CONET 2.0 (optional) connectivity
- Common Trigger (waveforms) or Individual Self-trigger modes
- DPP options: PHA, QDC, PSD, CFD
- Advanced Waveform Readout modes: ZLE, DAW
- Fully supported by CoMPASS and WaveDump2 readout software
- SDK for embedded Linux processor and host PC

Digitizers 2.0 - FPGA Block Diagram

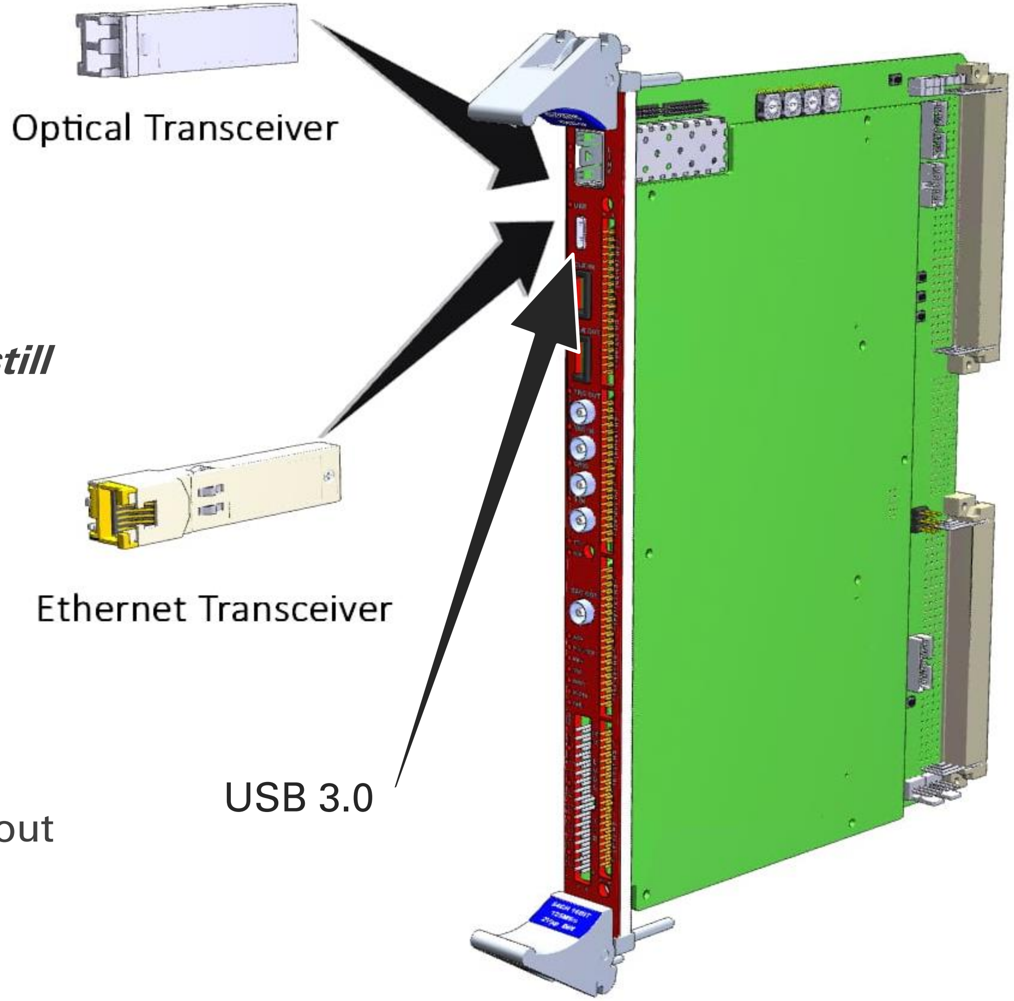


Examples of Applications



Readout interfaces

- **Ethernet**
  - Front Panel SFP+ with RJ-45 (copper) or LC (fiber)
  - TCP-IP stack implemented in embedded ARM (PS).
  - **1 GbE:** tested up to **100 MB/s**
  - **10 GbE**: fiber only. Tested up to ~**300 MB/s**. ***Optimization still ongoing***
- **USB 3.1**
  - Front Panel Type-C connector
  - Tested up to **300 MB/s**
- **VME**
  - Not implemented yet. Low priority. Pursuing bus-free readout systems!



Digitizer 2.0 - Communications

- **Ethernet**
  - Front Panel SFP+ with RJ-45 (copper) or LC connectors (fiber)
  - Ethernet port connected to Programmable Logic of the FPGA (PL)
  - TCP-IP stack implemented in embedded ARM (PS).
  - **1 GbE**: tested up to 100 MB/s (TCP-IP)
  - **10 GbE**: fiber only. Preliminary tests up to ~200 MB/s. Optimization still on going
- **USB 3.1**
  - Front Panel Type-C connector
  - Tested up to 300 MB/s
- **CONET (Daisy Chainable Optical Link)**
  - CAEN proprietary protocol
  - Current version (CONET 2.0): 1 Gb/s => ~90 MB/s, up to 8 boards in daisy chain
  - A5818 PCIe collector board (up to 4 links = 32 digitizers)
  - USB 3.1 to CONET adapter available (A4818)
  - Potential upgrades: 10 Gb/s, synchronization over CONET
- **VME**
  - Legacy of the old digitizers. Keep for retro compatibility.
  - VME64X compliant. MBLT64, 2eSST
  - Not implemented yet. Low priority. Pursuing bus-free readout systems!!!

Conet vs 10 GbE

10 GbE Advantages:

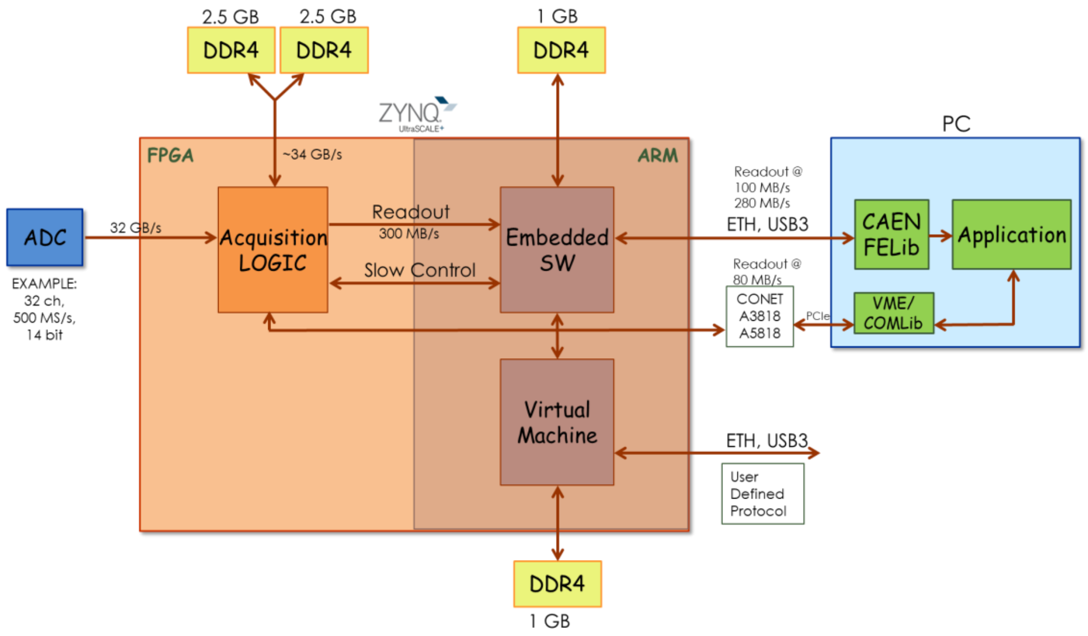
➢ CONET has no access to the Web Interface → USB connection required to update firmware – fine for experiments?

➢ Bandwidth 2-3 times bigger than CONET2

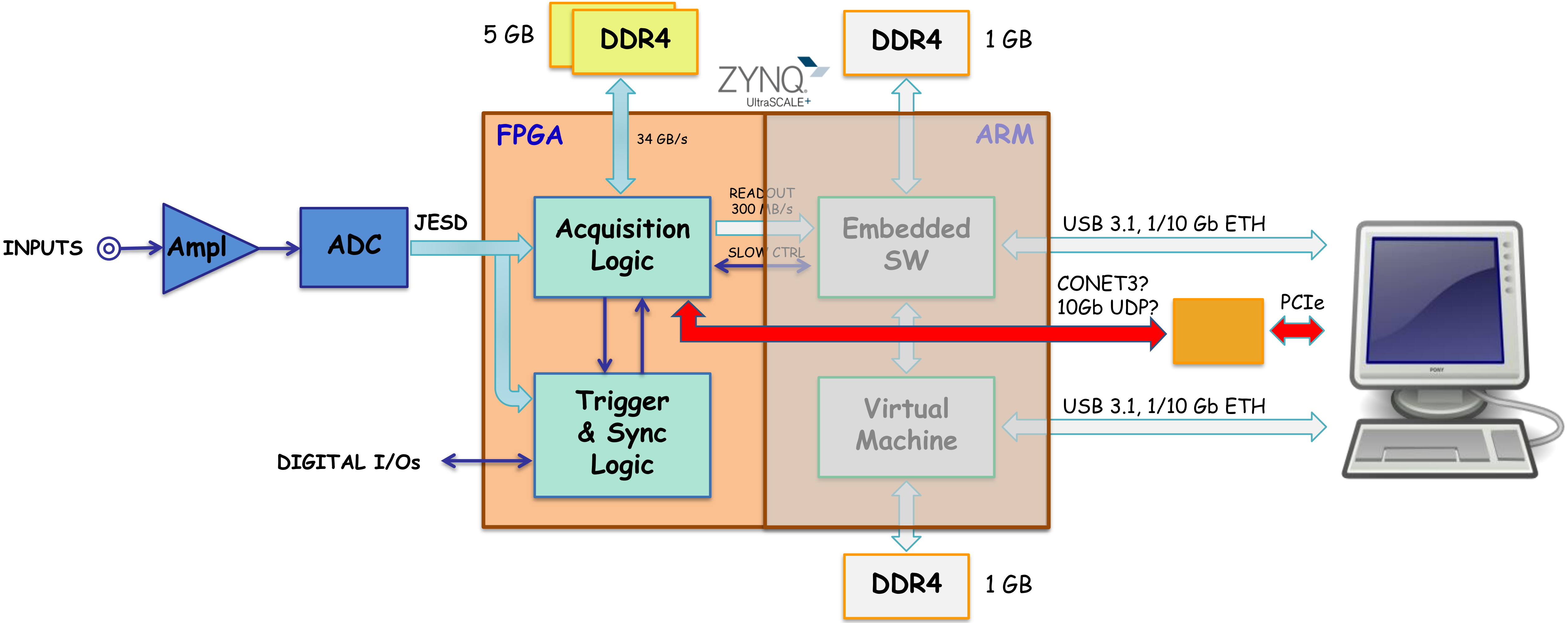
➢ Access to the embedded VM

CONET Advantages:

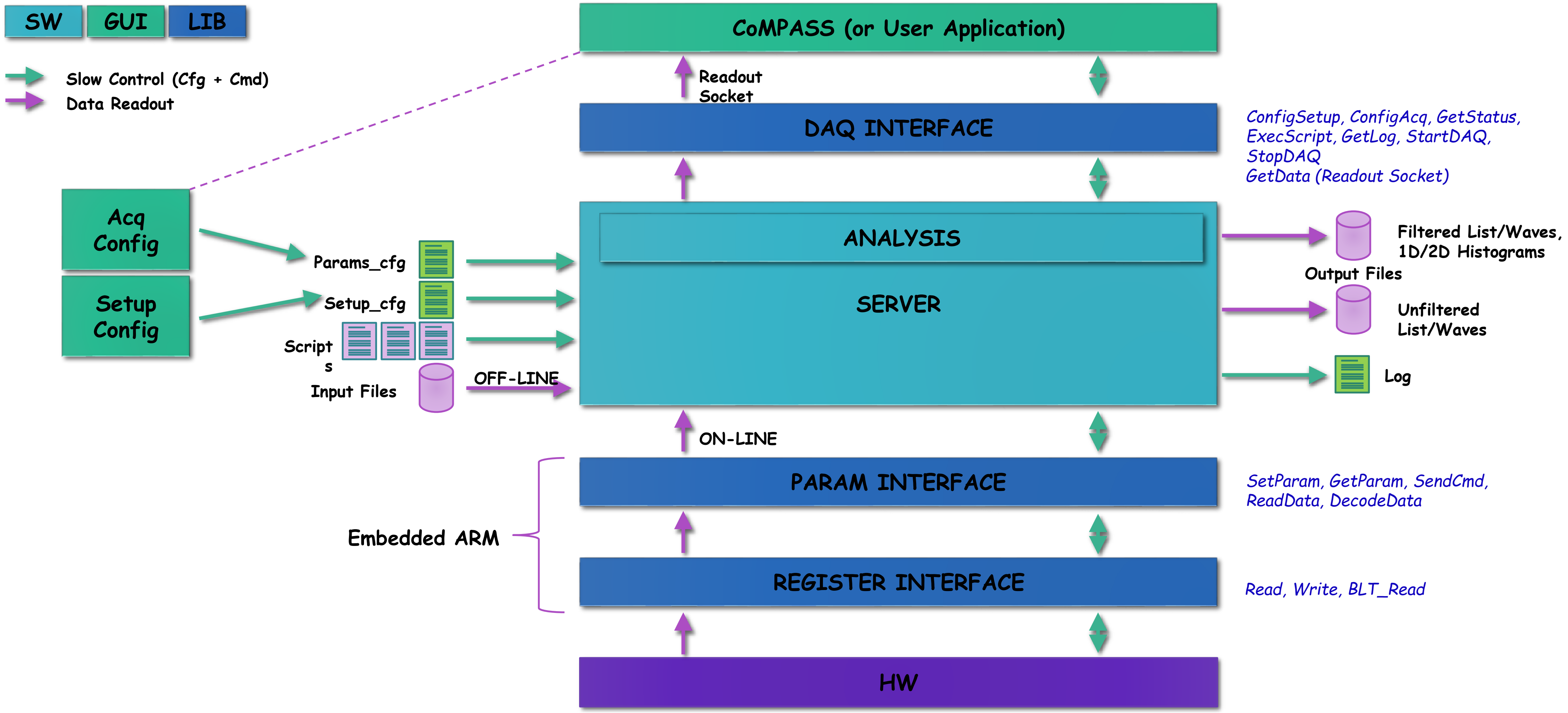
➢ CONET = deterministic latency → Better for high-level/software trigger lines



The Digitizer architecture



Digitizers 2.0 - Software Layers



WaveDump2

- C++ software for **CAEN Digitizer 2.0** running **FW Scope**
- User-friendly **GUI** for the board configuration and data acquisition
- **Multi-board management**
- Simultaneous plot of waveforms from up to 8 input channels
- **FFT** and **Samples Histogram** provided runtime
- **Data saving** (ASCII or binary format)
- Import/Export of configuration presets

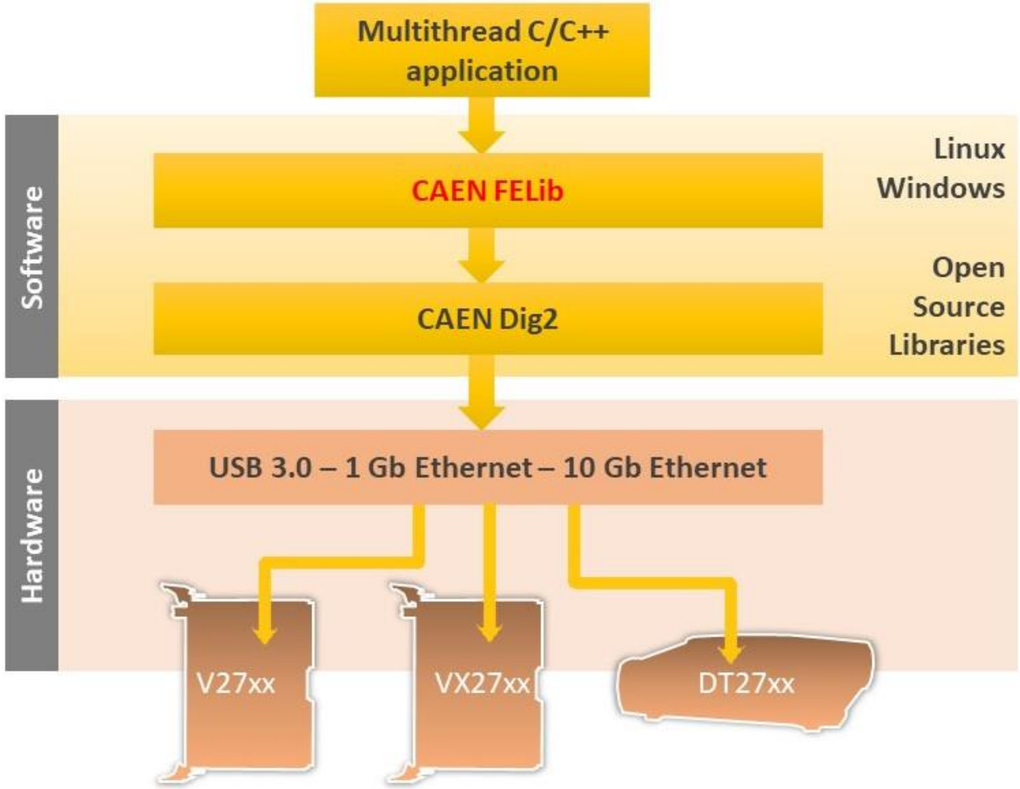
CoMPASS

- Support to all the **CAEN Digitizer** running **DPP FW**
- **Multi-board management**
- Simultaneous plot of waveform, energy, time, PSD, and TOF spectra
- ROI management and energy calibration
- Selectable filters on energy, PSD and Time Correlation
- Several options for **data saving**, including **ROOT**, **.csv**, **.bin**, **.n42.**

CAENFE Library – For custom software devel.

- Set of API for the control and use of the CAEN Digitizer 2.0
- Available for C and C++ environment
- Python wrapper available in the *pip* package system
- Extended support for mix CAEN system Digitizer 2.0 + Digitizer 1.0 available
- Open-source software (distributed under GNU Lesser General Public License 3+)

CAENFE Library – A New Approach



- Two layers: CAEN FELib and CAEN DIG2
- FELib provides API
- DIG2 implements the FELib API for the digitizer 2.0
- A new approach in the firmware access: parameters, an abstraction of the registers, easier to use and understand

Acquisition Modes

	62.5	100/125	250	500	1000	> 1000	Description
Scope	🟢	🟢	🟢	🟢	🟢	🟢	Oscilloscope mode, all channels triggered simultaneously
PHA	🔴	🟢	🟢	🟢	🔴	🔴	Spectroscopy with Charge Preamps and PMTs
PSD	🔴	🟢	🟢	🟢	🟢	🔴	Neutron/Gamma/Alpha discriminations with Scintillators
TDC	🔴	🟢	🟢	🟢	🟢	🔴	Digital CFD or LED, Resolution < 1 ns (<100 ps with 500/1000 MS/s)
QDC	🟢	🟢	🟢	🟢	🟢	🔴	Self-gated charge integrator
ZLE/DAW	🔴	🟢	🟢	🟢	🔴	🔴	Waveform fragments (zero suppression, adaptive acquisition window)
Open FPGA	🔴	🟢	🟡	🟡	🔴	🔴	User defined Algorithms and Output Data Content

🟢 Ready   🟡 Coming soon   🔴 Not Available

Digitizer options

#ch \ MS/s	62.5	100/125	250	500	1000	up to 5000
<8		DT	DT		DT	
8		V	V / DT	DT	V	DT[1]
16			V	V		V[1] / DT[1]
32	DT		coming...	coming...		V[1]
64	V	V / DT / R				
128		DT / R				

(1) SCA models => Max wave length = 1024 pts, Trg dead time = ~100 μs

V = VME

DT = Desktop

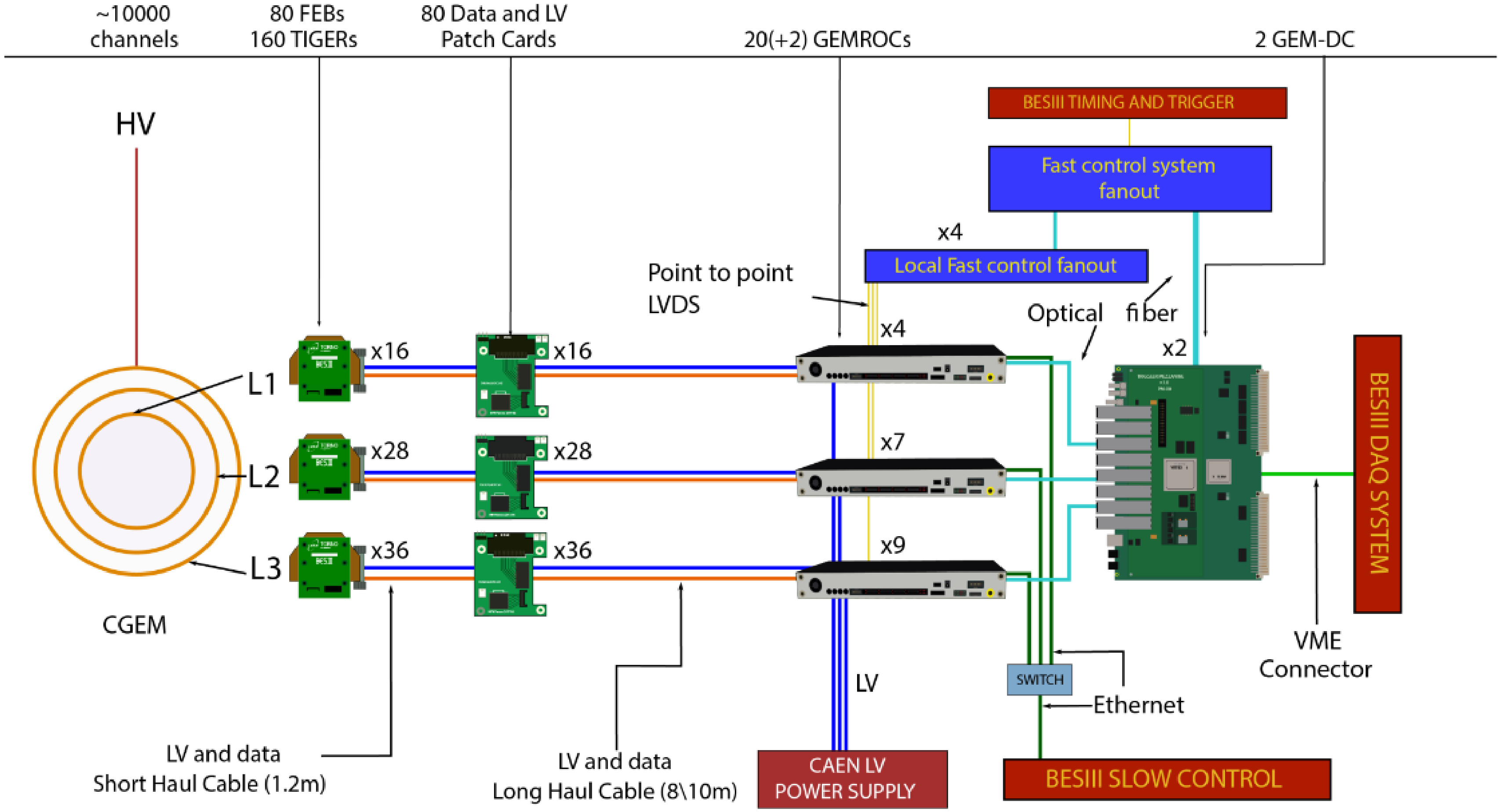
R = Rackable

Digitizer 2.0 - Synchronization

- **Front Panel Sync Connector**
  - Two 4-pin AMP Modu-II connectors (input + output)
  - Brings Reference Clock (typ. 62.5 MHz) + Sync (T0) signals
  - Daisy Chain (1st digitizer = master) or Star distribution from external fan-out
  - On board, high performance PLL for ADC clock synthesis and phase adjust
  - Sync signal defines Acquisition Start-Stop and/or the zero of the time stamp
- **Backplane Synchronization**
  - Reference Clock and Sync signals routed to J0 connector
  - Requires additional backplane (plugged on back side of P0 connectors on VME64X backplane)
  - Signals from a master digitizer (self-synching) or external source via P0
- **Synchronization from readout link (future upgrades)**
  - Clock recovery from the Front Panel link (optical or copper)
  - Potential support for White Rabbit
  - Potential evolution of CONET to a synch + readout link
- **Other I/Os**
  - 4 LEMO connectors: TrgIn, TrgOut, GPI, GPO (Typ. Start/Stop, Busy, Veto, etc…)
  - 16 LVDS In/Out: individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc…

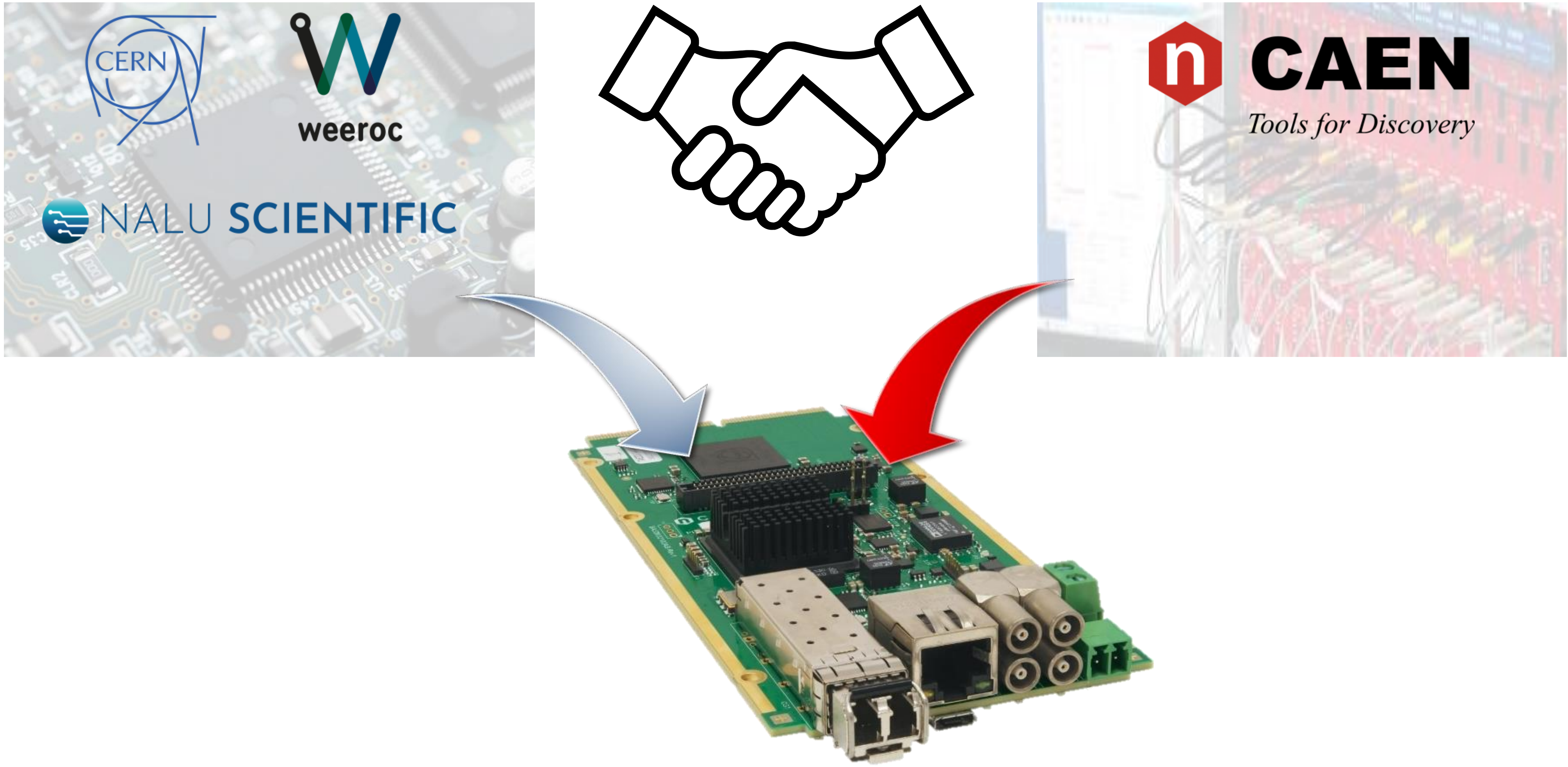
FERS-5200 use cases

Example 3: CGEM_IT readout chain



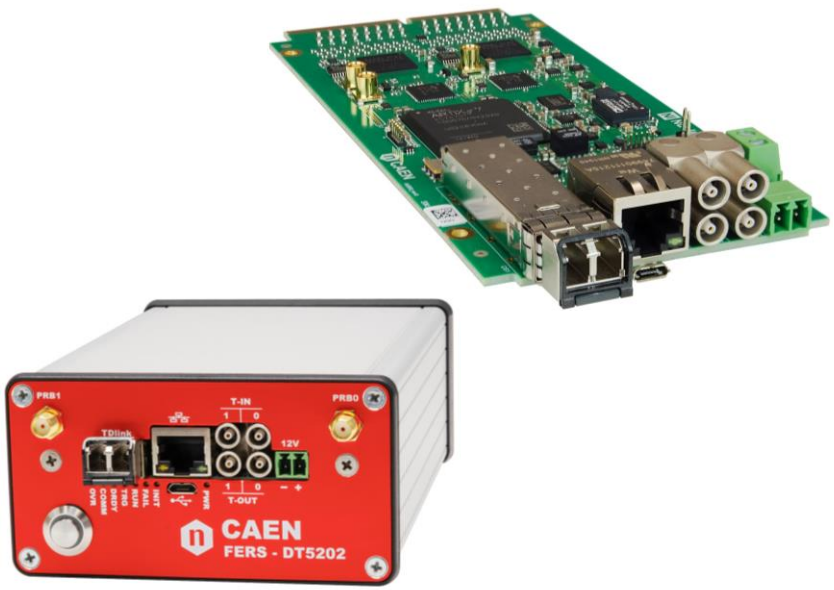
A. Amoroso et al., JINST 16 (2021) 08, P08065

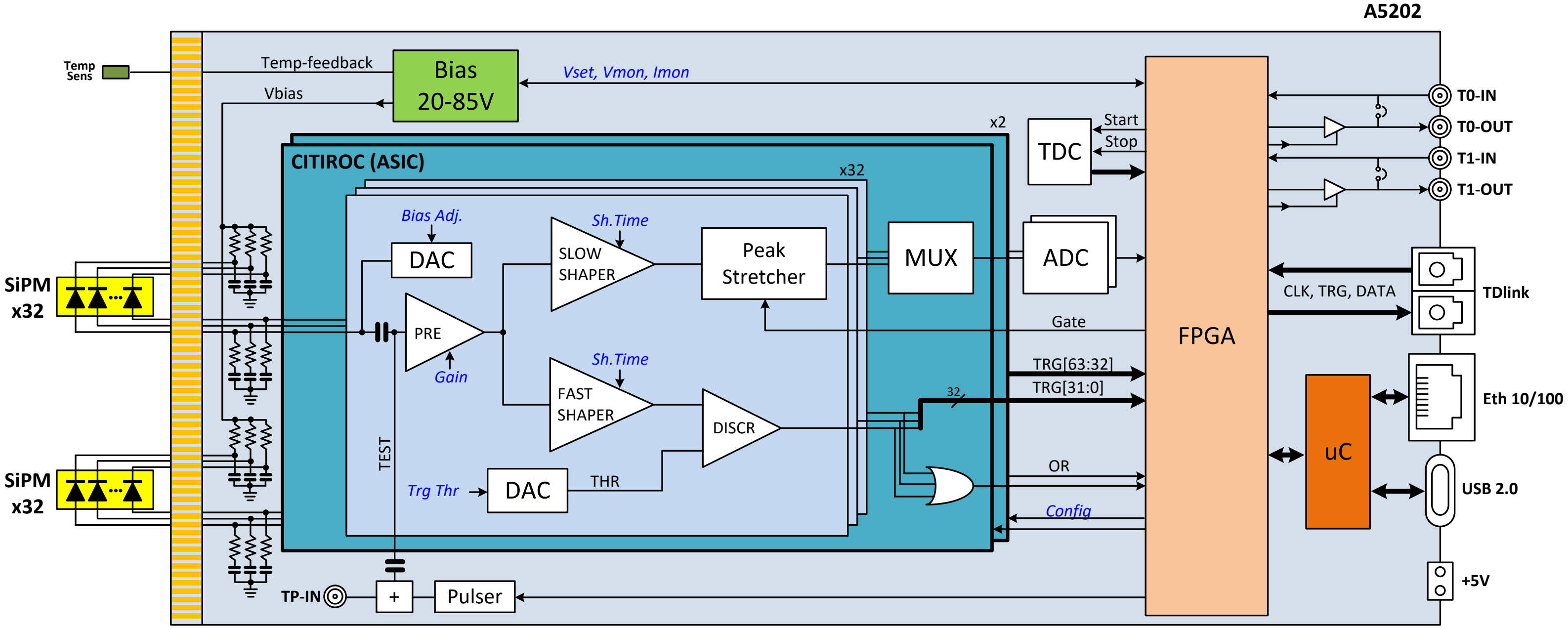
Synergies



A5202: 64 channel SiPM readout

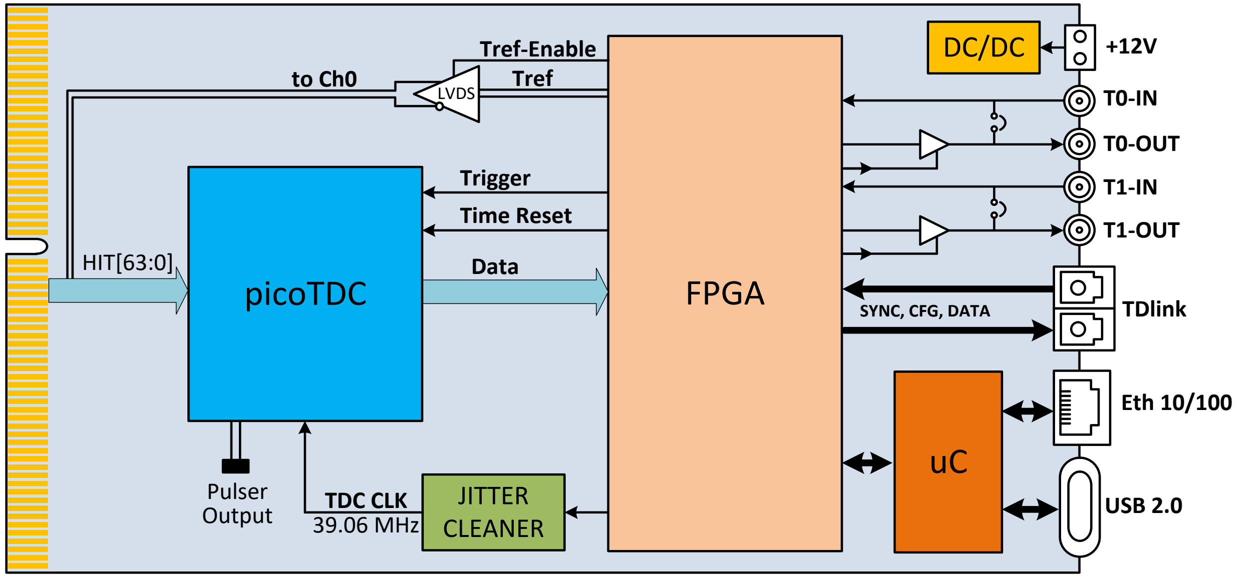
- 64-channels SiPM readout, based on analog chain + **Peak Sensing** strategy (Weeroc **Citiroc-1A**)
- Embedded 20-85 V module for SiPM **bias**
- **Single photoelectron** energy resolution and **500 ps** event timestamp resolution
- Readout modes: photon counting, spectroscopy (PHA), event timestamping





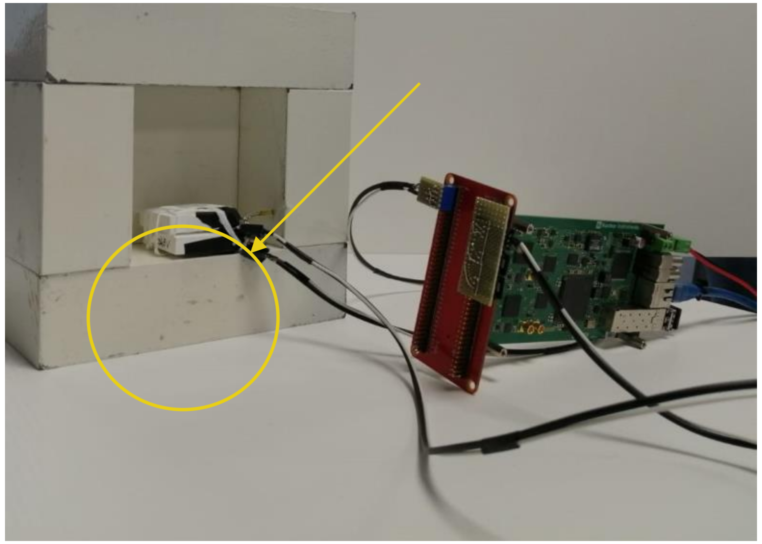
A5203: 64/128 channel 3 ps TDC

- 64/128-channels with timing resolution LSB = 3.125 ps, **RMS typ. 7 ps -** CERN **picoTDC** ASIC
- Input board (A5256) with fast discriminators (16+1 channels)
- Acq. modes: Common Start, Common Stop, Trigger Matching, Streaming (Leading, Trailing, ToT)
- Automatic **walk** correction

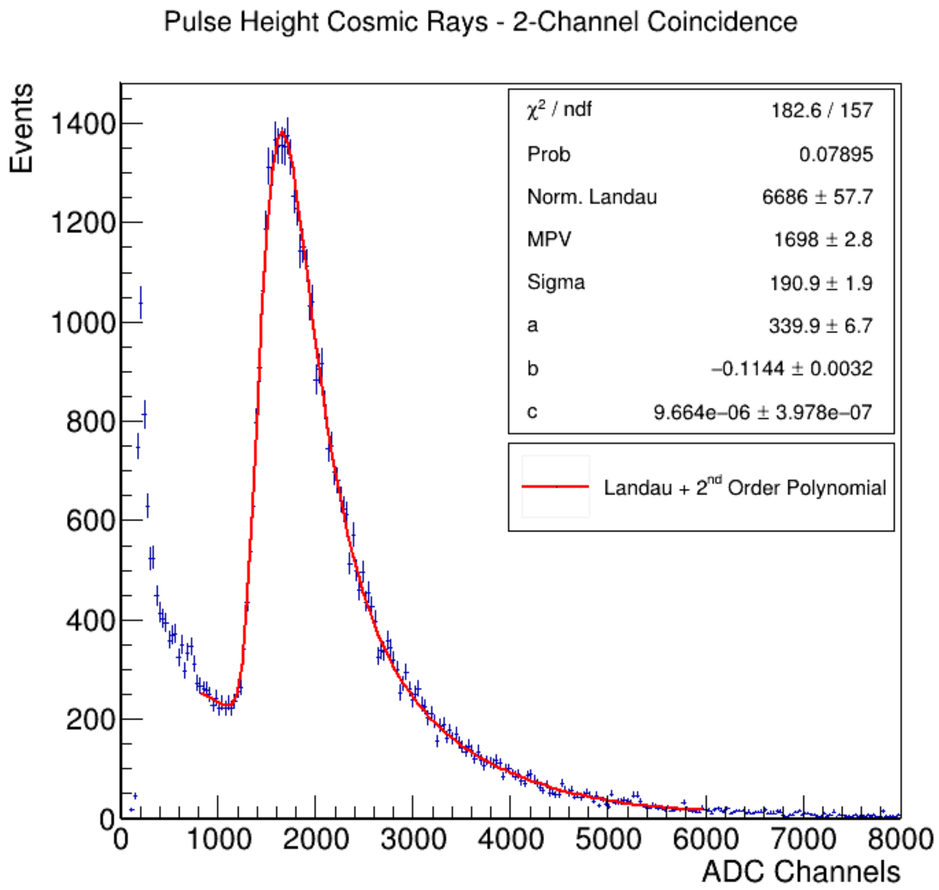


Measurement of Cosmic Ray Energy Loss

- ➢Two 4.8 cm x 4.8 cm x 1 cm plastic scintillators, each one coupled to a Hamamatsu S13360-6050CS SiPM



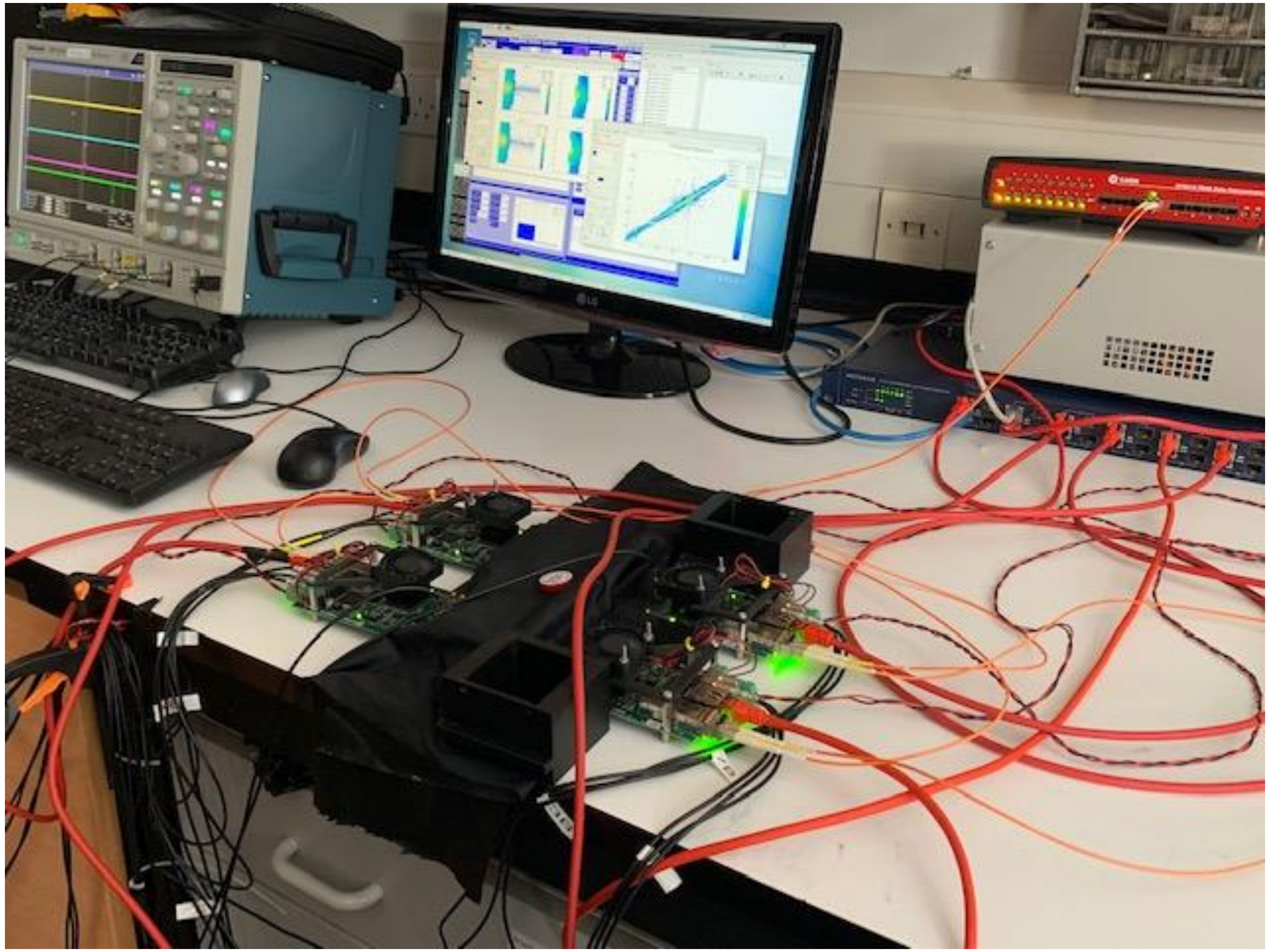
- ➢Two channel coincidence (implemented at firmware level) used as trigger for PHA acquisition



Landau from relativistic muons loss of energy clearly visible

Muon tomography - nuclear waste

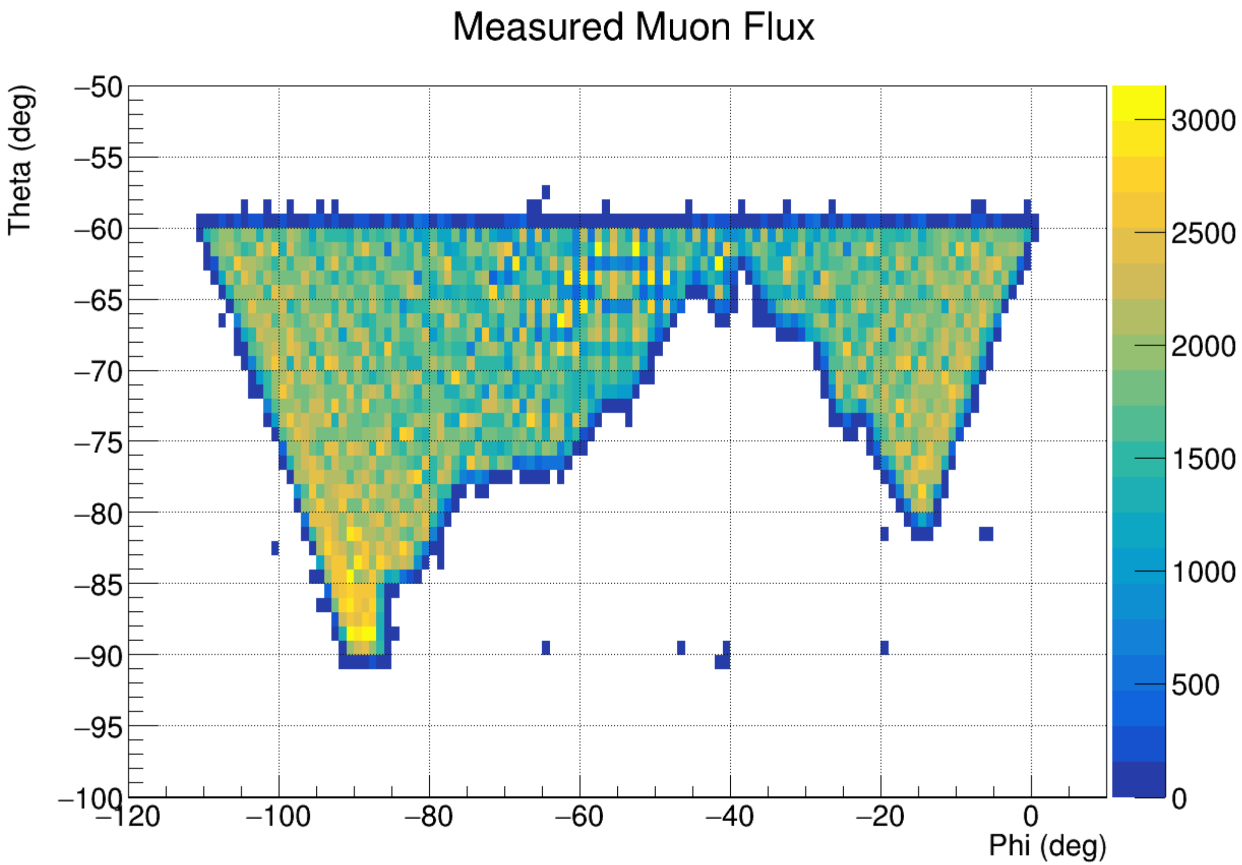
- **Muon tomography scanner**, suitable for **nuclear waste characterization,** by Lynkeos Technology (Scotland)
- First design with MA-PMTs detectors and MAROC chip readout
- Device successfully deployed at Sellafield site (UK)
- Upgrading to **SiPMs** detectors in 2021 – readout electronics based on FERS



First-of-a-kind muography for nuclear waste characterization
D. Mahon *et al.*
Philos. Trans. R. Soc. A, 377 (2018), p. 0048, 10.1098/rsta.2018.0048

Muon tomography - environmental

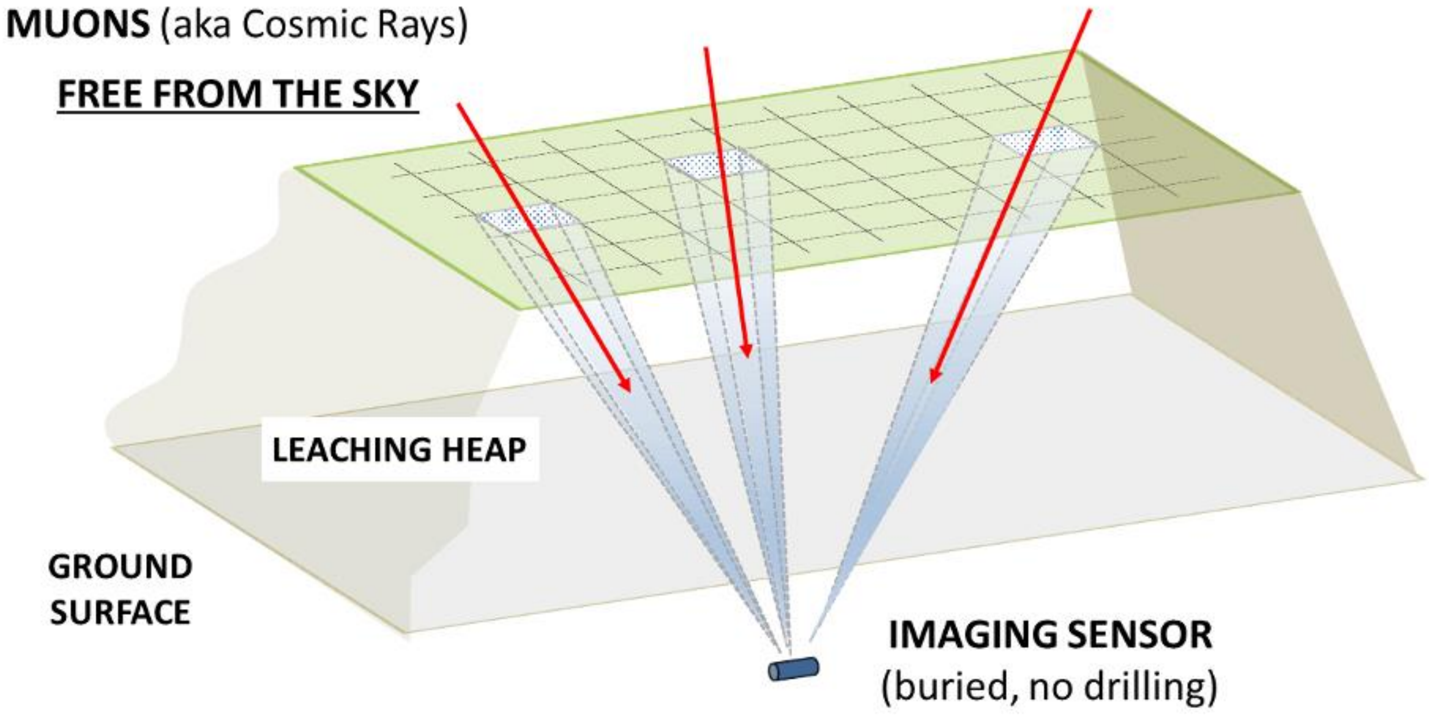
- **Muon tomography scanner** to monitor **glaciers**
- Designed based on bundles of scintillating fibers and A5202 electronics
- Good preliminary results from simulation



A new detector to muon tomography for glaciers melting monitoring
S.Rabaglia *et al.*
https://agenda.infn.it/event/28874/contributions/170201/

Muon tomography - geophysics

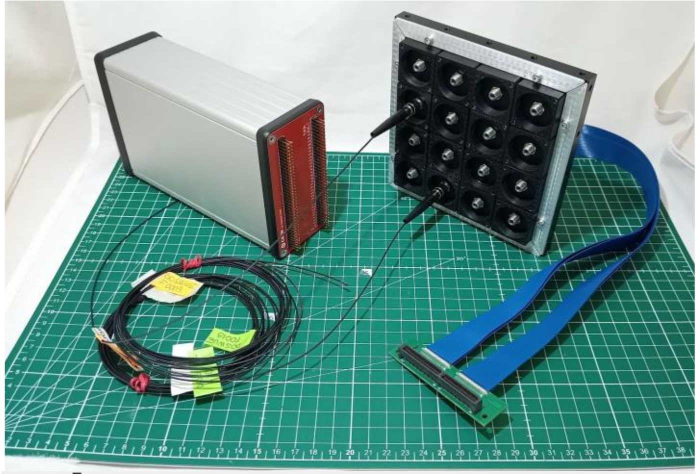
- **Imaging sensor** for mining, Oil&Gas
- Based on FERS units with Concentrator board

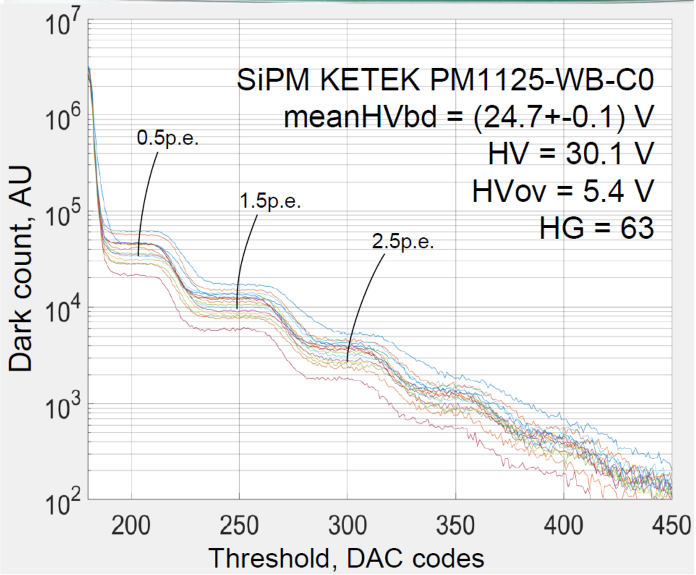


https://muonvision.com/technology-how-does-muon-vision-work/

ORIGIN project

- **Biomedical application:** real-time, in-vivo dosimeter imaging for oncological brachytherapy treatment
- **Standalone** desktop version DT5202 used to readout 16/32 PMMA fibers with scintillators in their tip
- CAEN DT5202 demonstrated to have a good imaging resolution and uniformity among channels
- Close staircases, clearly-resoluted p.e. and negligible noise

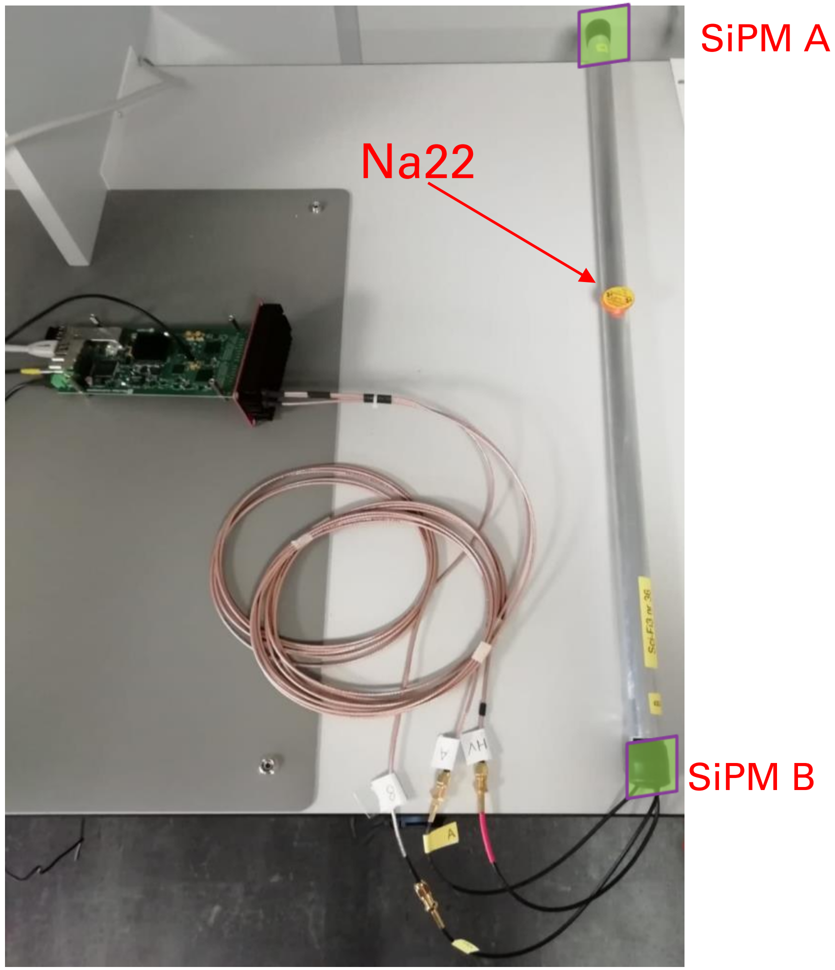




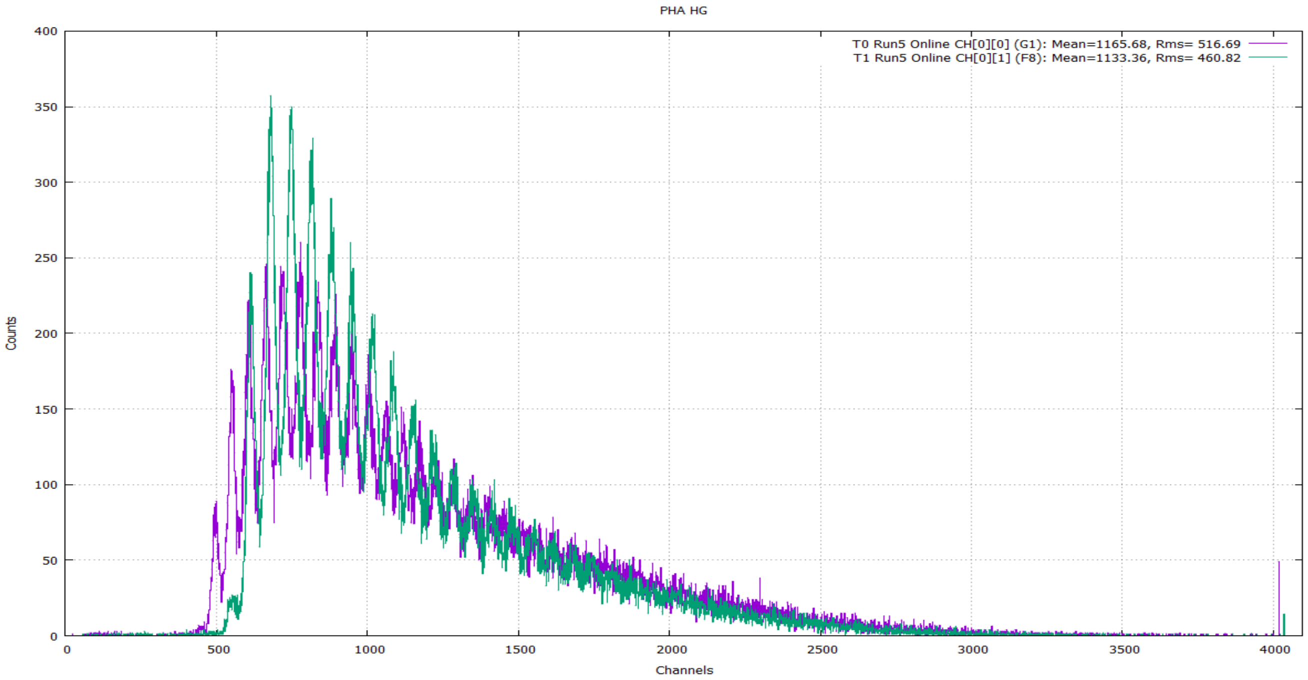
See NSS-MIC 2021 poster "Qualification of a Silicon Photomultiplier scalable readout system" (#912)

FERS in D&D operations

https://www.micado-project.eu/

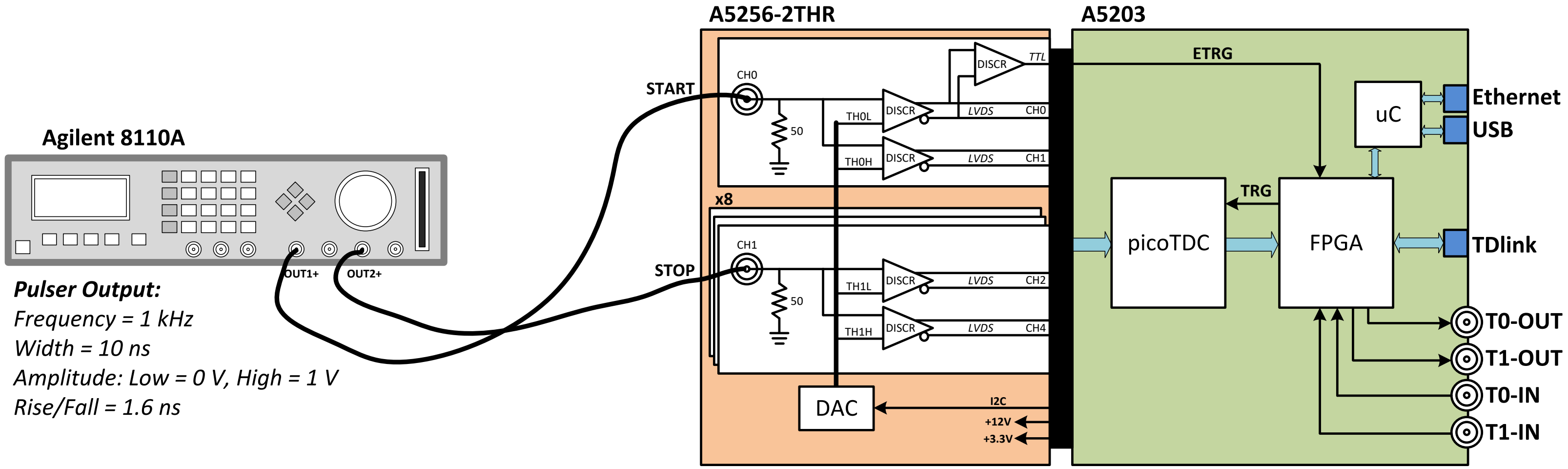


- Detection system for gammas and neutrons, based on SciFi & SiLiF detectors
- **SiPM-coupled SciFiGamma bar** using A5253 adapter
- Coincidence trigger



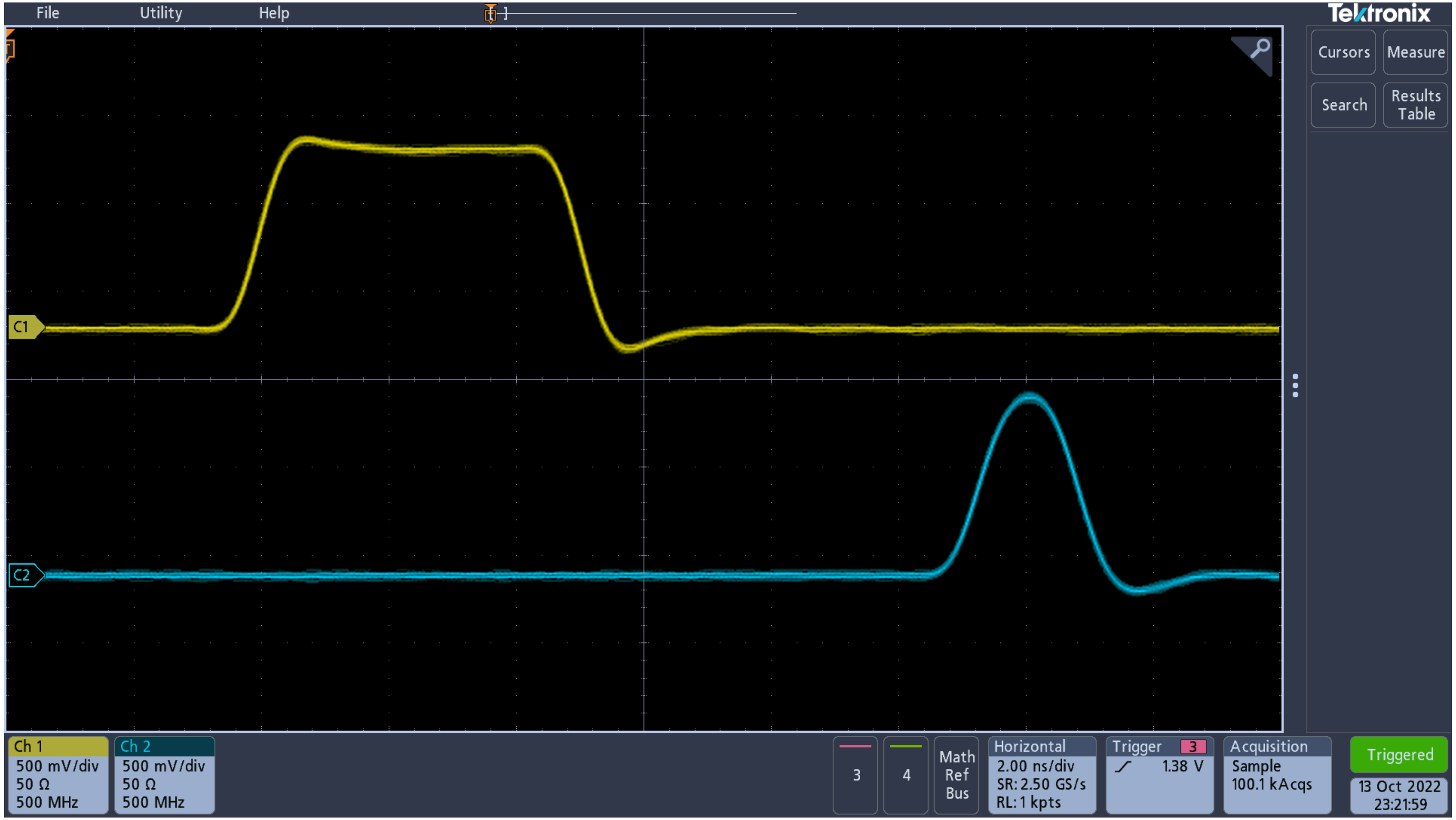
Timing Resolution with fixed amplitude (1)

Setup:
A5203: 64 ch. picoTDC
A5256: 16+1 ch. Dual Threshold Fast Discriminator
Agilent A8110A: Dual Pulse Generator (1V, 0.8 ns rising edge)



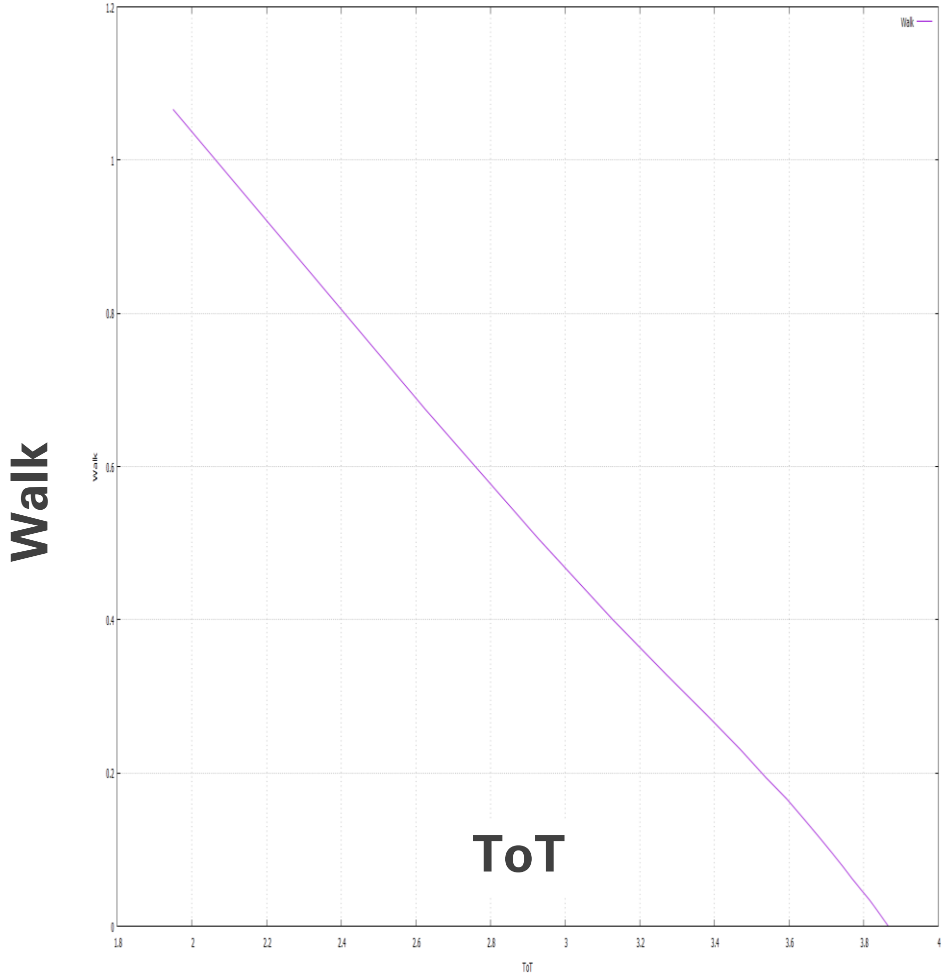
	Low Thr		High Thr	
	Mean	RMS	Mean	RMS
deltaT (start-stop)	4.7 ns	5 ps	4.9 ns	6 ps
ToT	10.6 ns	6.5 ps	10.2 ns	5.5 ps

Pulses

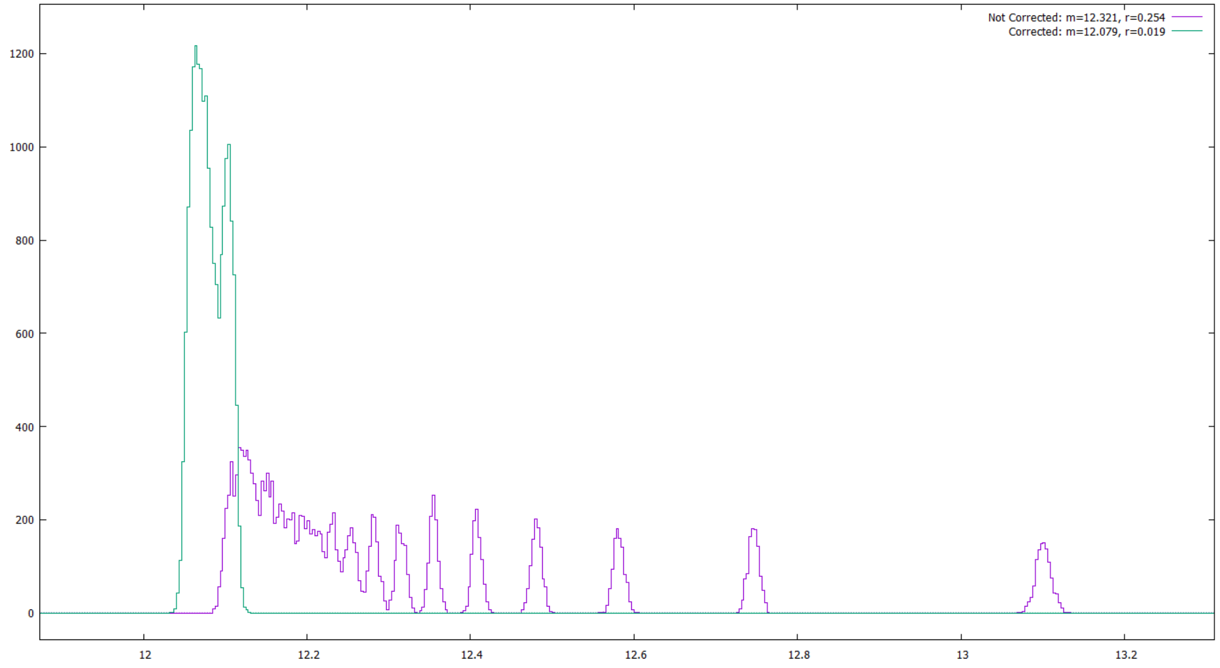


File
Utility
Help
Tektronix
Cursors
Measure
Search
Results Table
C1
C2
Ch 1
500 mV/div
50 Ω
500 MHz
Ch 2
500 mV/div
50 Ω
500 MHz
3
4
Math Ref Bus
Horizontal
2.00 ns/div
SR: 2.50 GS/s
RL: 1 kpts
Trigger
3
1.38 V
Acquisition
Sample
100.1 kAcqs
Triggered
13 Oct 2022
23:21:59

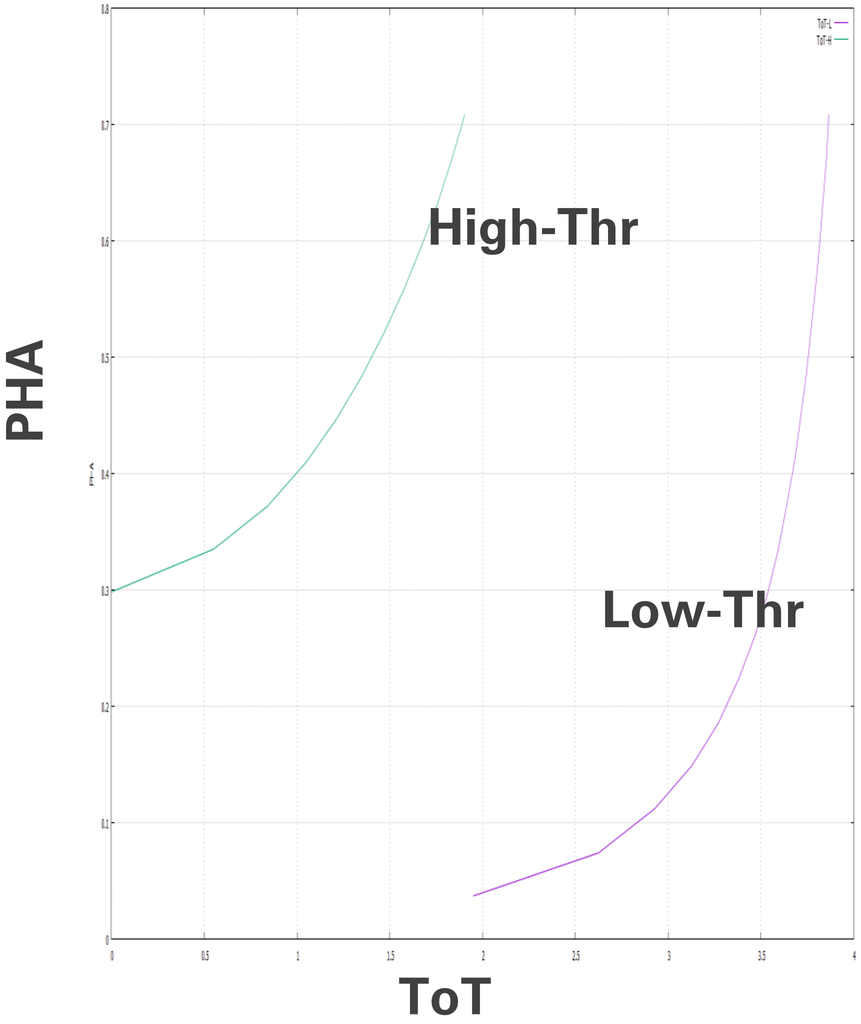
Walk correction



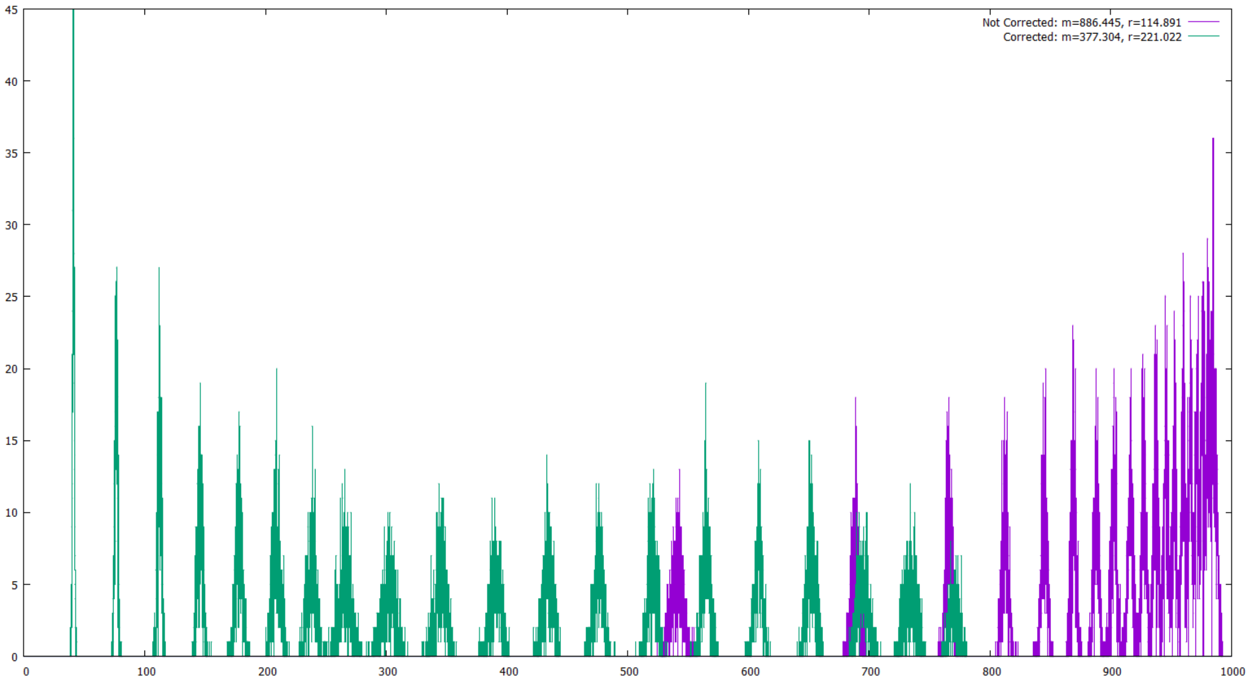
Amplitude Sweep from 35 mV to 750 mV:
Low Thr. = 30 mV, High Thr. = 300 mV
ΔT = 254 ps RMS (no correction)
Use sampled waveform to calculate **ToT-Walk** curve
ΔT = 19 ps RMS (after correction)



Amplitude Reconstruction



Amplitude Sweep from 35 mV to 750 mV:
Low Thr. = 30 mV, High Thr. = 300 mV
Use sampled waveform to calculate **ToT-PHA** curve
Double Threshold helps in linearization



Conclusion

- FERS is **modular, easy-scalable and flexible**

- A5202 is already used for many SiPM-based applications

- A5203 proved to be suitable for high-res time measurements, even if taking into account walk

A5202: 64 ch. SiPM readout (READY)

- Based on **Citiroc** ASIC
- Preamp, Fast shaper + Discrim, Slow shaper + Peak Sensing + Mux ADC
- High Voltage (up to 80 V) for SiPM biasing
- Acq modes: spectroscopy (PHA), photon counting, timing list mode (ToA + ToT)
- Single photon detection (threshold at 1/3 p.e.). Timing resolution = ~0.3 ns RMS.

A5203: 64/128 ch. TDC (READY)

- Based on **picoTDC** ASIC
- Start-Stop timing resolution = ~5 ps RMS (tested with pulser, 0.8 ns rising edge, 1 Vpp)
- Acq. modes: Common Start, Common Stop, Trigger Matching, Streaming (Leading, Trailing, ToT)
- Extension board (A5256) with fast discriminators (16+1 channels)

A5204: 64 ch. SiPM readout (2023)

- Based on **Radioroc** + **picoTDC** ASICs
- Similar to A5202, with improved timing resolution = 55 ps FWHM (on single photon)

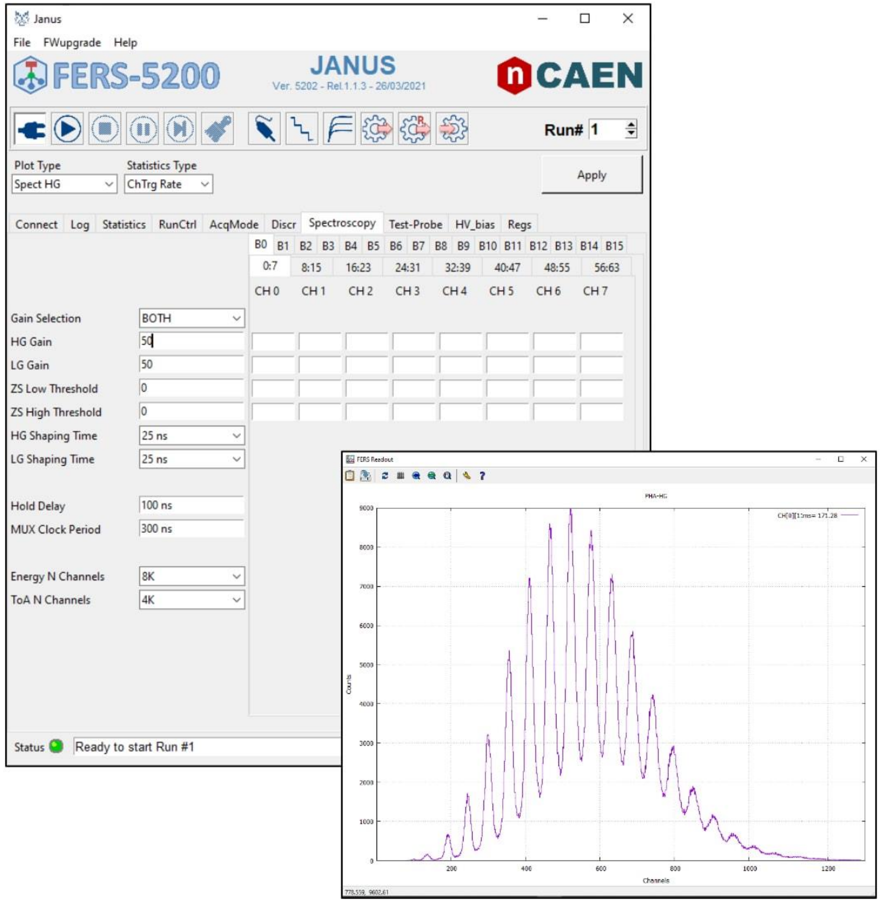
A5205: 64 ch. SSD, GEM, PIN diodes readout (2023)

- Based on **Psiroc** + **picoTDC** ASICs
- Programmable gain: 125 mV/pC up to 4 V/pC. Min trigger threshold = 0,5 fC
- Pos/Neg inputs. Dynamic range up to 5 pC with PHA, 100 pC with ToT
- Timing res = 150 ps RMS @ Q_{IN}=4 fC
- Linearized ToT for high rate, high-res energy and ps timing!

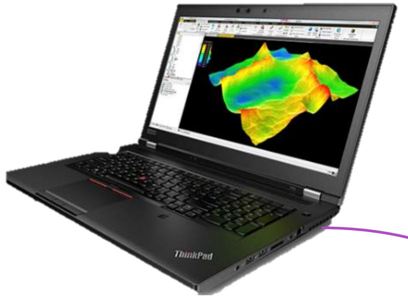
Janus Software

CAEN **Janus software** is free and available for FERS multi-board control and data acquisition:

- ➢Model-dependent GUI for a quick and easy start
- ➢**Open-Source** for user customization
- ➢High Voltage fully controllable by the software
- ➢Management of the acquisition parameters of all connected boards
- ➢Multi parametric Jobs and Runs with time or counts preset
- ➢Data saving of lists in **.bin**, **.txt** format
- ➢Statistics and Spectra visualization

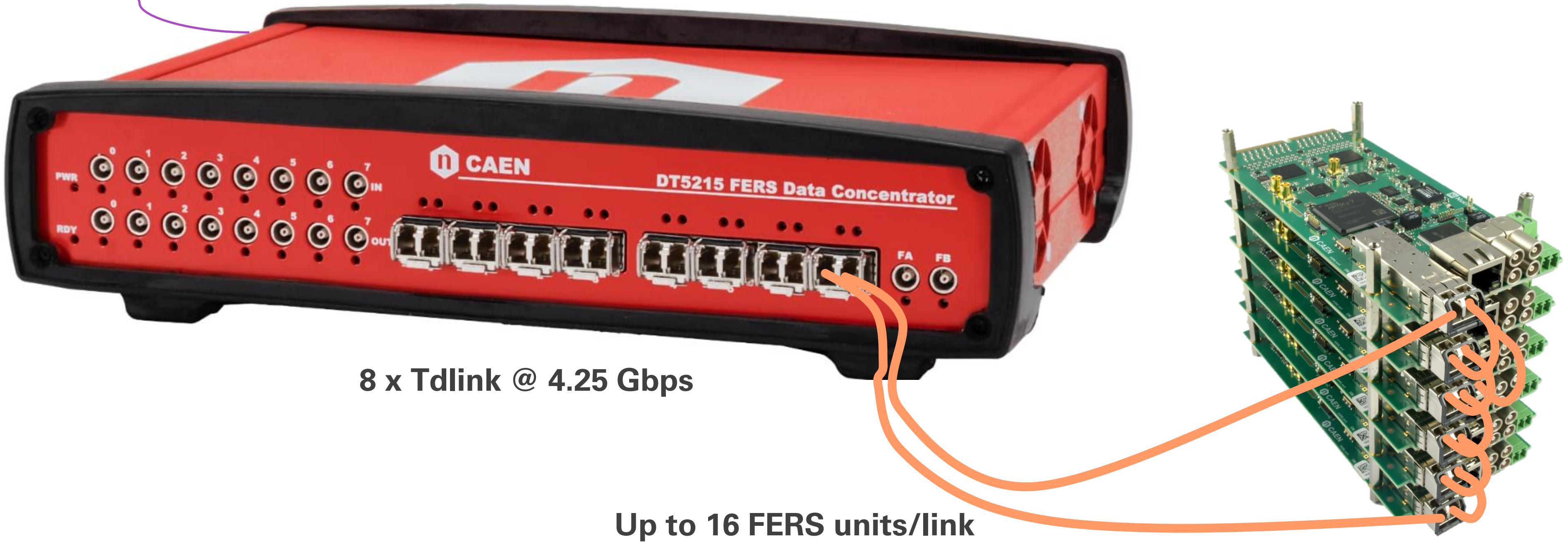


DT5215 – Concentrator Board



Readout Interface
- 1/10 Gbps Ethernet
- USB-3.0

Zynq Ultrascale SoC – FPGA and ARM
- Readout process management
- Event sorting
- Event Building



8 x Tdlink @ 4.25 Gbps

Up to 16 FERS units/link