# Characterization of ToASt ASIC for the readout of the PANDA MVD strip detector

**Francesca Lenta[1,2], Daniela Calvo[1], Fabio Cossio[1], Giovanni Mazza[1], Richard Wheadon[1], Kai-Thomas Brinkmann[5], Michele Caselle[3], Andreas Kopmann[3], Olena Manzhura[3], Marvin Peter[5], Vladimir Sidorenko[3], Pavel Staněk[4], Tobias Stockmanns[6], Lukáš Tomášek[4], Nils Tröll[4], Kai Lukas Unger[3], Hans-Georg Zaunick[5]**

[1]I.N.F.N. sezione di Torino
[2]Politecnico di Torino
[3]Karlsruher Institut für Technologie
[4]Department of Physics, Czech technical university in Prague
[5]Justs-Liebig-Universitat Giessen
[6]Jülich Forschungszentrum

## ABSTRACT

The ToASt ASIC is a 64-channel integrated circuit developed for the readout of the silicon strip detector that will be placed in the Micro-Vertex of the PANDA experiment. ToASt is implemented in a commercial 110 nm CMOS technology and can provide information on the position, time, and deposited energy of the particle passing through the detector. Its time resolution is given by its 160 MHz primary clock. The ASIC has been developed in the framework of the European FAIRnet project.

The Micro Vertex Detector (MVD) of the PANDA experiment will consist of two parts: a barrel section located around disk; a disk section in the forward position. These two sections will be equipped with Silicon Pixel (SPDs) and Silicon Strip Detectors (SSDs).

The ToASt analogue front end is divided into two parts. The first part is composed by a charge-sensitive preamplifier that can be programmed to accept signals of both polarities, a programmable shaper, and a current buffer. The second part consists of a Time-over-Threshold (ToT) stage with linear discharge and two comparators with independent thresholds. The double threshold information can be used to reduce time jitter on small signals by sampling the time information with a low threshold, where the signal edge is faster, and using a higher threshold to validate the event, thus reducing noise events.

Space information is provided by the channel number, while time and energy information can be obtained from two time stamps obtained by storing the value of a global counter on the rising and falling edge of a comparator. The rising and falling times provide the timing information, while the energy information is obtained from the difference between the times of the falling edge and the rising edge (ToT method).

The 64 channels are divided into 8 regions and each region contains read and configuration logic for 8 channels and a 16-cell FIFO. The 8 regions are read by a global read unit, featuring a 64-cell FIFO and two 160 Mb/s serial links. A global configuration unit manages the configuration information of all regions. The configuration interface is based on a serial link operating at 1/2 the master clock frequency. It controls 16 global configuration registers and $64\times3$ channel configuration registers.

The chip has been characterized electrically both standalone and coupled with sensors, with focus on its noise performances. It has also been characterized for radiation tolerance, both in terms of TID and SEU.

In particular, this work aims to guarantee that the studied ASICs can sustain the levels of ionizing radiation expected in the PANDA experiment and to study the noise characteristics in the two polarities of the ASIC.