



**Politecnico
di Torino**

***Characterization of the radiation tolerant ToASt
ASIC for the readout of the PANDA MVD strip detector***

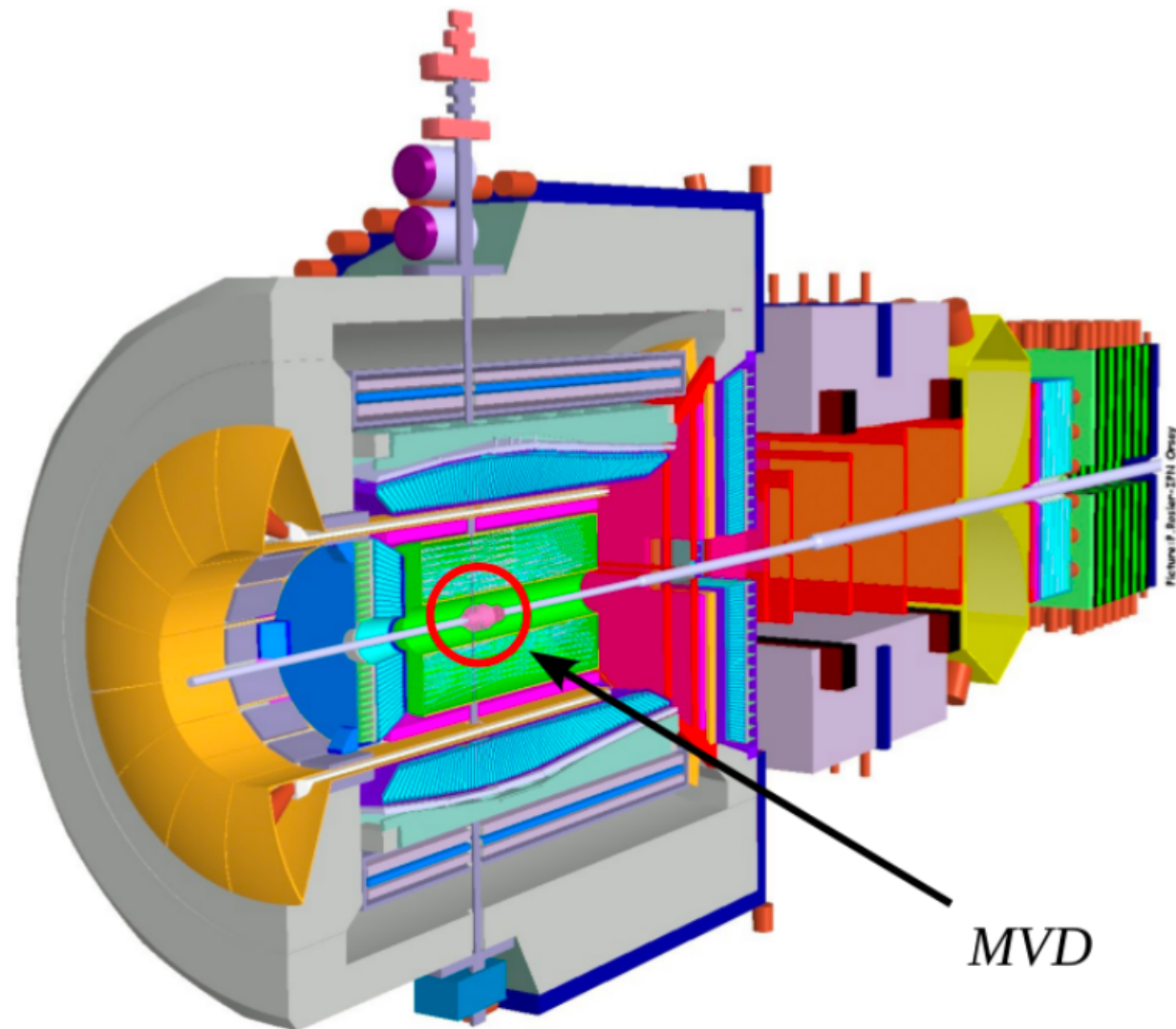
FRANCESCA LENTA ON BEHALF OF THE PANDA-MVD GROUP

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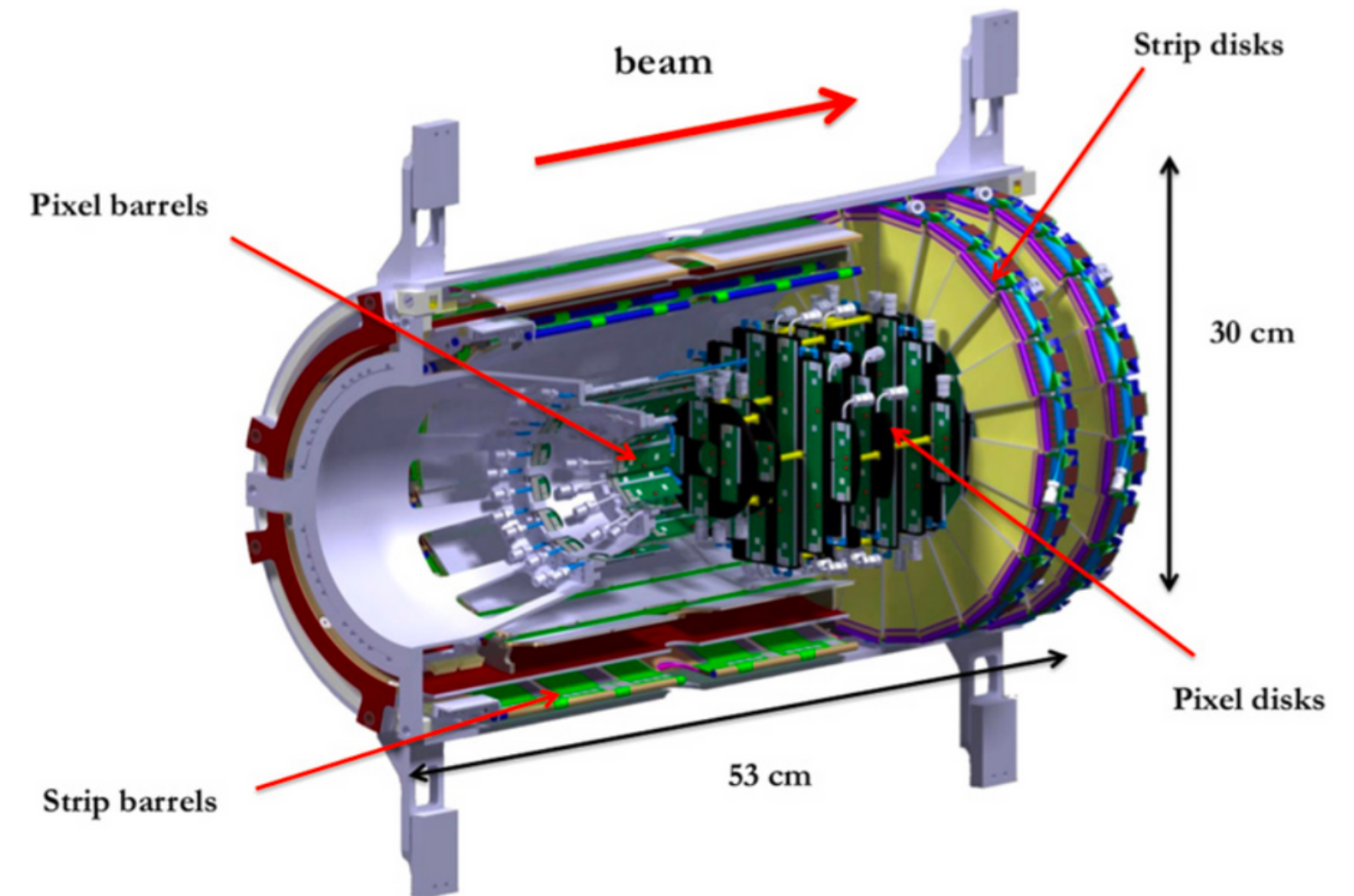
SEPTEMBER 26th 2023

IPRD23 – Siena

The PANDA experiment



- Located at the FAIR facility in Darmstadt
- *antiproton-proton* and *antiproton-nuclei* annihilation reactions
- Fixed target (a target pipe intersects the beam pipe) and triggerless experiment



- Barrel region : 2 layers of Silicon Pixel Detectors (SPDs) + 2 of Silicon Strip Detectors (SSDs)
- Forward region : 4 SPDs disks, 2 SPDs + SSDs disks
- Double side SSDs

Silicon Strip Detector



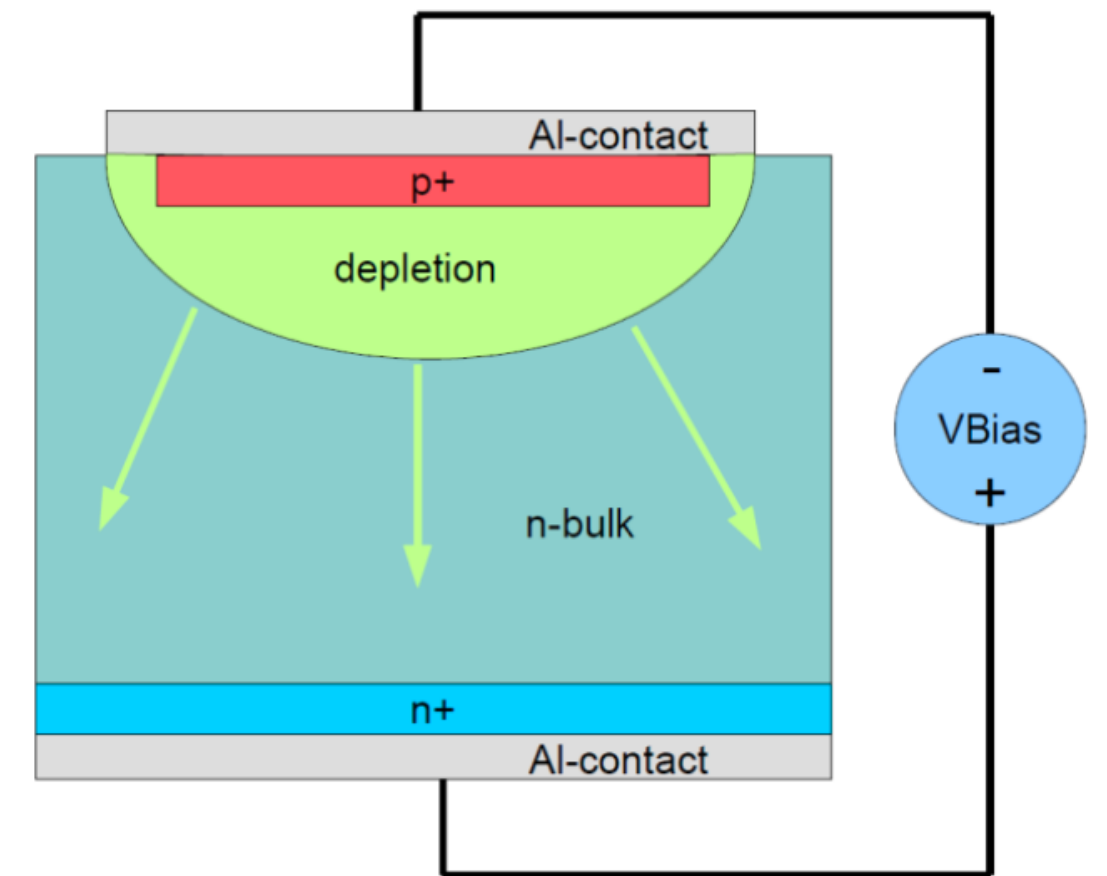
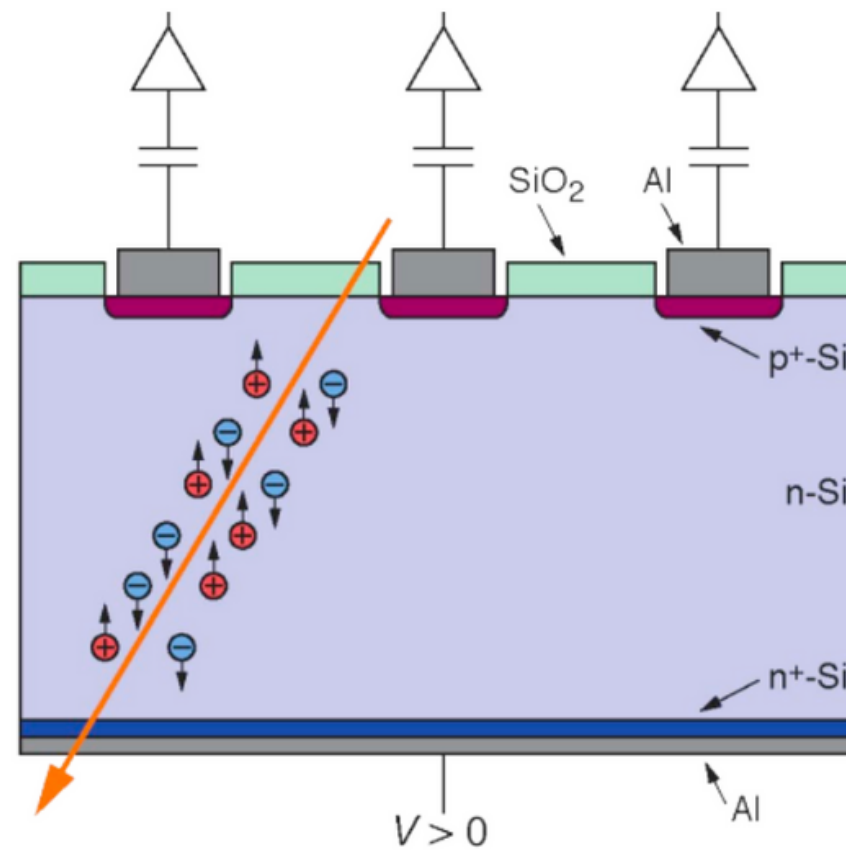
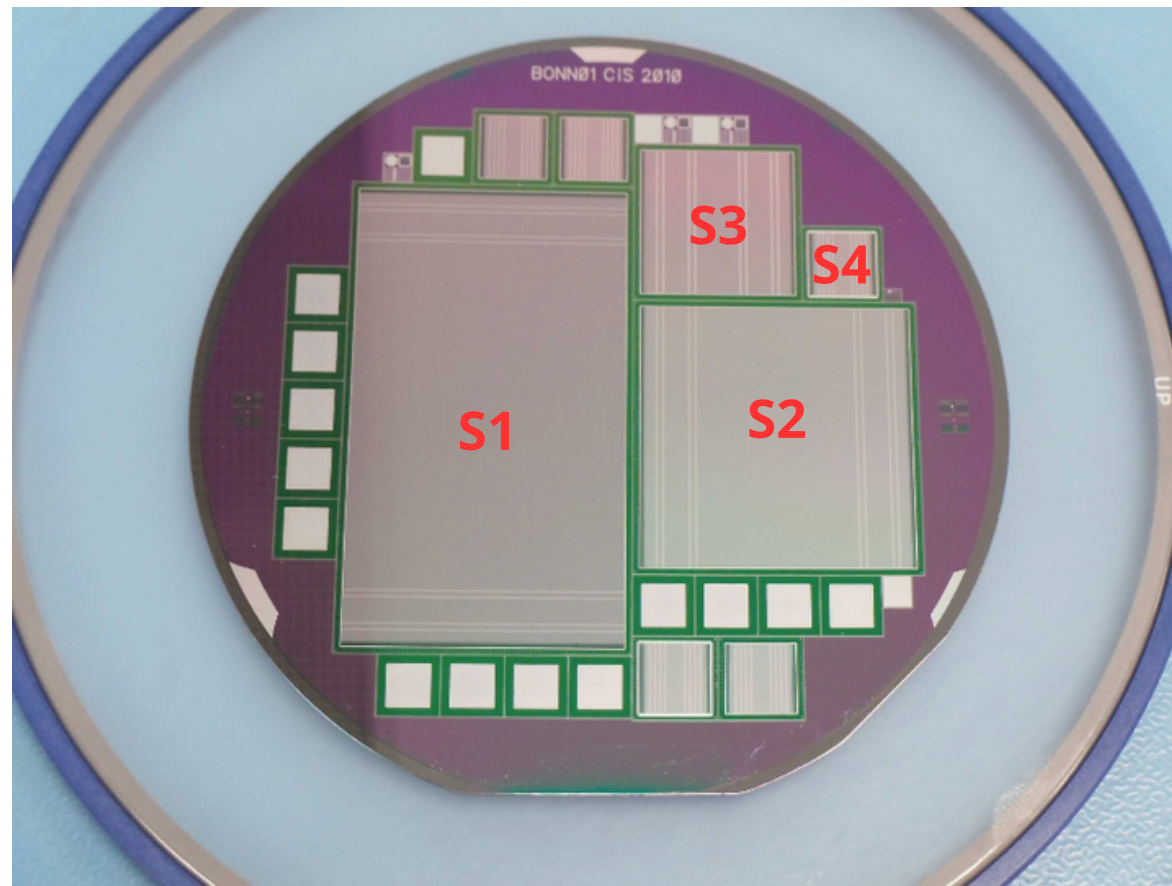
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DOUBLE SIDE SILICON STRIP DETECTOR:

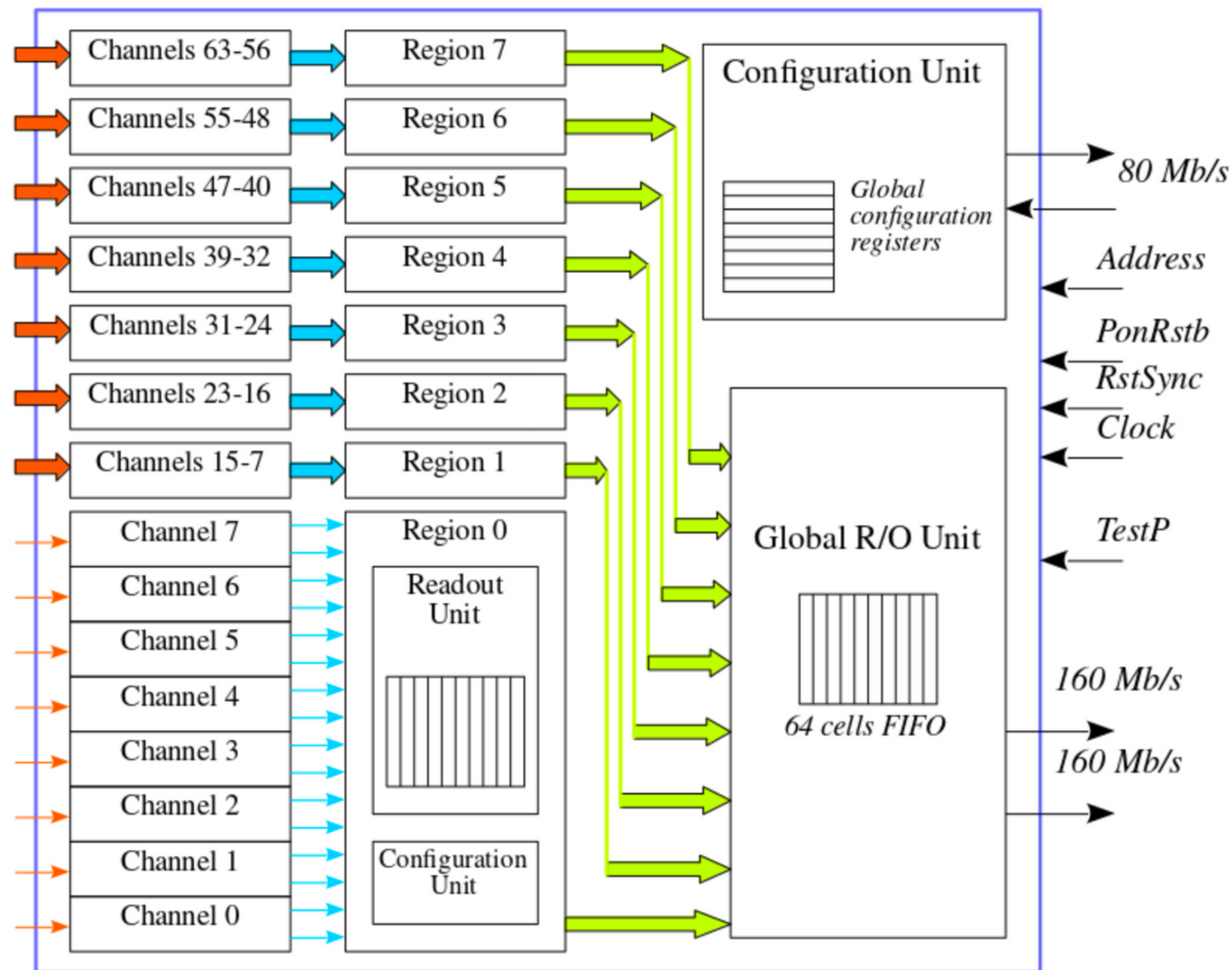
- Doped silicon semiconductor
- PN-junction
- Depletion voltage ≈ 100 V
- Breakdown voltage > 200 V



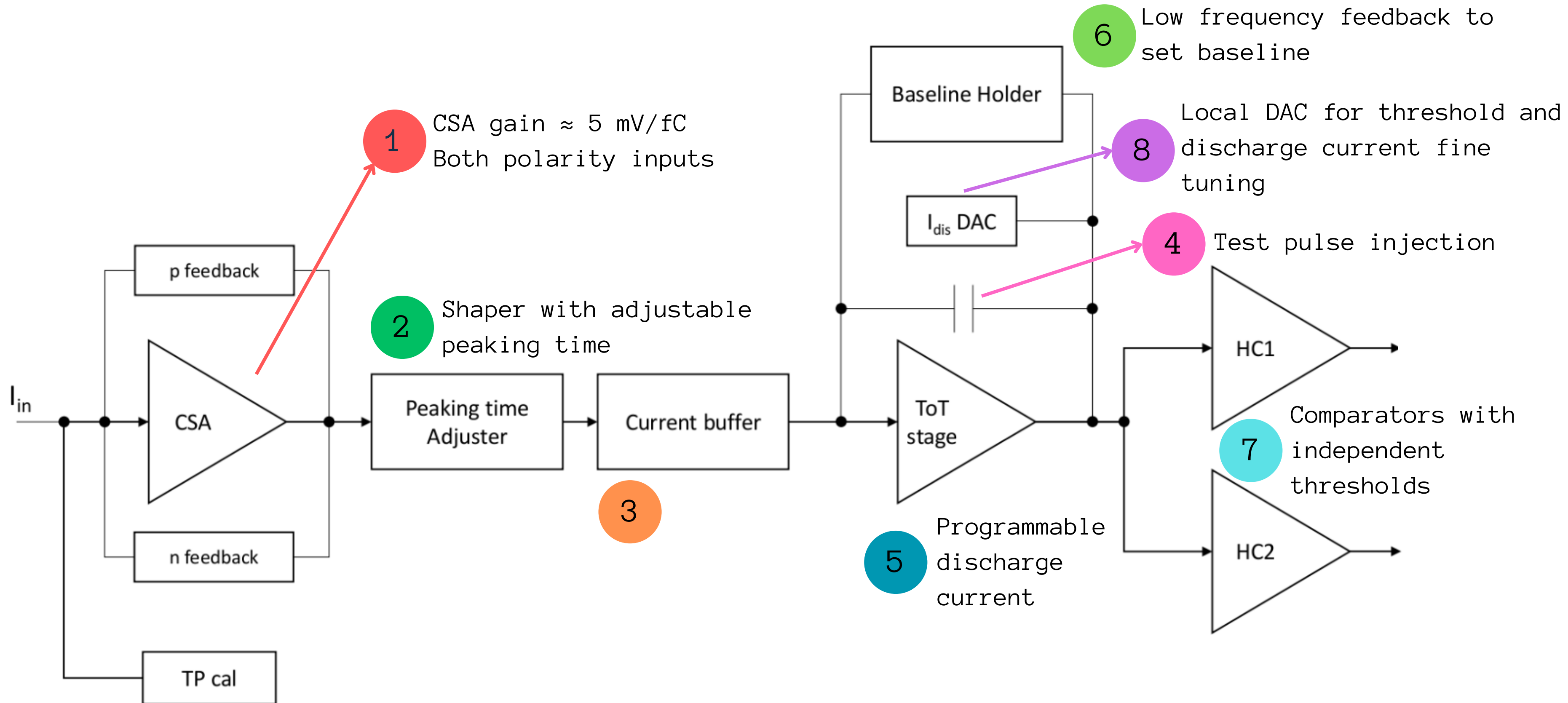
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ToAst specifics and architecture

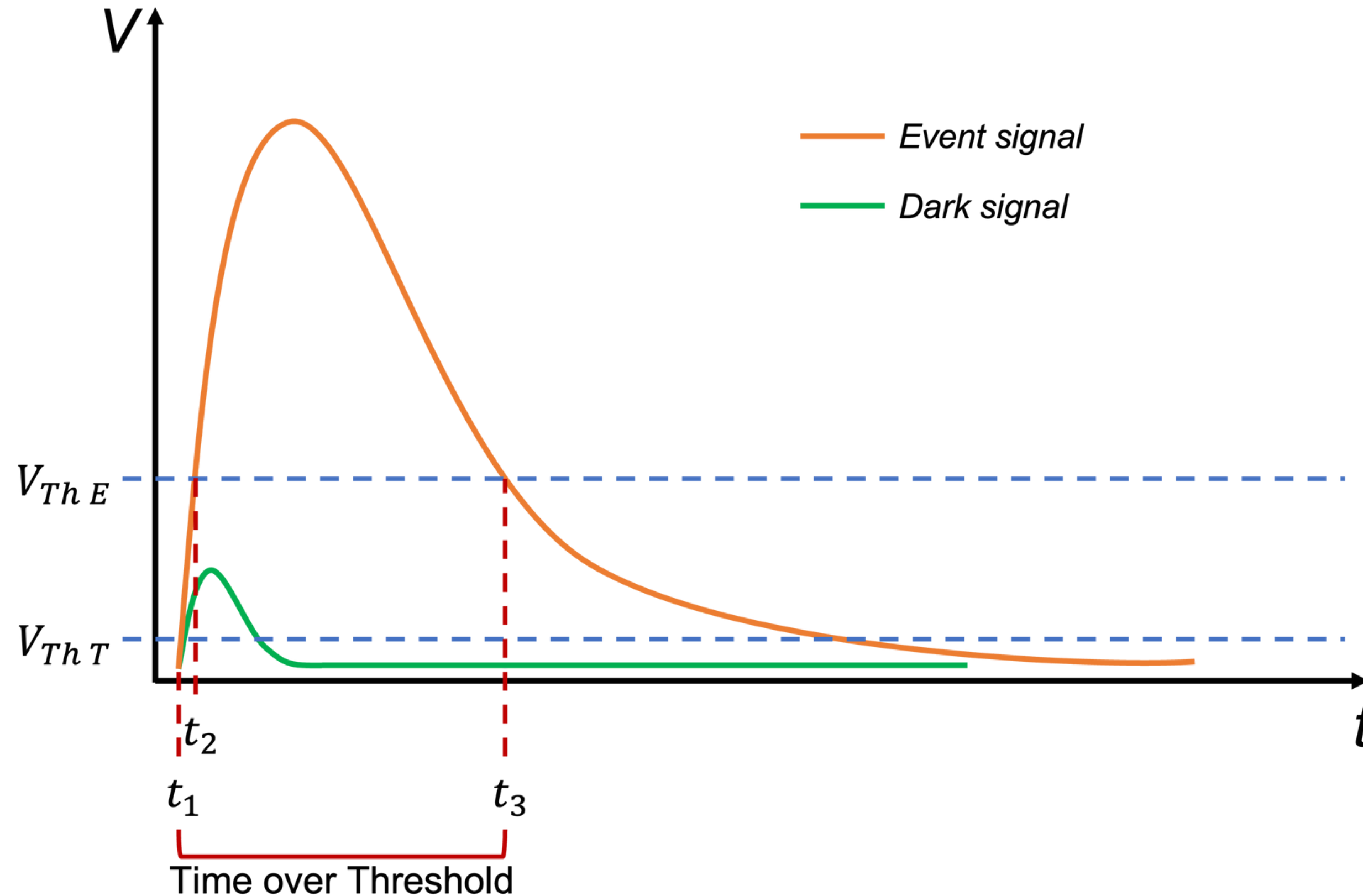
- Each particle crossing the detector has to be associated with its space, energy and its Time of Arrival (ToA)
- 64 readout channels
- Each channel provides the ToA and the charge measurement
- 160MHz clock
- 8 regions with local FIFO
- Two 160 Mb/s serial lines
- Configuration serial link running at half the master clock frequency (80 Mb/s)
- Fully digital interface in order to avoid the transmission of noise sensitive analog signals
- Triplicated logic to protect against single event upsets
- Commercial 110 nm CMOS technology



ToASt analog channel



ToAST time measurement



Two threshold:

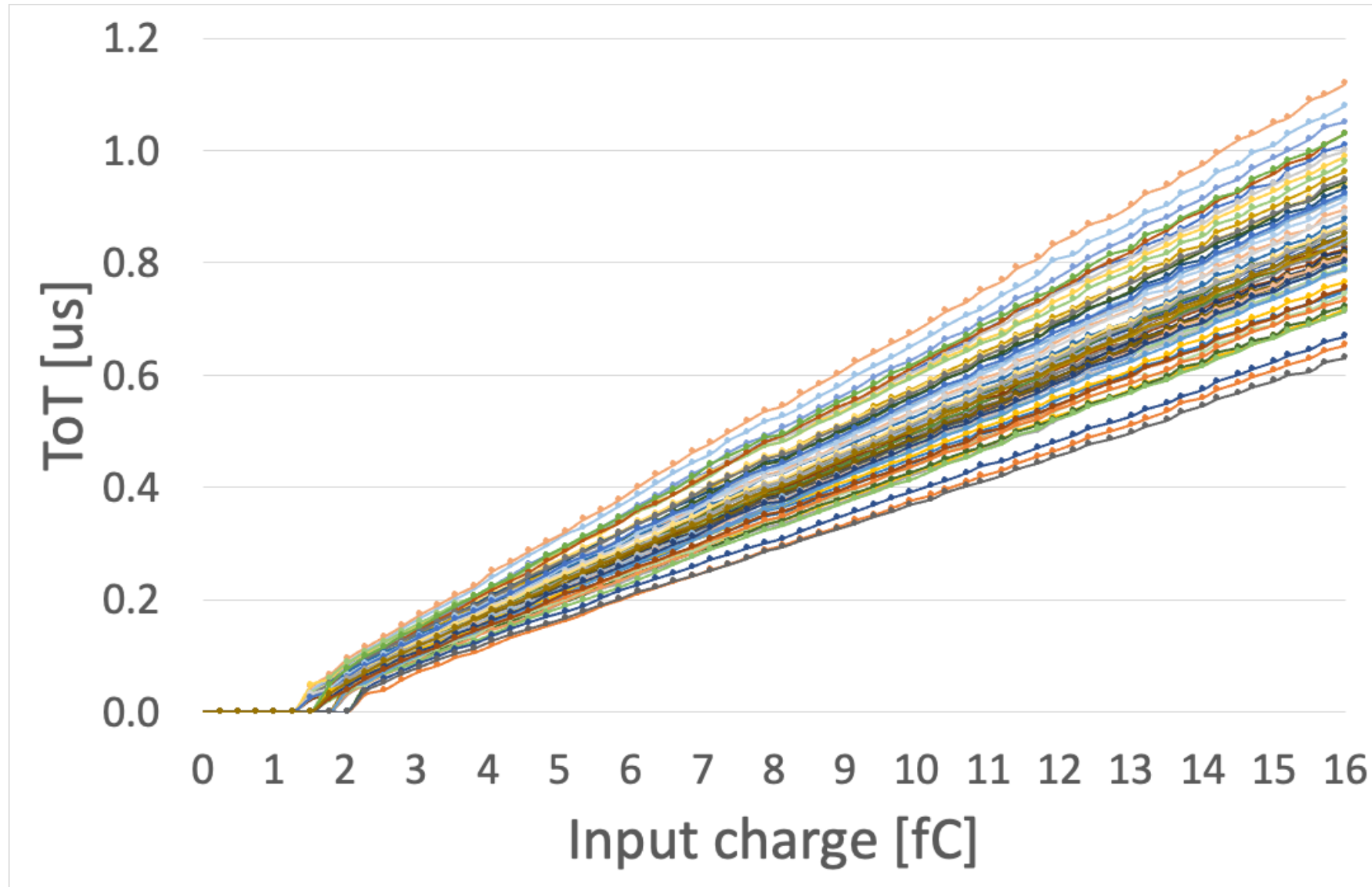
- store the time stamp on the low threshold ($V_{Th T}$)
- validate it with the high threshold ($V_{Th E}$)

$$\text{ToT} = t_3 - t_1$$

Possibility to disable the double threshold

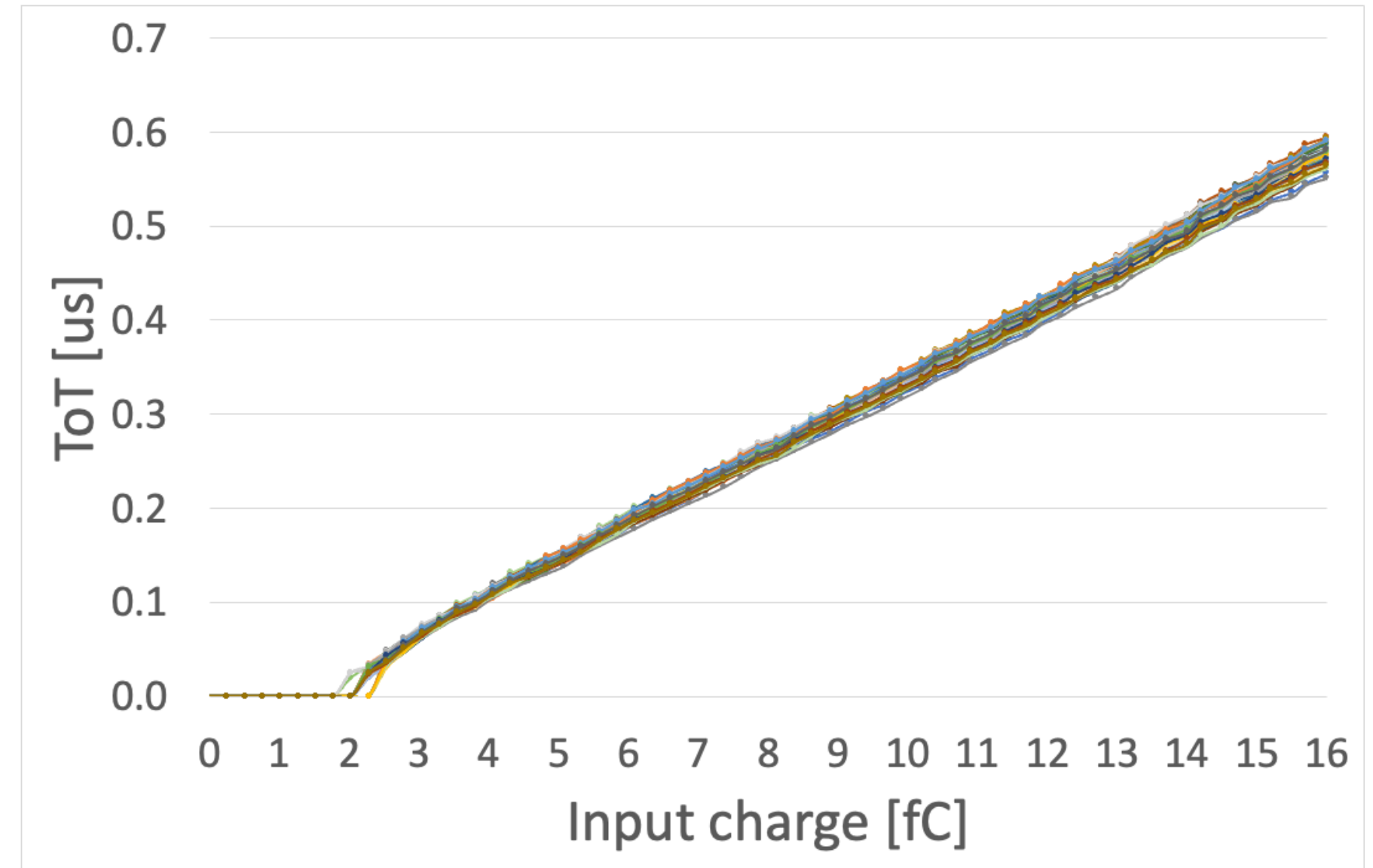
Calibration

BEFORE CALIBRATION



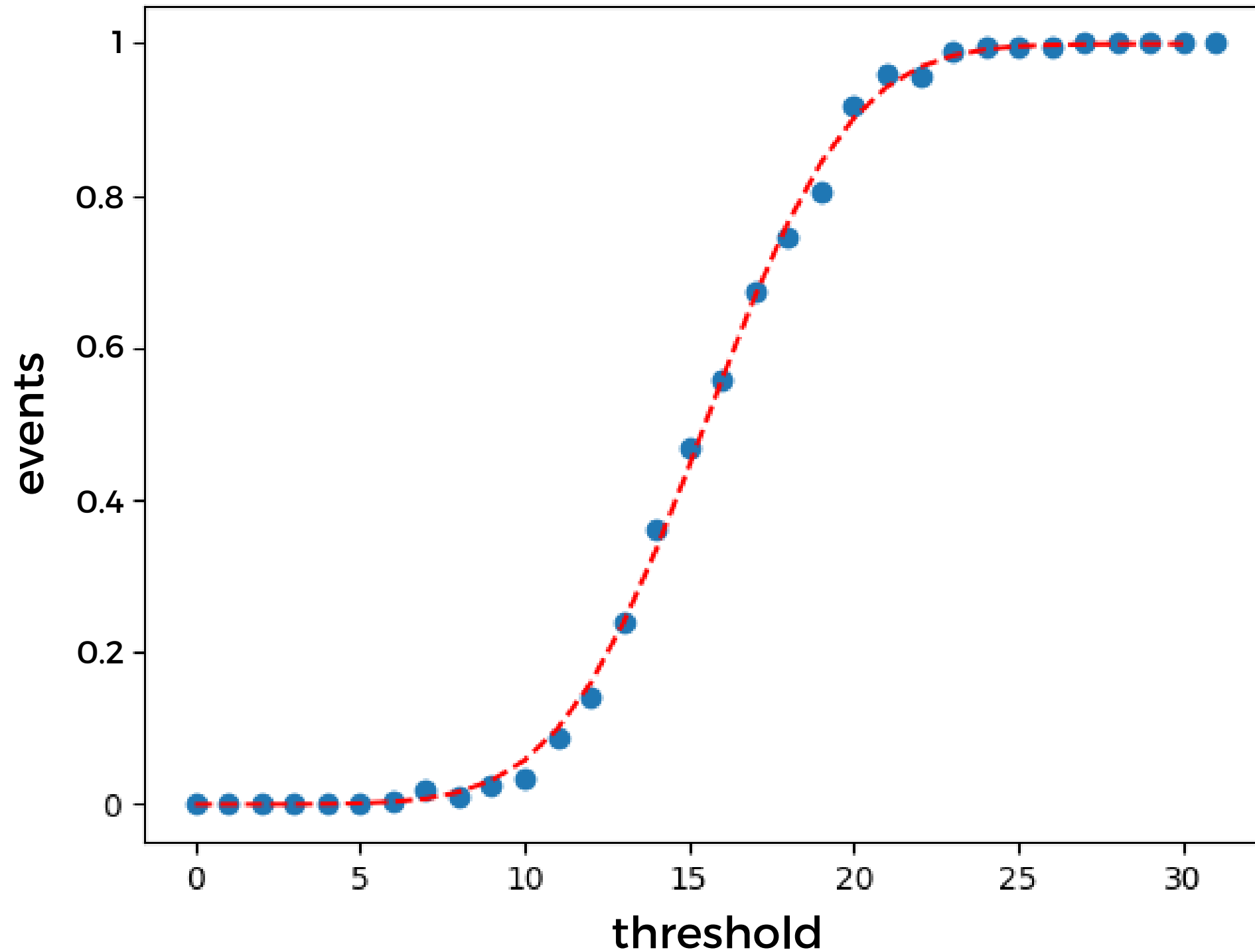
- All 64 channels respond correctly to the Test Pulse
- ToT measured Gain 50 – 60 ns/fC

AFTER CALIBRATION



- Gain spread reduced from 11.7% to 1.5%
- ToT offset spread reduced from 15.6% to 3.5%

Noise measurement

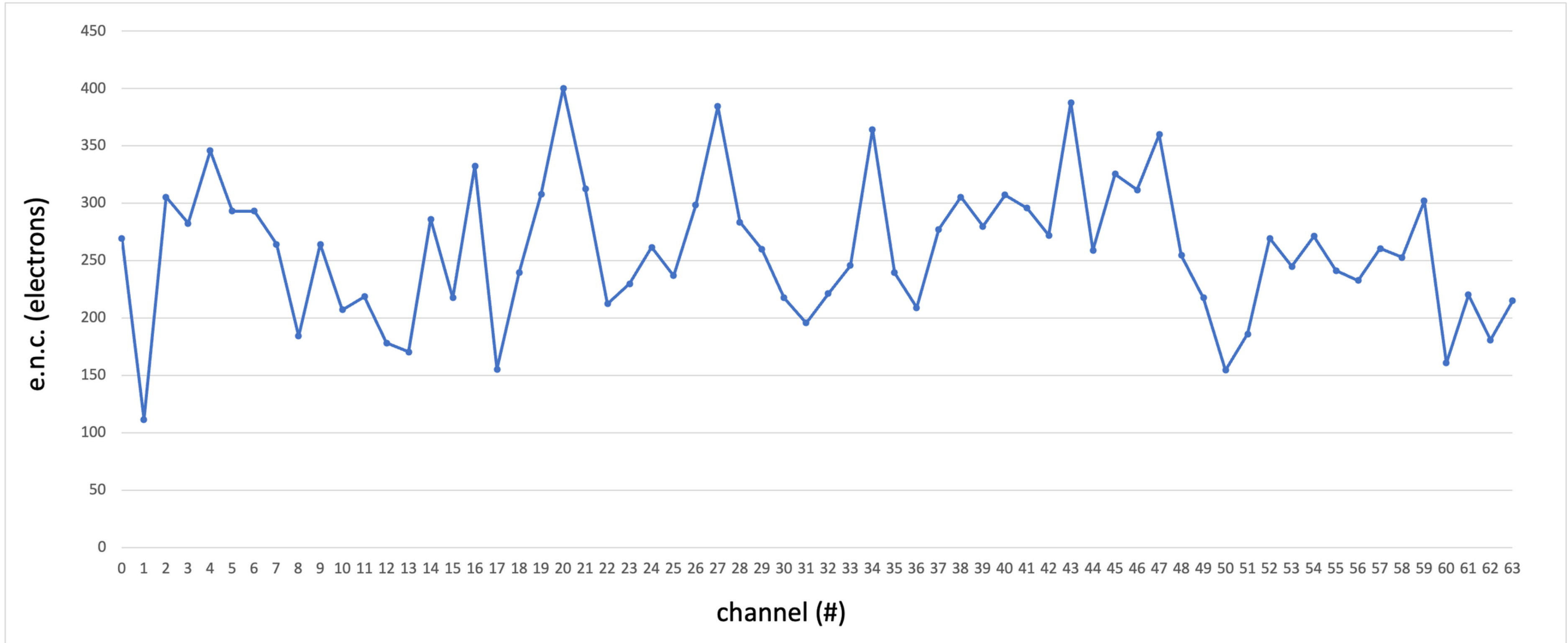


Scan performed with a fixed number of pulses and changing the threshold

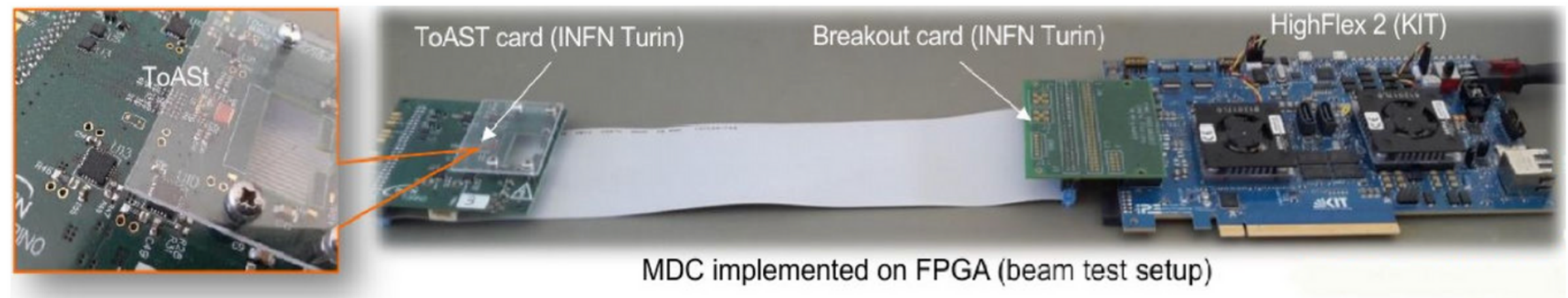
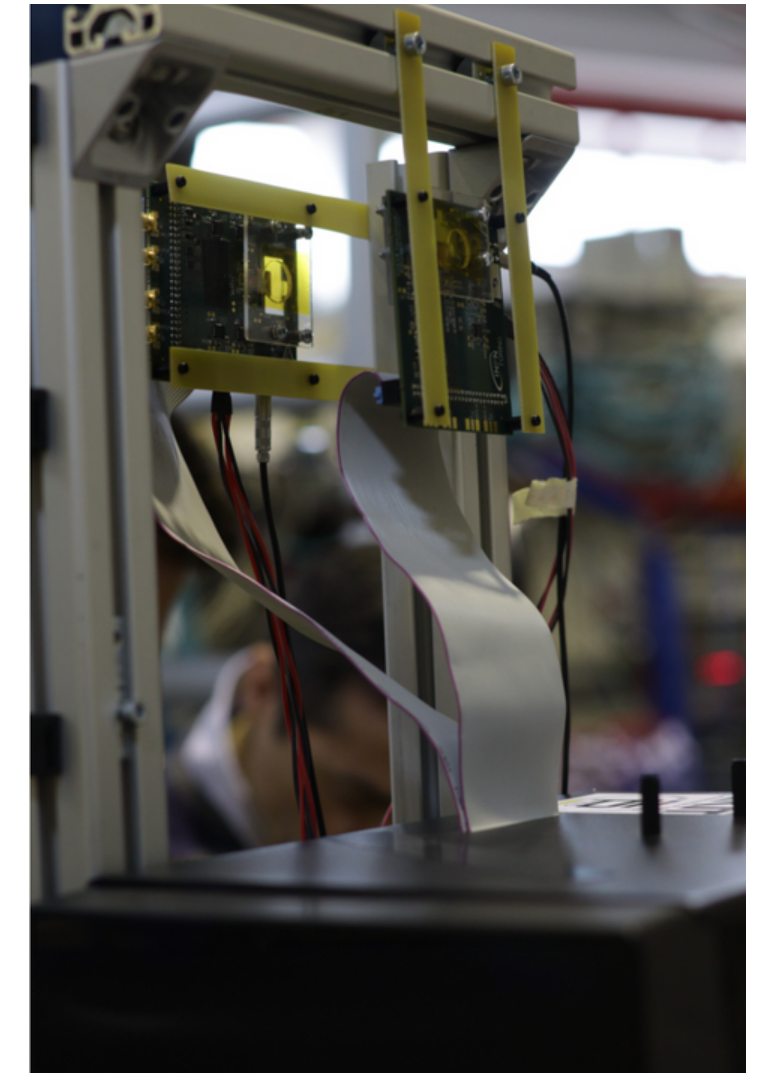
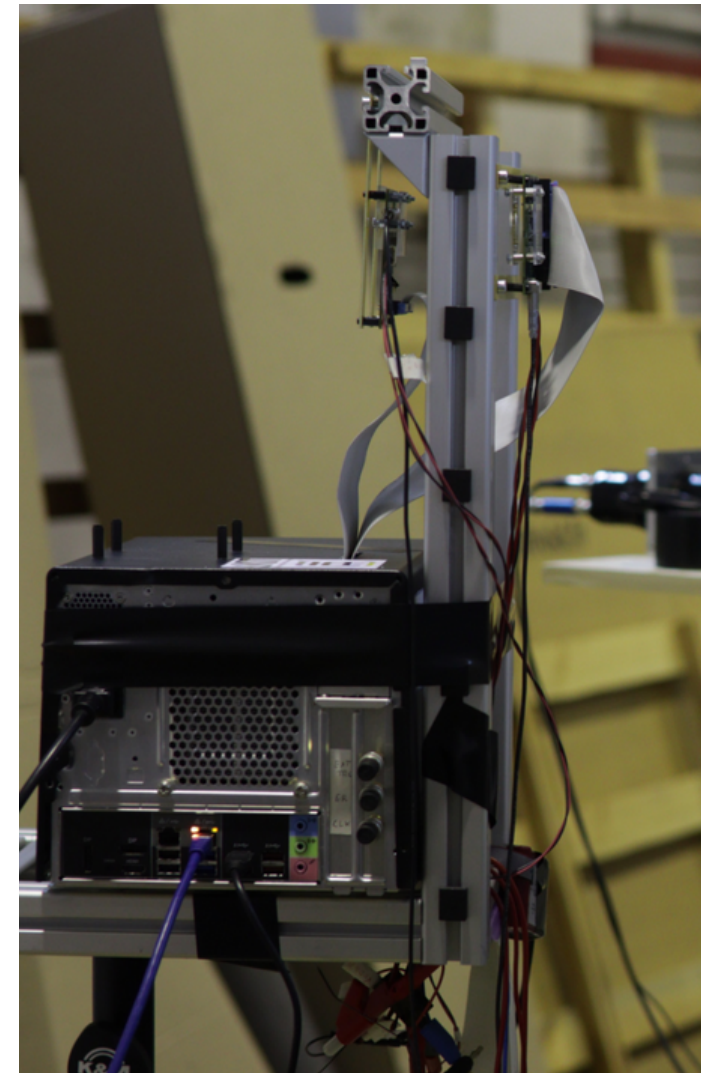
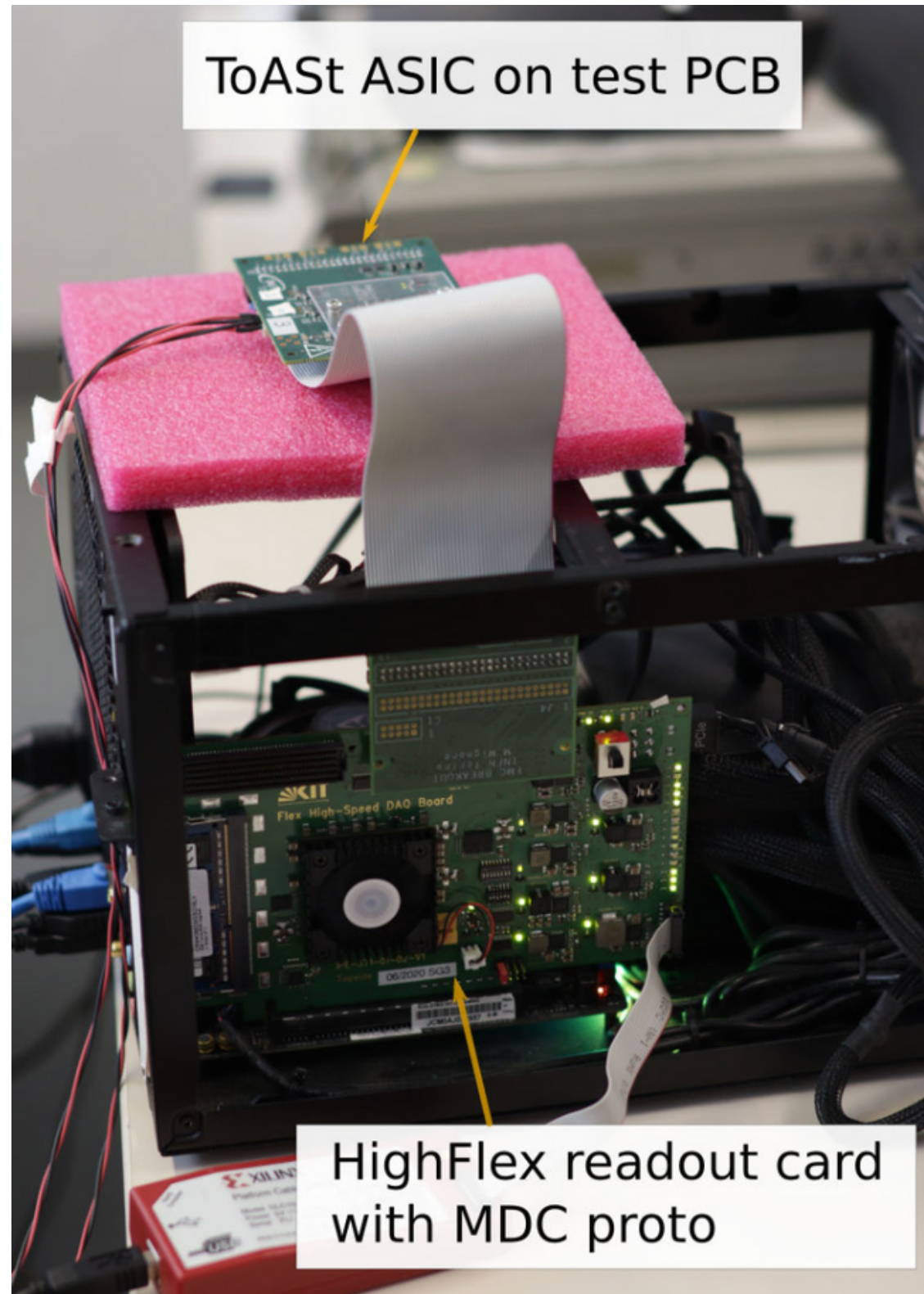
$$f(x') = \frac{N}{2} \left(1 + \frac{2}{\sigma\sqrt{\pi}} \int_0^{x'} \exp(-s^2) dx \right)$$

$$s = \frac{x - \mu}{\sigma}$$

Noise measurement

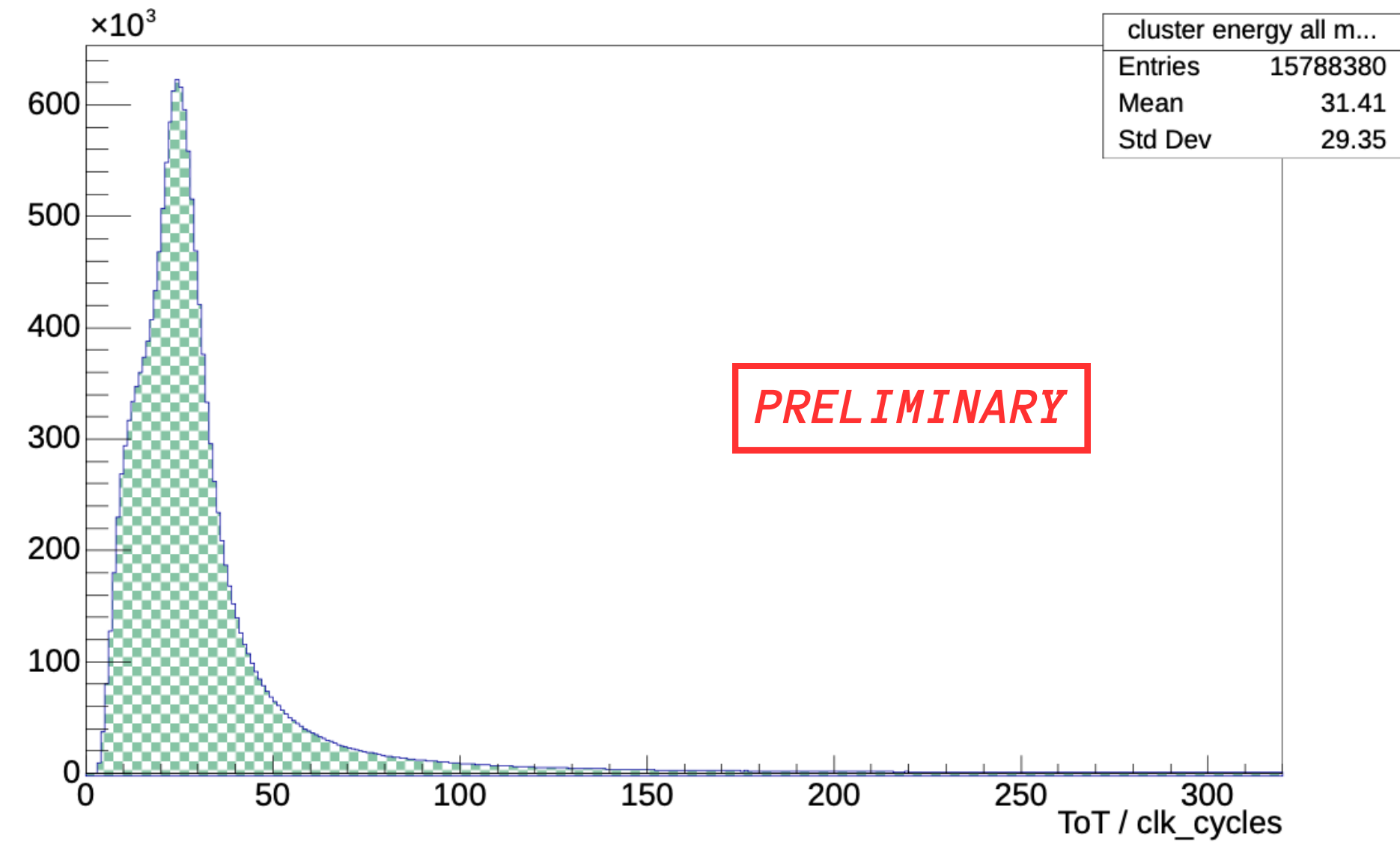


Preliminary beam test measurement

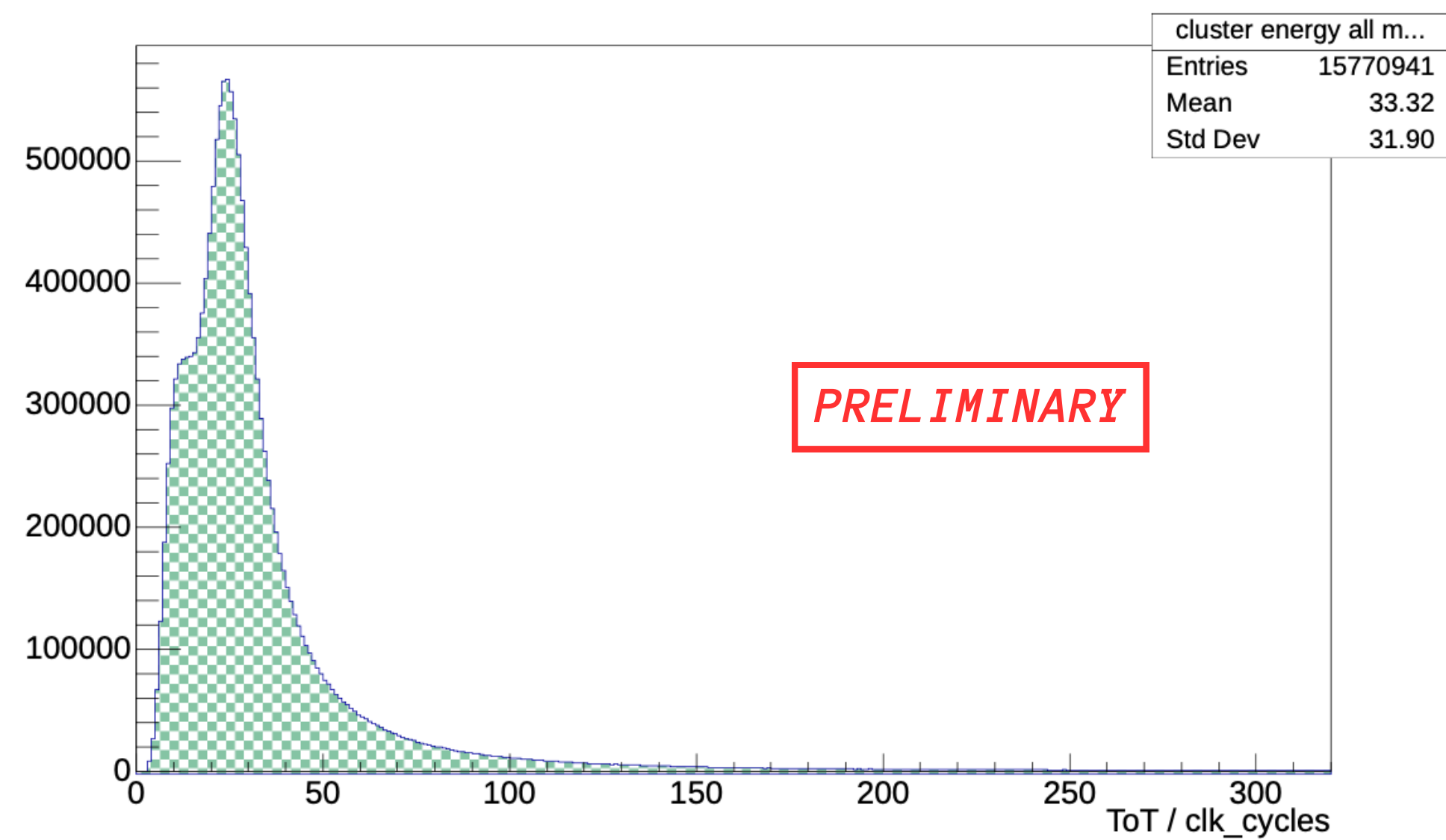


Preliminary beam test measurement

ToAST 0



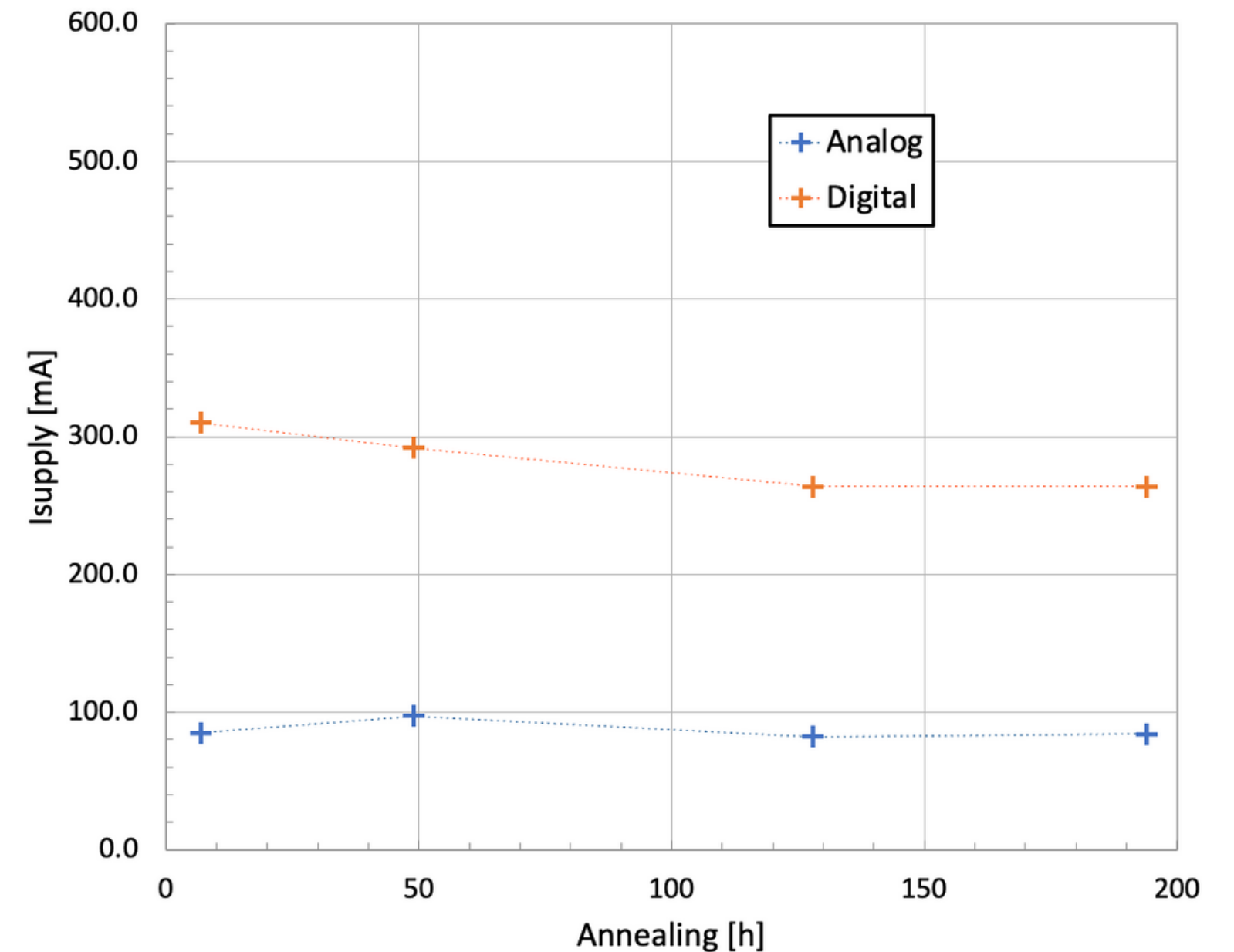
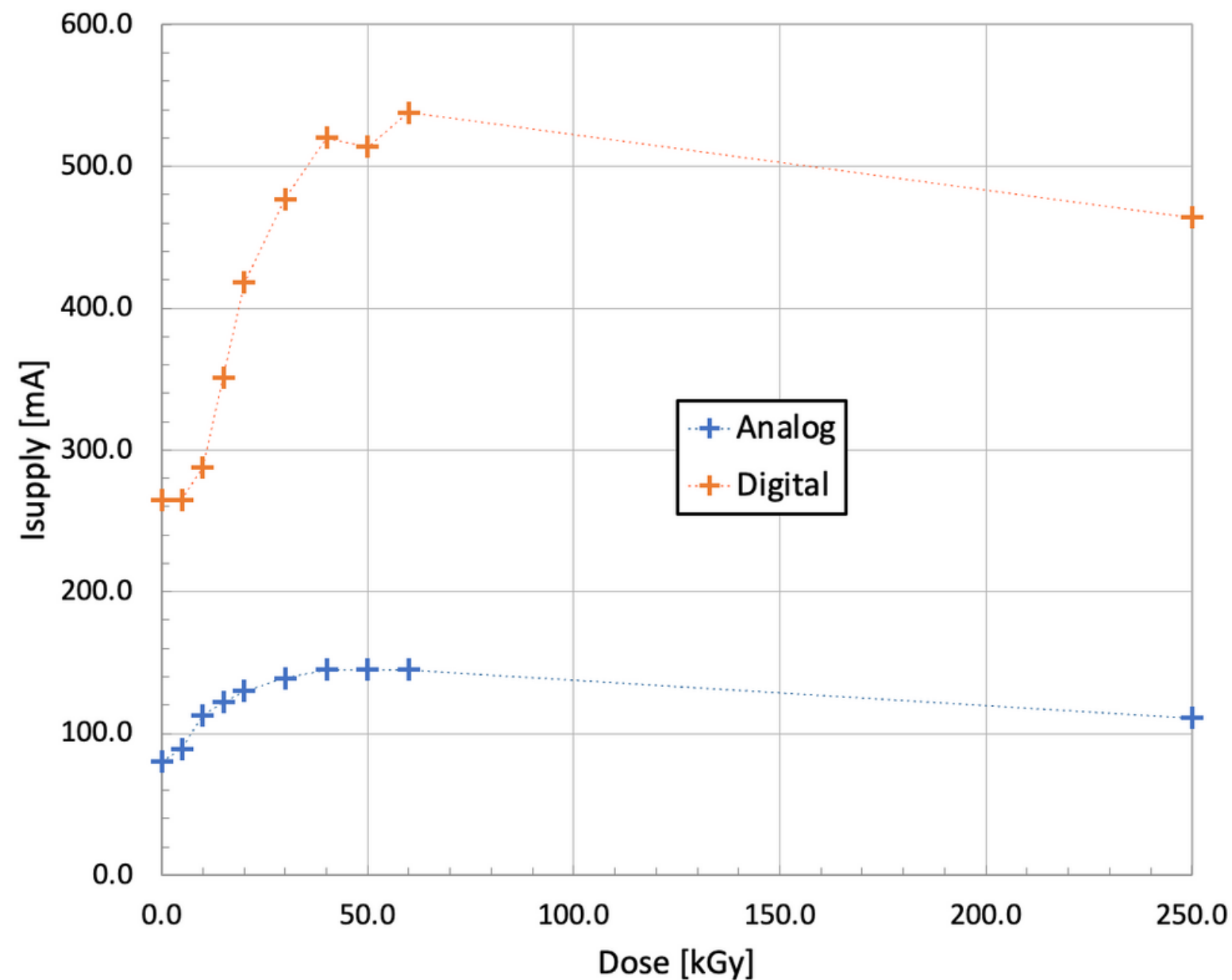
ToAST 1



Under analysis

Total Ionizing Dose tests

SUPPLY CURRENT



- Measure made in INFN Padova in collaboration with *S. Mattiazzo*
- Irradiated up to 250 kGy (dose rate 3.5 Gy/s)

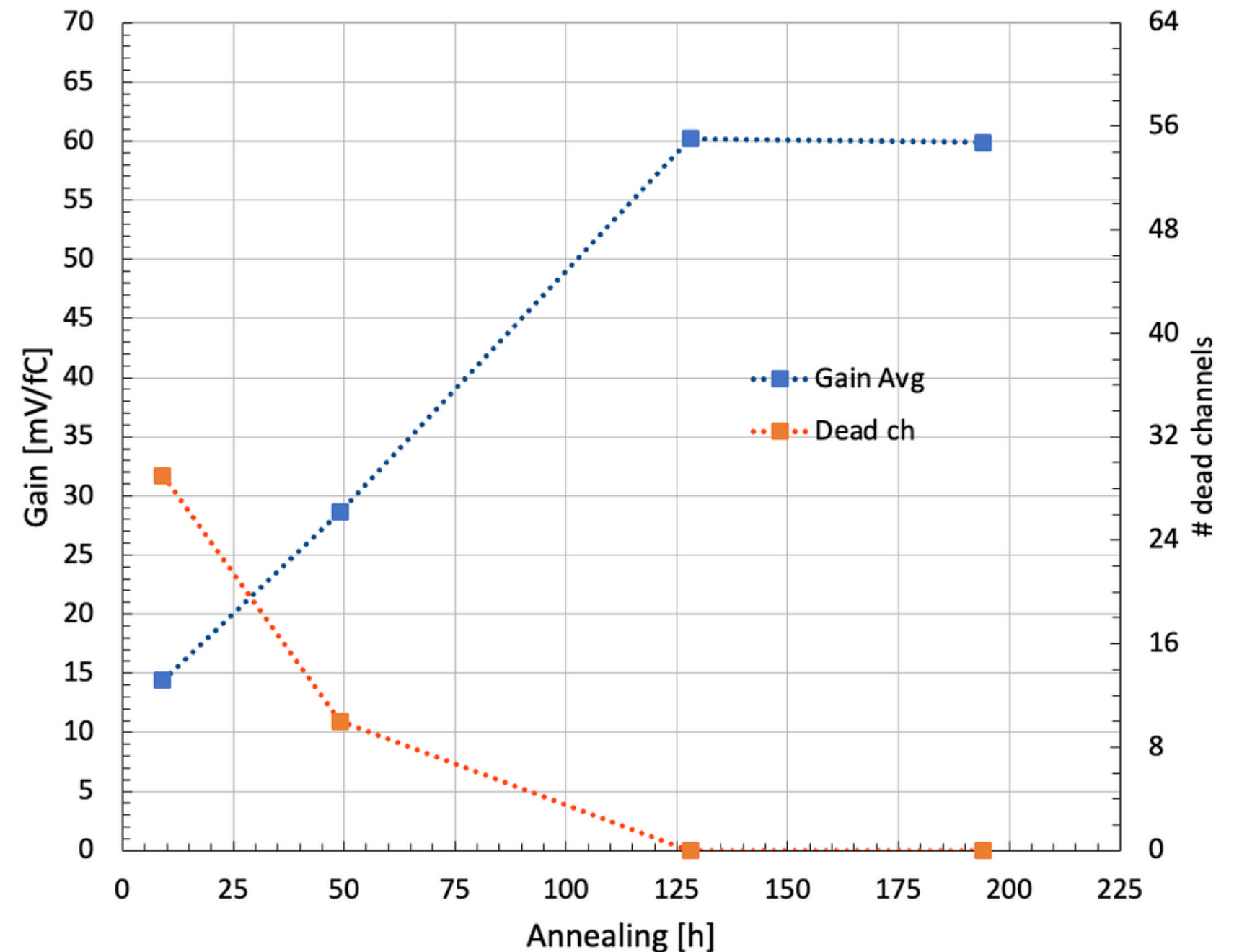
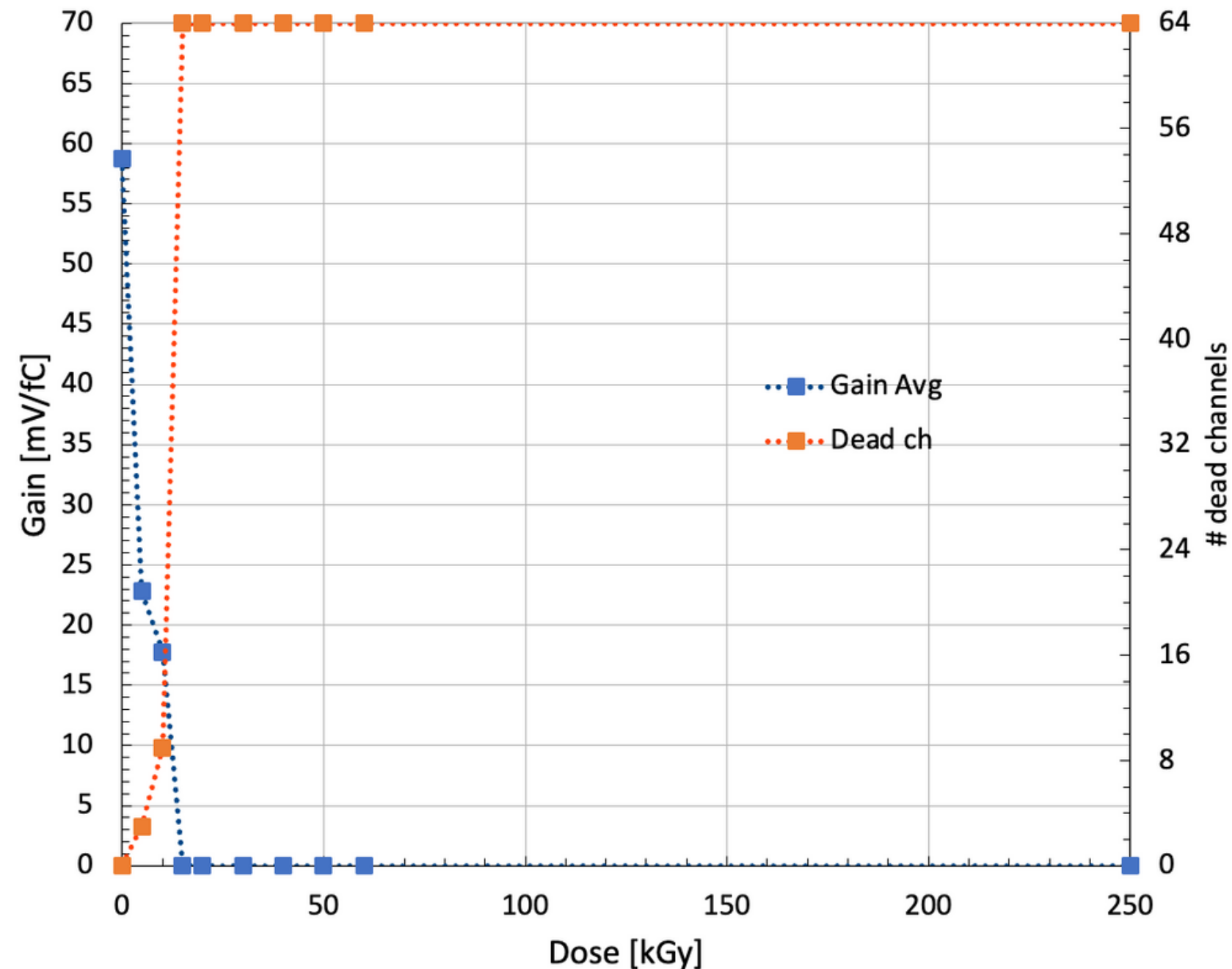
Annealing:

- from 0 to 49 hours at 15 °C
- from 49 to 121 hours at 100 °C

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Total Ionizing Dose tests

GAIN



DEAD CHANNEL --> no answer to Test Pulse

Likely due to a switch sensitivity to the leakage current

CONCLUSION

ToASt:

- A 64 channels ASIC
- Designed for the readout of the silicon strip detectors of the PANDA MicroVertex Detector

Test:

- Performances of Gain and Noise are as expected
- Tested with detector under preliminary beam test --> results under analysis
- Test for Total Ionizing Dose is not fully satisfying --> improvement required

Future works:

- Beam test data analysis
- Next version of ToASt

THANKS FOR THE ATTENTION

BACKUP SLIDES

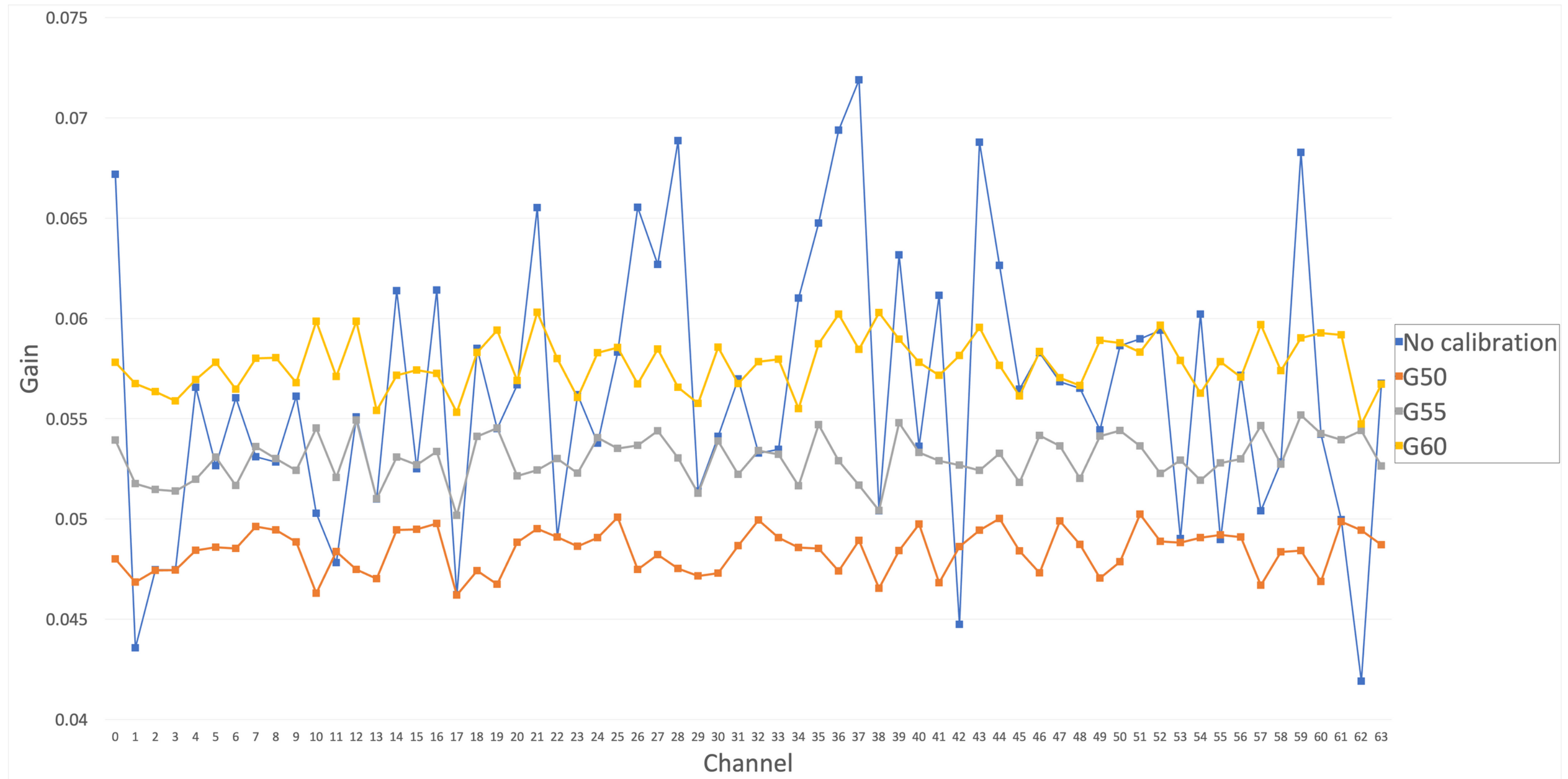
Measurement – gain calibration procedure

Calibration procedure:

- For each channel, measure the transfer curve for each channel ToT Ibias DAC value
- Select a reference gain
- For each channel, select the DAC value providing the gain closest to the reference
- For each channel, measure the offset of the ToT
- Select a reference offset
- For each channel, select the DAC value providing the offset closest to the reference

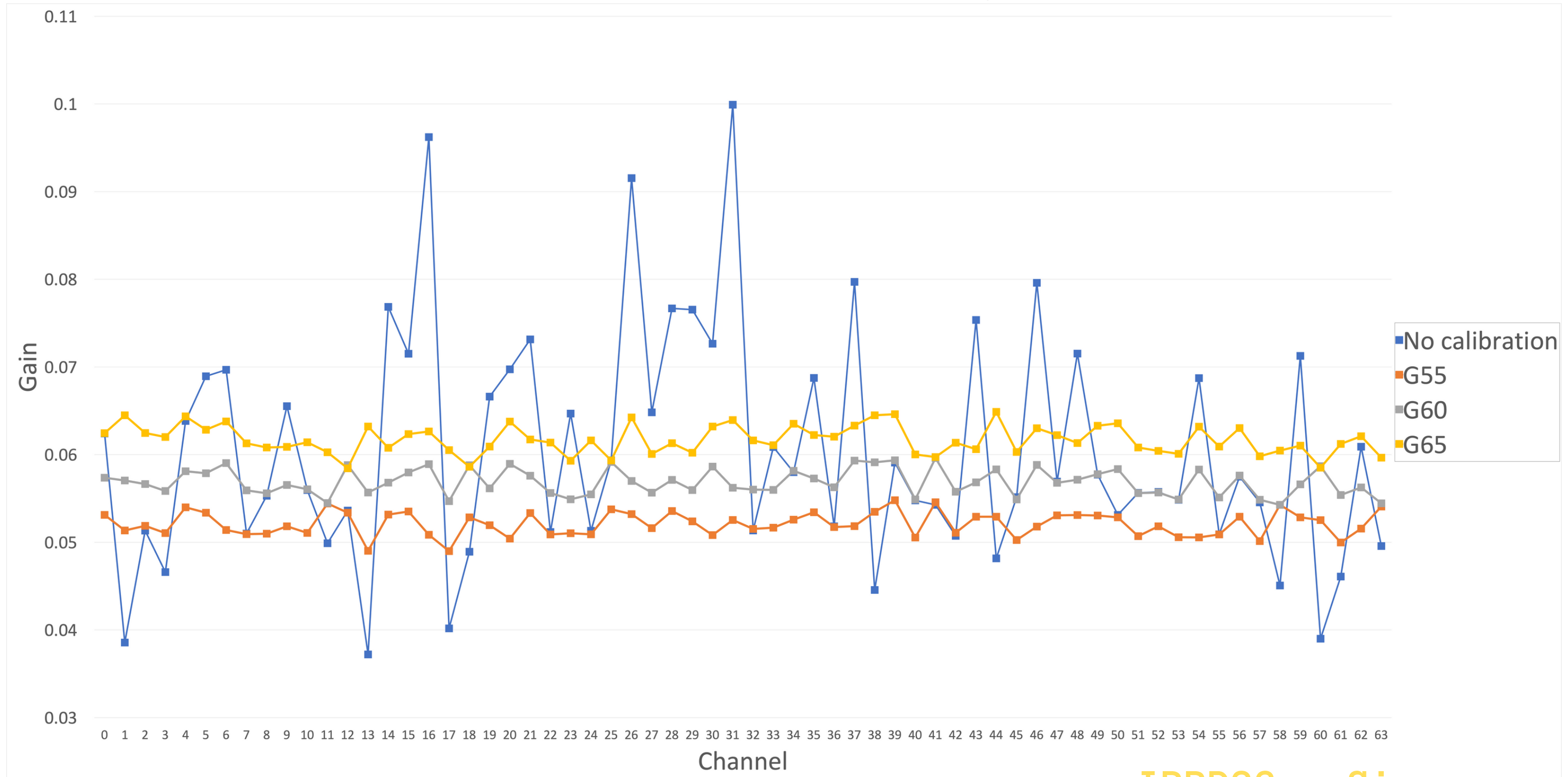
Measurement – gain calibration

Board without sensor – ptype



Measurement – gain calibration

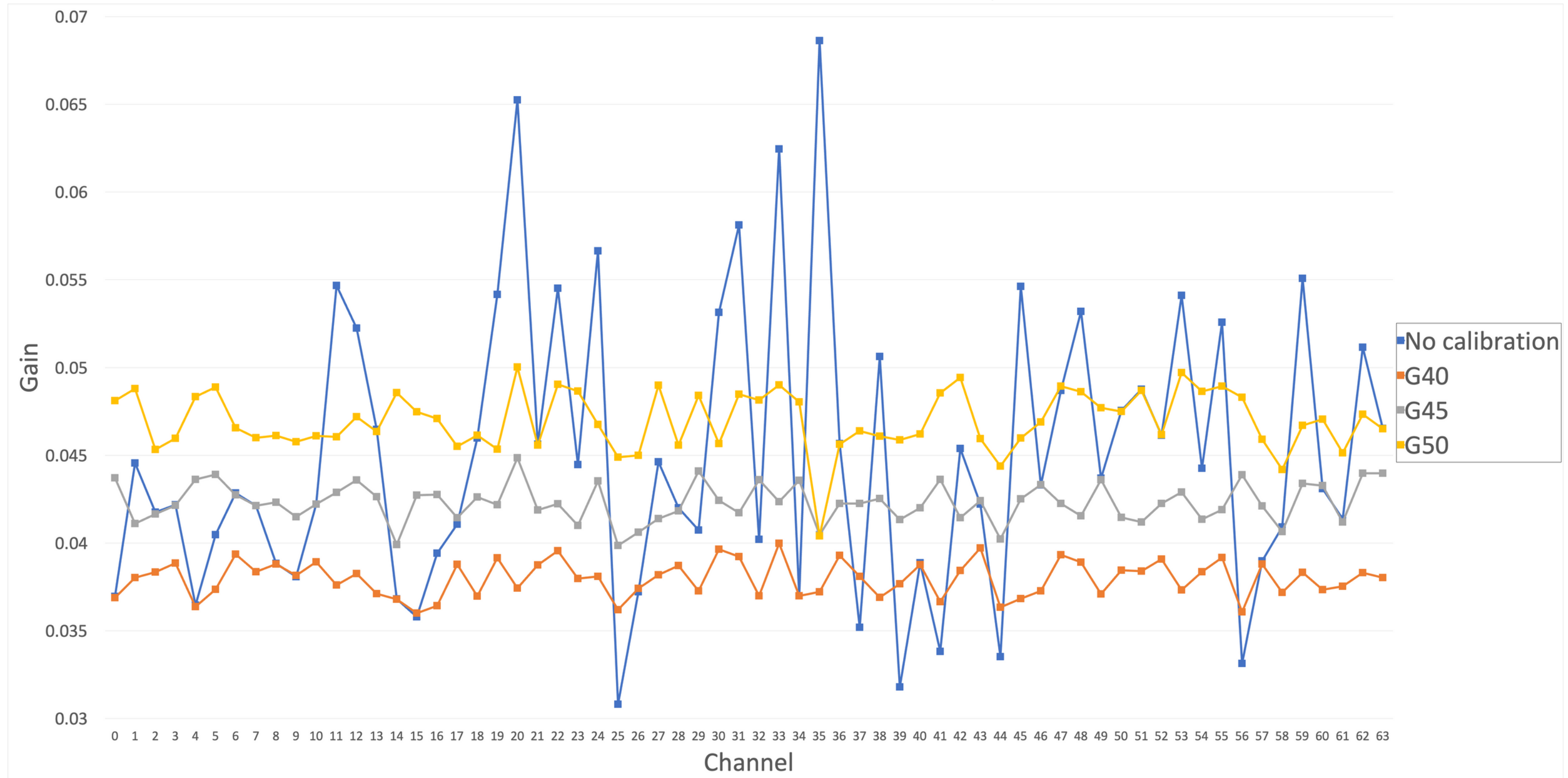
Board without sensor – ntype



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Measurement – gain calibration

Board with S3 sensor – ntype

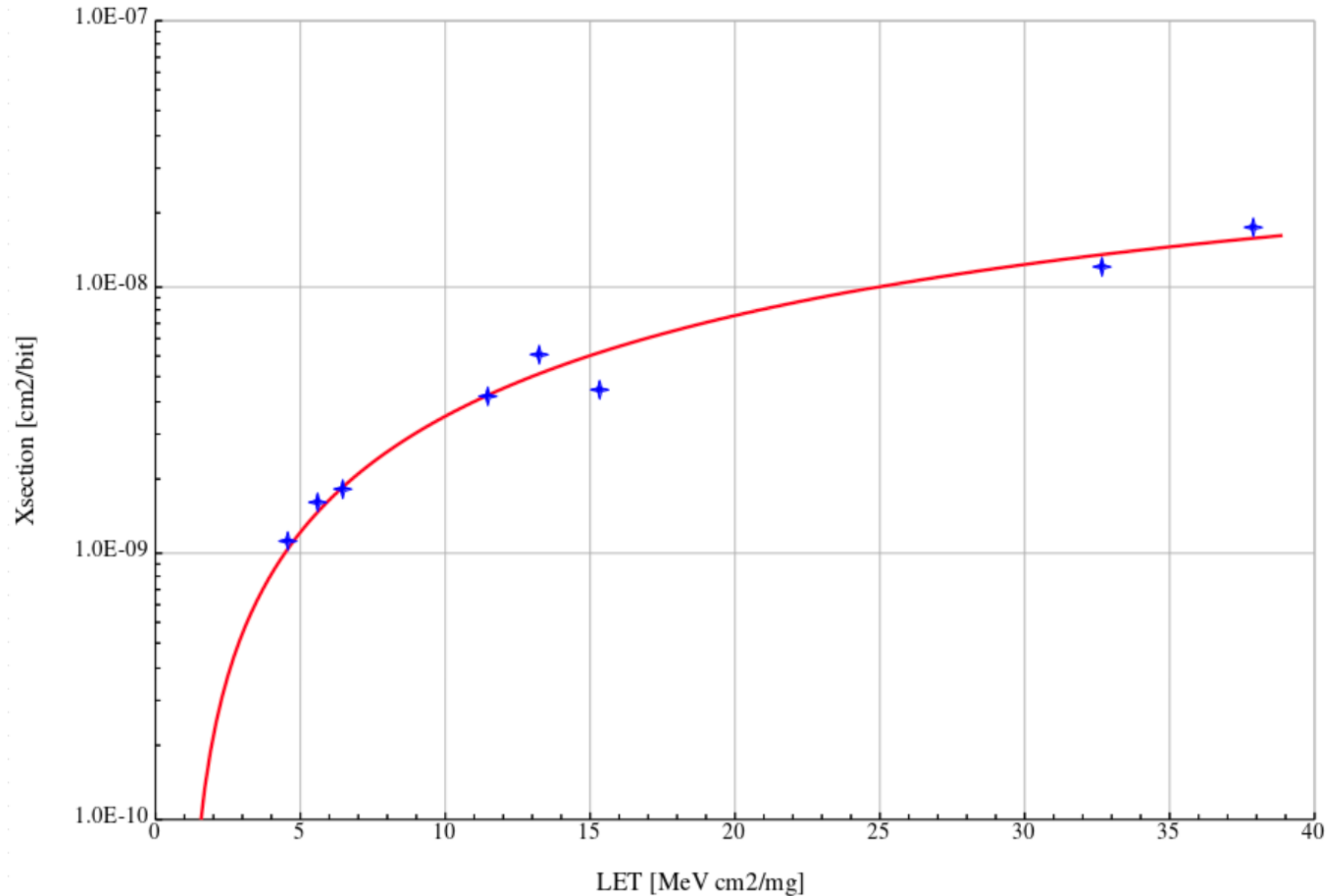


SSDs readout requirements

Specification	Min	Max	Unit
Channels per chip	64		
ToA (pk-pk)		6.25	ns
ToA (r.m.s.)		1.8	ns
Charge resolution	8		bits
Input charge	1	40	fC
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Noise		1500	e ⁻
Preamp peaking time	50	≥ 100	ns
Reference clock		160	MHz
Power consumption		256	mW
Radiation tolerance		20	kGy
Chip dimensions	4.5 × 3.5		mm ²
Pads position	On two sides only		

Single Event Upset

- Test at INFN LNL SIRAD facility
- Ion fluence $5 \cdot 10^7$ per ion
- Estimated cross section for 200 MeV protons : $3 \times 10^{(-15)}$ cm²
- Hadron flux 5×10^6 hadrons/(cm²×s) → $9.3 \times 10^{(-2)}$ errors/(h chip)
- Only 1→0 errors observed – triplication error found in the Verilog code



ToASt channel schematic

