ECFA
European Committee for Future Accelerators
ECFA Detector R&D Roadmap

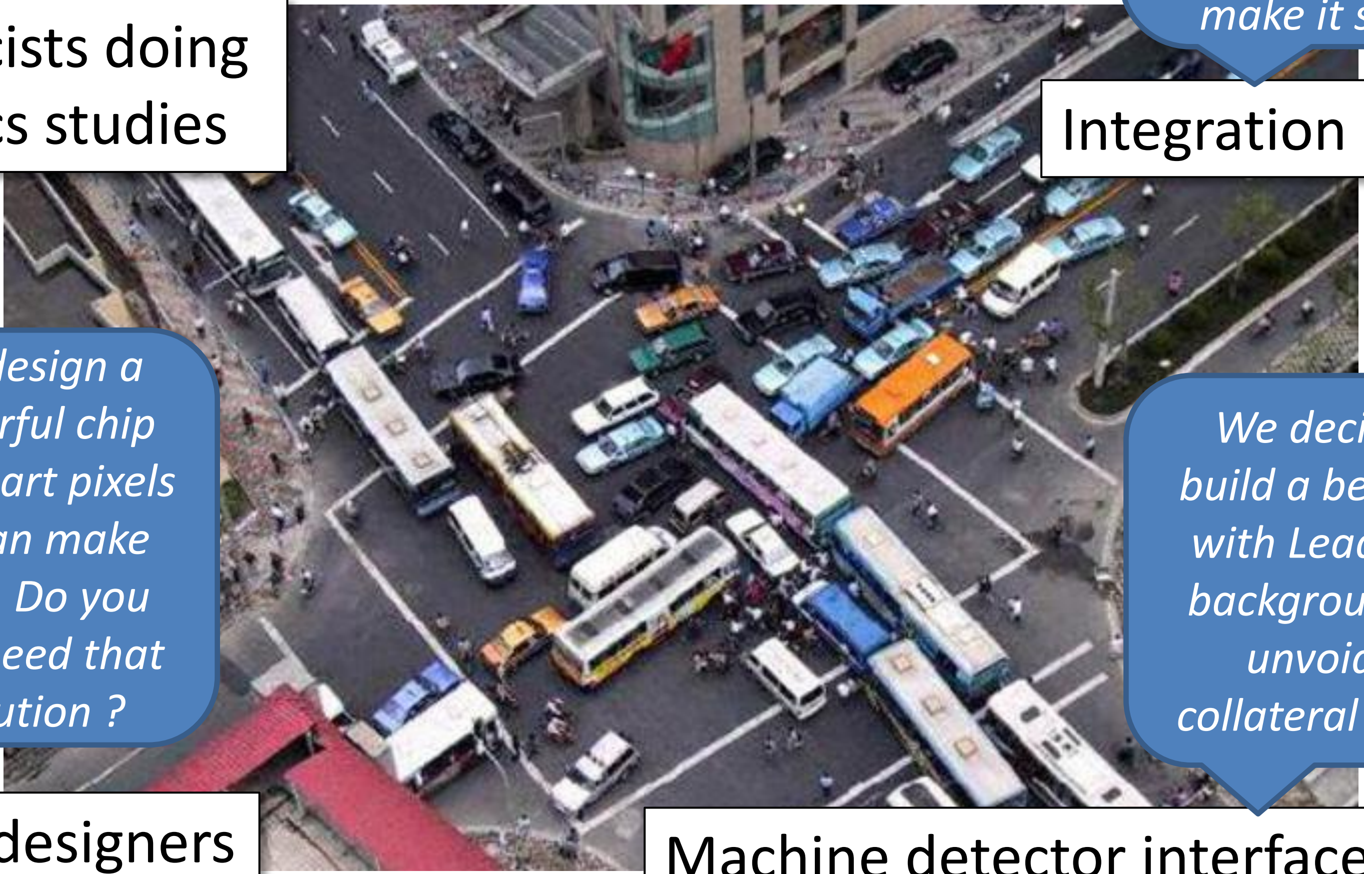
ECFA PED study on future e+e- EW/Higgs/Top/Flavour factories
ECFA WG3: Topical workshop on tracking and vertexing

Conceptual designs and R&D challenges for vertex detectors and silicon trackers

“how the detectors in the concepts would fit within the constraints and deliver the needed performance, and what are the R&D challenges towards making the concept a reality”

⇨ Not a technology R&D overview

A matter of priority ?



I want the ideal detector, just make it !

Physicists doing physics studies

Give me space and materials for my cables and mechanical supports. Can I add some concrete to make it stiffer ?

Integration experts

I can design a wonderful chip with smart pixels that can make coffee. Do you really need that resolution ?

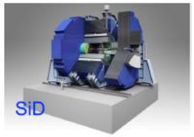
Chip designers

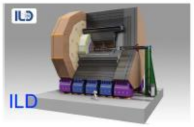
We decided to build a beam pipe with Lead. Beam background is an unvoidable collateral damage

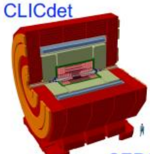
Machine detector interface experts

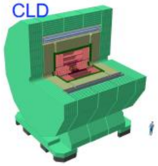
Tracking/vertexing detectors in future e^+e^- colliders

Collider	ILC		CLIC	FCCee			CEPC	
Bunch separation (ns)	330/550		0.5	20/990/3000			25/680	
Power Pulsing	yes		yes	no			no	
beamstrahlung	high		high	low			low	
Detector concept	SiD	ILC	CLICdet	CLD	IDEA	Lar	Baseline	IDEA
B Field (T)	5	3.5	4	2	2	2	3	2
Vertex	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel
Vertex Rmin (mm)	16	16	31	12	12	12	16	16
Tracker	Si-strips	TPC	Si-Pixel	Si-Pixel	DC/Si-strips	DC/Si-strips or Si-Pixels	TPC or Strips	DC/Si-strips
Tracker Rmax (m)	1.25	1.8	1.5	2.2	2.0	2.0	1.8	2.1
Disks layers	4 + 4	2 + 5	6 + 7	3 + 7	3 (150 mrad)		2+6	

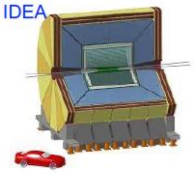


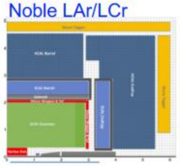


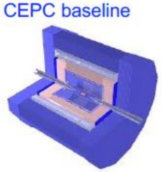


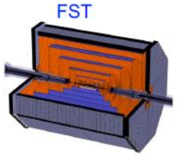


(From D. Dannheim)



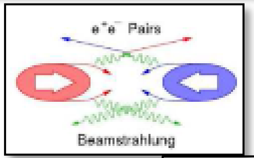




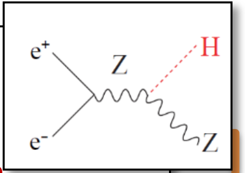


Large similarities between the concepts but also significant differences

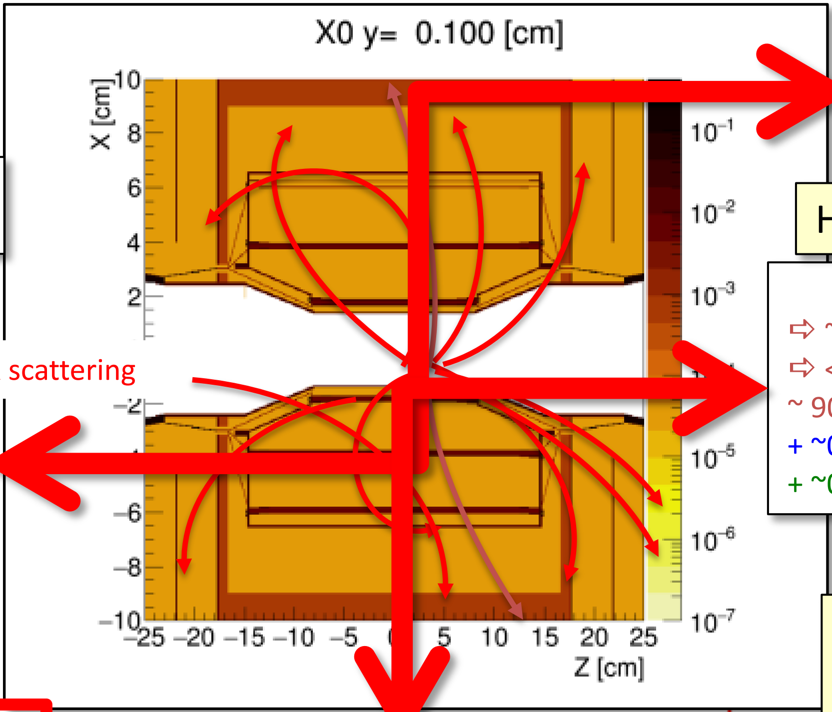
Vertex detector requirements



Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks
- ⇨ Vertex/Jet charge determination



Beam background (~ 5 hits/BX/cm² on layer 0, ILC)



Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Time resolution
O(1 µs) (O(1 ns for CLIC)

Power consumption
~< 50mW/cm²

Fast read-out & low Power Architectures (~ 20 mW/cm²)

Cooling
Stiffness / Alignment

Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17 um
- ⇨ (σ_{sp} ~3 um)

High granularity

Material Budget
- ⇨ ~ 0.1-0.2 % X_0 / layer
- ⇨ < 1% X_0 for the whole VTX
- ~ 900 µm Si
- + ~0.14% X_0 for the beam pipe (ILC)
- + ~0.3 % X_0 for the beam pipe (FCC)

Low material detectors & supports structures

$$\sigma_{d_0} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

$a \simeq 5\,\mu m$; $b\sim 15\ \mu m.GeV$ FCCee

$b\sim 10\ \mu m.GeV$ ILC

Power pulsing (ILC) vs continuous beam (FCCee)

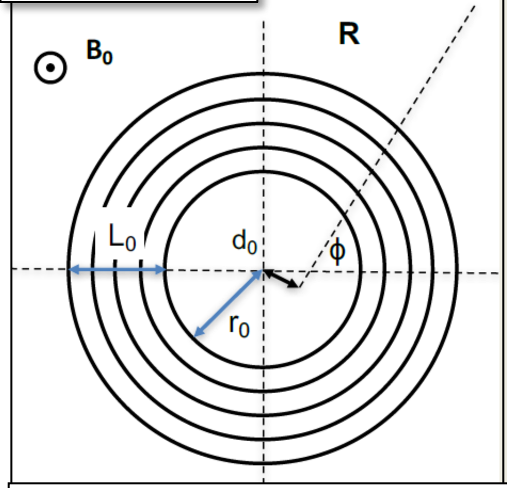
Challenge:

⇨Keep excellent spatial resolution, low material budget, moderate Power consumption and push towards better time resolution (BX)

Tracker requirements

- Material budget vs intrinsic resolution
  - ✓ Typically σ_{sp} ~5-10 μm/layer ; material ~1-2% X_0/layer ; Power ~< 100 mW/cm^2
  - ✓ Low momentum vs high momentum

Level arm !



Often, the "canonical" requirement is expressed as

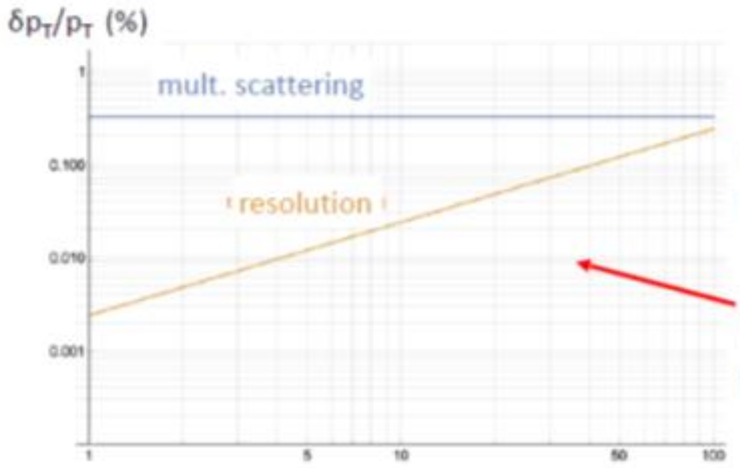
$$\sigma_{p_T}/p_T^2 \simeq 2\times 10^{-5}\,\mathrm{GeV}^{-1}$$

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

$$\frac{\Delta p_T}{p_T}\Big|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV}/c}{0.3\beta B_0 L_0}\sqrt{\frac{d_{tot}}{X_0 \sin\theta}} \qquad \frac{\Delta p_T}{p_T}\Big|_{res.} \approx \frac{12\,\sigma_{r\phi}\,p_T}{0.3\,B_0 L_0^2}\sqrt{\frac{5}{N+5}}$$

$$d_{tot}/X_0 = (N+1)d/X_0$$

d = layer thickness, N = # layers



Paolo Giacomelli (Annecy 2021)

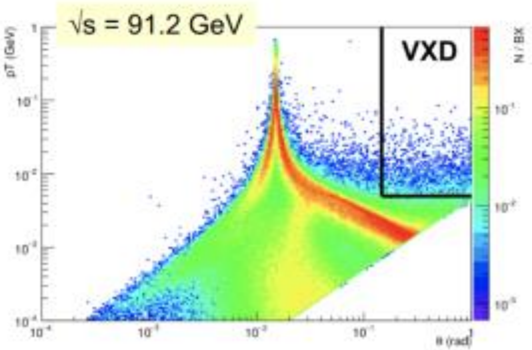
Here illustrated for the CLD detector at 90° :
Total material budget = 11% of X_0

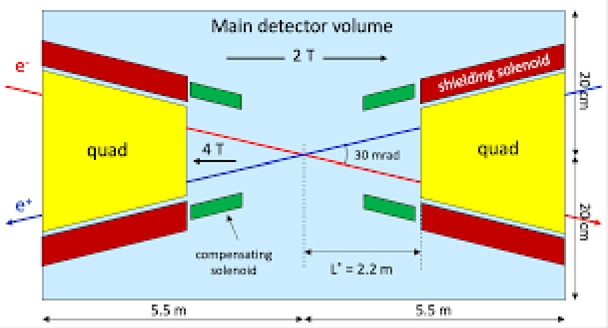
From analytic expressions for track parameter resolutions.

m.s. term dominates for pT ~< 100 GeV/c

Vertex/tracking detector comments

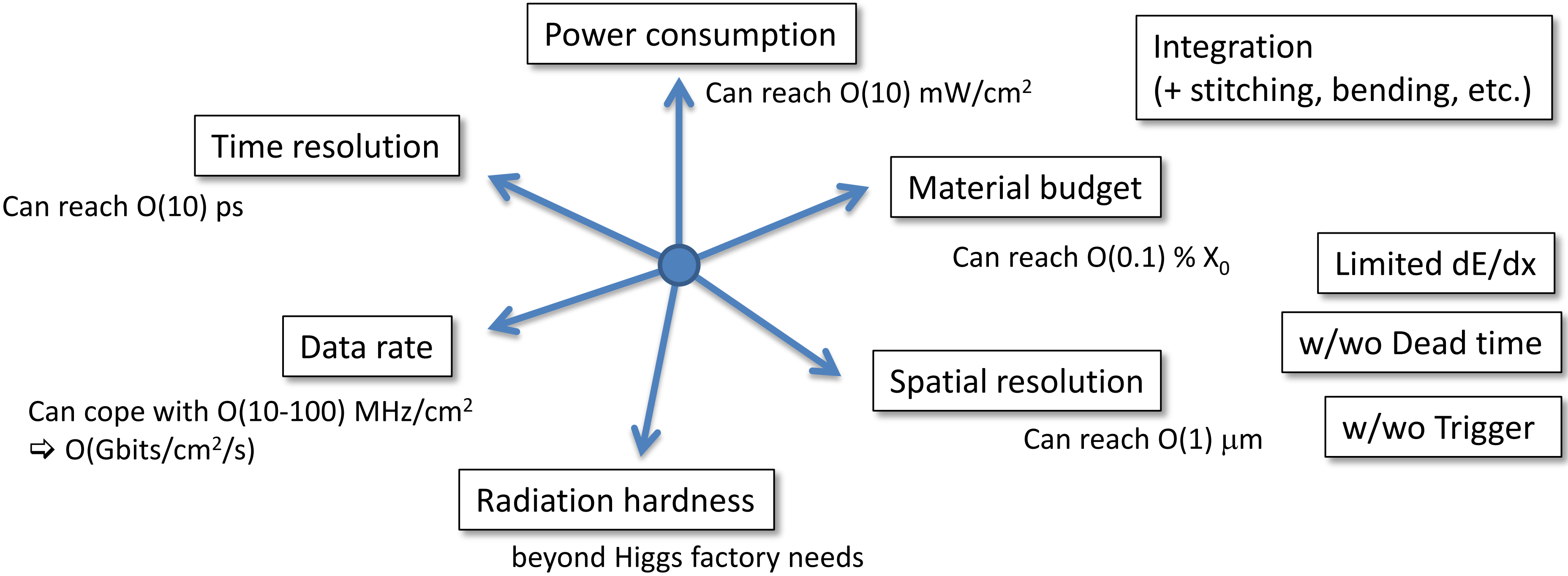
- Particle ID has to be included in the tracker concept
  - ✓ dEdx and/or dNdx and/or fast timing
- Inner and outer radius are key factors
- Forward acceptance (e.g. asymmetry measurements)
  - ✓ Limited by MDI constraints, beam pipe, luminosity measurements, etc.
    - 30 mrad acceptance (FCCee)
- B-field
  - ✓ Limited to 2 T in circular machine (@ Z-pole)
- Beam structure
  - ✓ Power pulsing only for linears
- Background
  - ✓ Beamstrahlung (incoherent e+e- pairs)
    - Occupancy driver for linears
    - Less severe for circular (⇨Rmin reduction ~10mm))
  - ✓ Synchrotron radiation (mainly circulars)
    - Possible shielding (increase beampipe material budget)
- Geometry
  - ✓ Probably 5-6 layers VTX (R < 60 mm)
    - Robustness (standalone tracking)
    - low momentum tracking
    - Track seeding @ different radii
    - e.g. FIPs, highly ionizing particles, LLPs, etc.
  - ✓ « long barrel » (sticking the first measurement point to the beam pipe)
    - Minimize « Rmin » w.r.t. to « short barrel+disk » approach.
- Trigger-less





Silicon detectors

Silicon tracking detector figure of merit



Power consumption

Can reach O(10) mW/cm^2

Integration
(+ stitching, bending, etc.)

Time resolution

Can reach O(10) ps

Material budget

Can reach O(0.1) % X_0

Limited dE/dx

w/wo Dead time

w/wo Trigger

Data rate

Can cope with O(10-100) MHz/cm^2
⇨ O(Gbits/cm^2/s)

Spatial resolution

Can reach O(1) µm

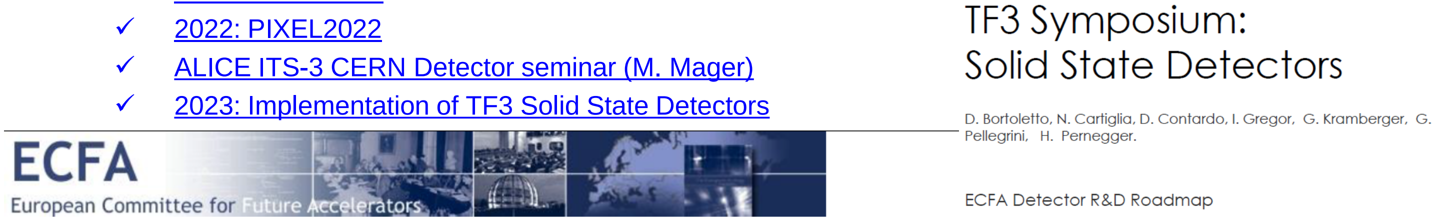
Radiation hardness

beyond Higgs factory needs

- Ultimate performances look like the ideal tracking or vertexing detector. However
  - ✓ Very precise ⇨ not that fast
  - ✓ Very fast ⇨ large pitch and/or large Power
- Need a **hierarchy** or **specialized** layers
  - ✓ Governed by physics requirements and experimental conditions
  - ✓ Fast timing and small granularity/low material budget are very antagonist
  - ✓ R&D needed to improve the parameter space

Silicon detectors landscape

- A very active area. e.g. see
  - ✓ 2021: ECFA Detector R&D Roadmap Symposium of Task Force 3 Solid State Detectors
  - ✓ 2022: VCI 16th Vienna conference
  - ✓ 2022: 15th Pisa Meeting on Advanced Detectors
  - ✓ 2022: AIDAInnova Kick-off meeting
  - ✓ 2022: Vertex2022
  - ✓ 2022: PIXEL2022
  - ✓ ALICE ITS-3 CERN Detector seminar (M. Mager)
  - ✓ 2023: Implementation of TF3 Solid State Detectors



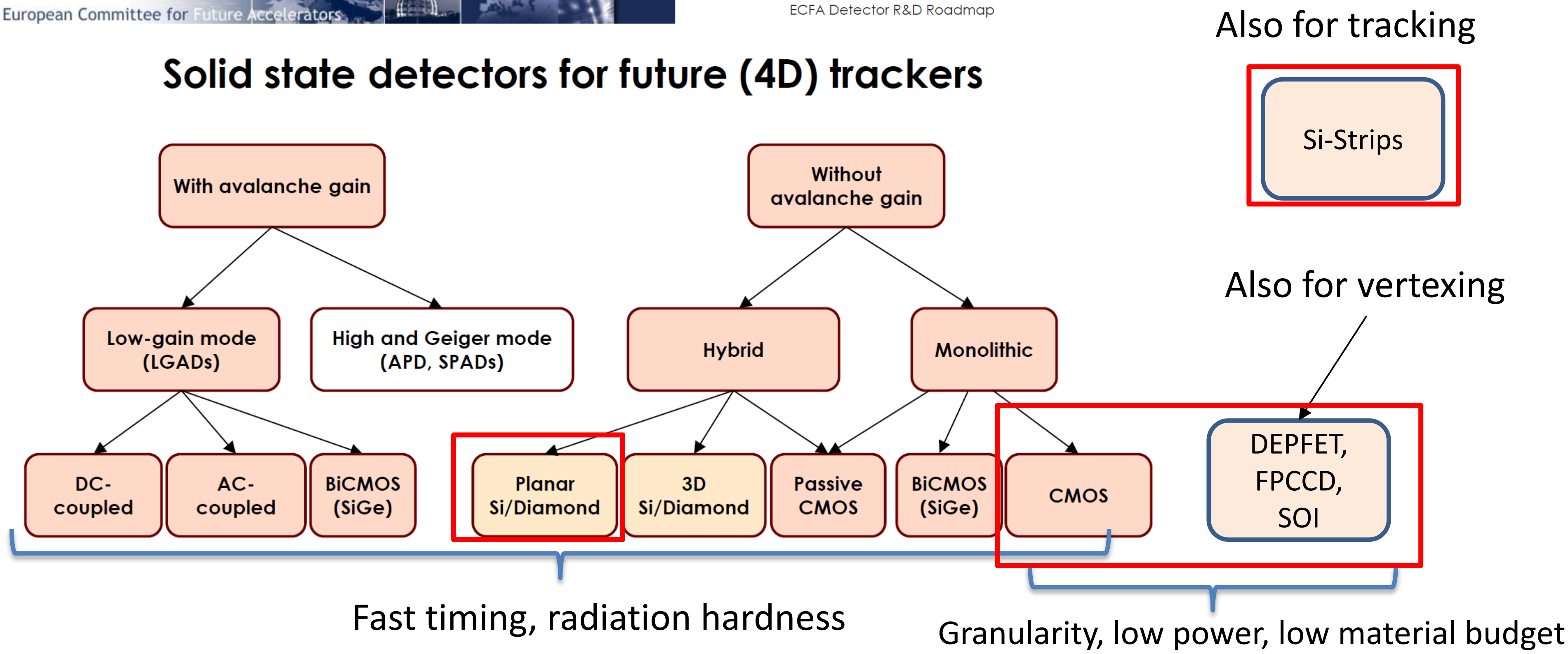
ECFA

European Committee for Future Accelerators

TF3 Symposium:
Solid State Detectors

D. Bortoletto, N. Cartiglia, D. Contardo, I. Gregor, G. Kramberger, G. Pellegrini, H. Pernegger.

ECFA Detector R&D Roadmap



Solid state detectors for future (4D) trackers

With avalanche gain

Low-gain mode (LGADs)

DC-coupled

AC-coupled

BiCMOS (SiGe)

High and Geiger mode (APD, SPADs)

Without avalanche gain

Hybrid

Planar Si/Diamond

3D Si/Diamond

Passive CMOS

Monolithic

BiCMOS (SiGe)

CMOS

Also for tracking

Si-Strips

Also for vertexing

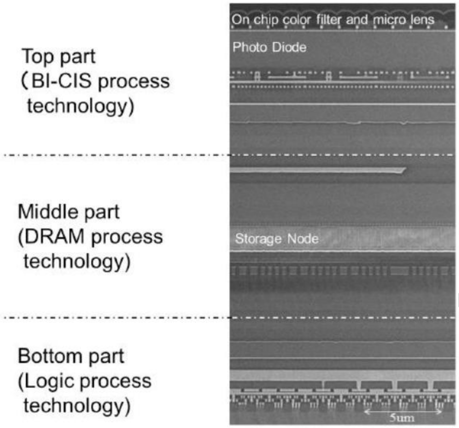
DEPFET, FPCCD, SOI

Fast timing, radiation hardness

Granularity, low power, low material budget

Plenty of R&Ds to follow carefully…

Wafer stacking in CMOS (quoted by W. Snoeys)

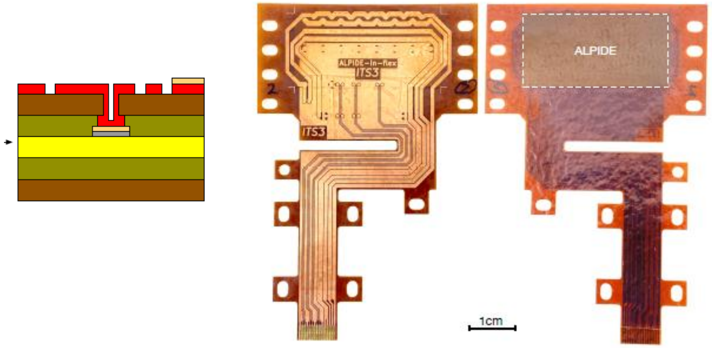


Example: SONY

Several wafers stacked with different technologies to make a full sensor
⇨ Starts to be available in imaging tech.

MAPS Foil: Embedded MAPS inside polymide flexible printed circuits

⇨ Provides electrical connection, protection, bending, 0.1%X_0

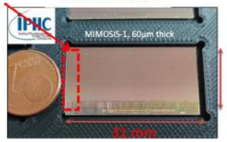


arXiv:2205.12669v1 [physics.ins-det] 2022

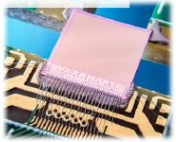
Huge panel of R&D and projects in CMOS

- ✓ Different technologies (TJ180 nm, TPSCo 65nm, LF 110 nm, etc.)

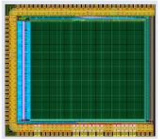
MIMOSIS-1
180 nm CMOS



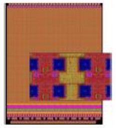
CLICTD
180 nm CMOS



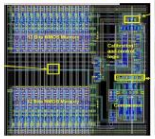
JadePix2
180 nm HV-CMOS



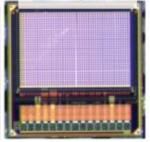
ARCADIA MD1
110 nm CMOS



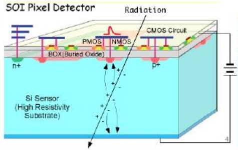
Chronopix
90 nm CMOS

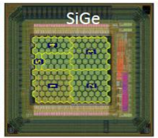


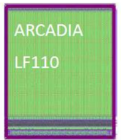
CE-65
65 nm CMOS



Many others: LF150, LF110, SOI, XFAB, SiGe BiCMOS, with and without gain layer, TJ180 …



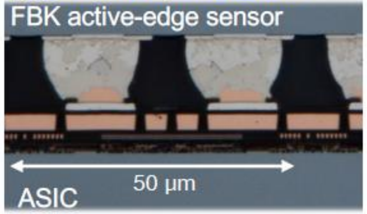




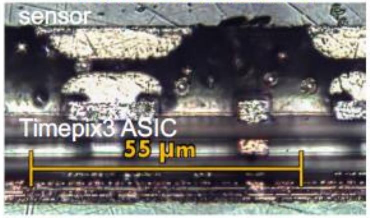
Hybrid R&D

- 25 um bump bonding
- Anisotropic Conductive Film

25 µm bump bonding @ IZM

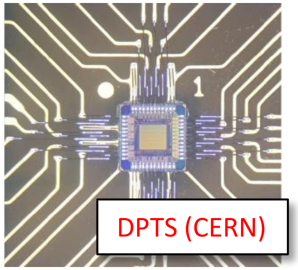


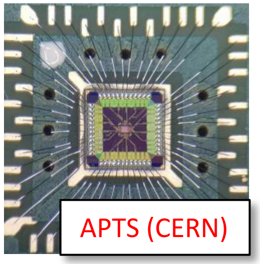
55 µm ACF interconnect



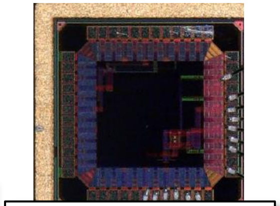
An example of R&D: TPSCo 65 nm CMOS technology

- 65 nm feature size technology
  - ✓ Main driver: CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades
    - Privileged relation between CERN with the foundry
- Added values
  - ✓ Larger wafers (⇨ 30 cm)
  - ✓ More functionalities inside the pixel
  - ✓ Keeps pixel dimensions small ⇨ spatial res.
  - ✓ Potentially faster read-out
  - ✓ Lower Power consumption
  - ✓ Synergy with Higgs factories requirements
- First submission: MLR1 (2020)
  - ✓ Validated the technology for HEP
- 2nd Submission ER1 (2022-23)
  - ✓ Dedicated to ITS3 (MOSS/MOST; stitching)


DPTS (CERN)


APTS (CERN)

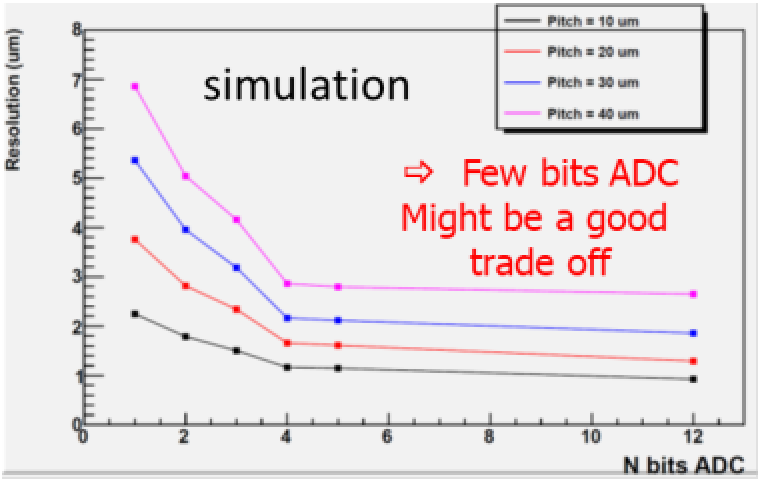

CE-65 (IPHC)


TANGERINE (DESY)

Challenge 1: the spatial resolution

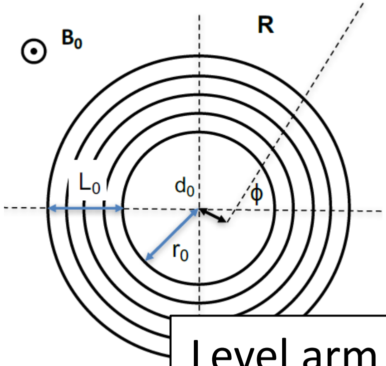
Spatial resolution in Higgs factories

- Typical targets:
  - ✓ σ_{sp}~3 μm for the vertex layers
  - ✓ σ_{sp}~5-10 μm for the outer tracker layers
- Resolution in each layer depends on
  - ✓ Pitch
    - In conflict with the functionnalities inside the pixel
    - Favored by small feature size technology
  - ✓ Charge deposition
    - Sensitive layer thickness
  - ✓ Charge sharing (SNR vs resolution)
    - Depletion:
    - Staggered pixels
  - ✓ Charge encoding
    - Binary output / ADC / Tot / etc.



⇨ Few bits ADC Might be a good trade off

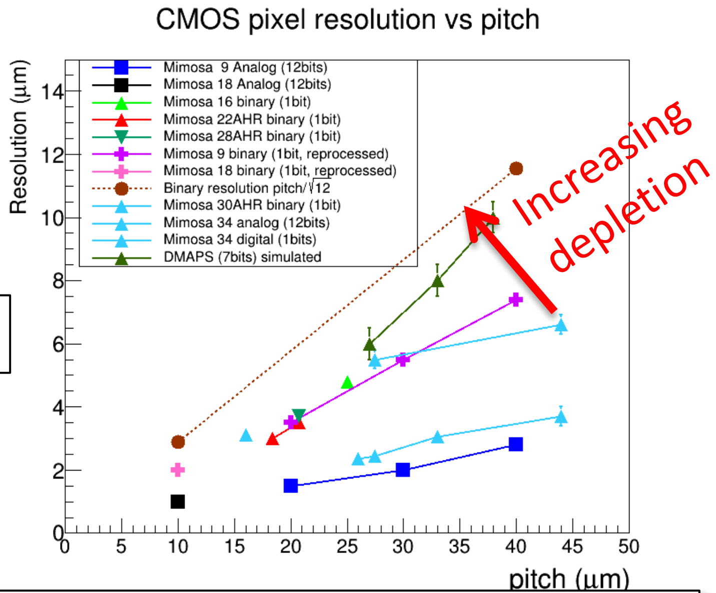
$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.\sin^{3/2}\theta}\right)^2$$



Level arm !

$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0\sin\theta}}\sqrt{1+\frac{1}{2}\left(\frac{r_0}{L_0}\right)+\frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

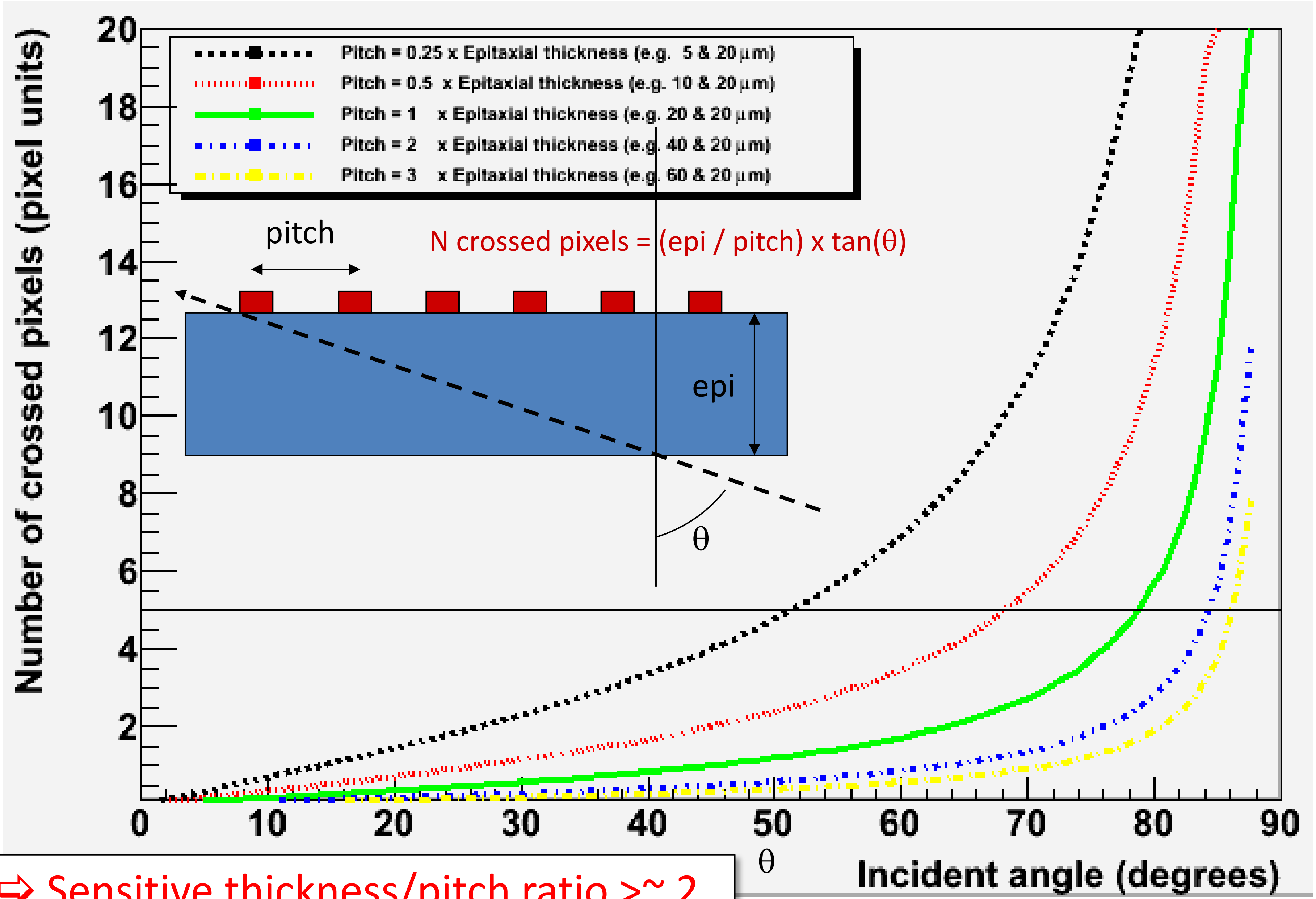

CMOS pixel resolution vs pitch

Increasing depletion

⇨ σ_{sp} ~ 3 μm ⇦⇨ pitch ~ 15-20 μm

(assuming binary output, ~20 μm epi.thickness & large depletion in 180nm tech.)

Elongated clusters: low pT tagging

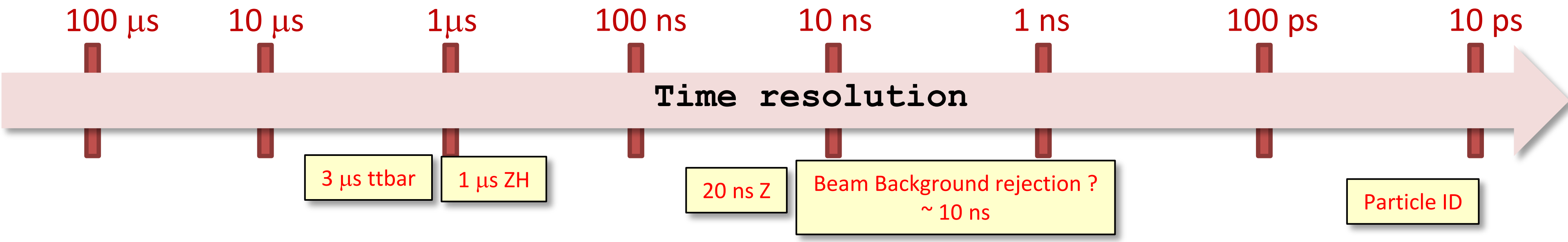


N crossed pixels = (epi / pitch) x tan(θ)

⇨ Sensitive thickness/pitch ratio >~ 2

Challenge 2: time resolution

Timing & 4-D tracking



100 μs | 10 μs | 1μs | 100 ns | 10 ns | 1 ns | 100 ps | 10 ps

Time resolution

3 μs ttbar

1 μs ZH

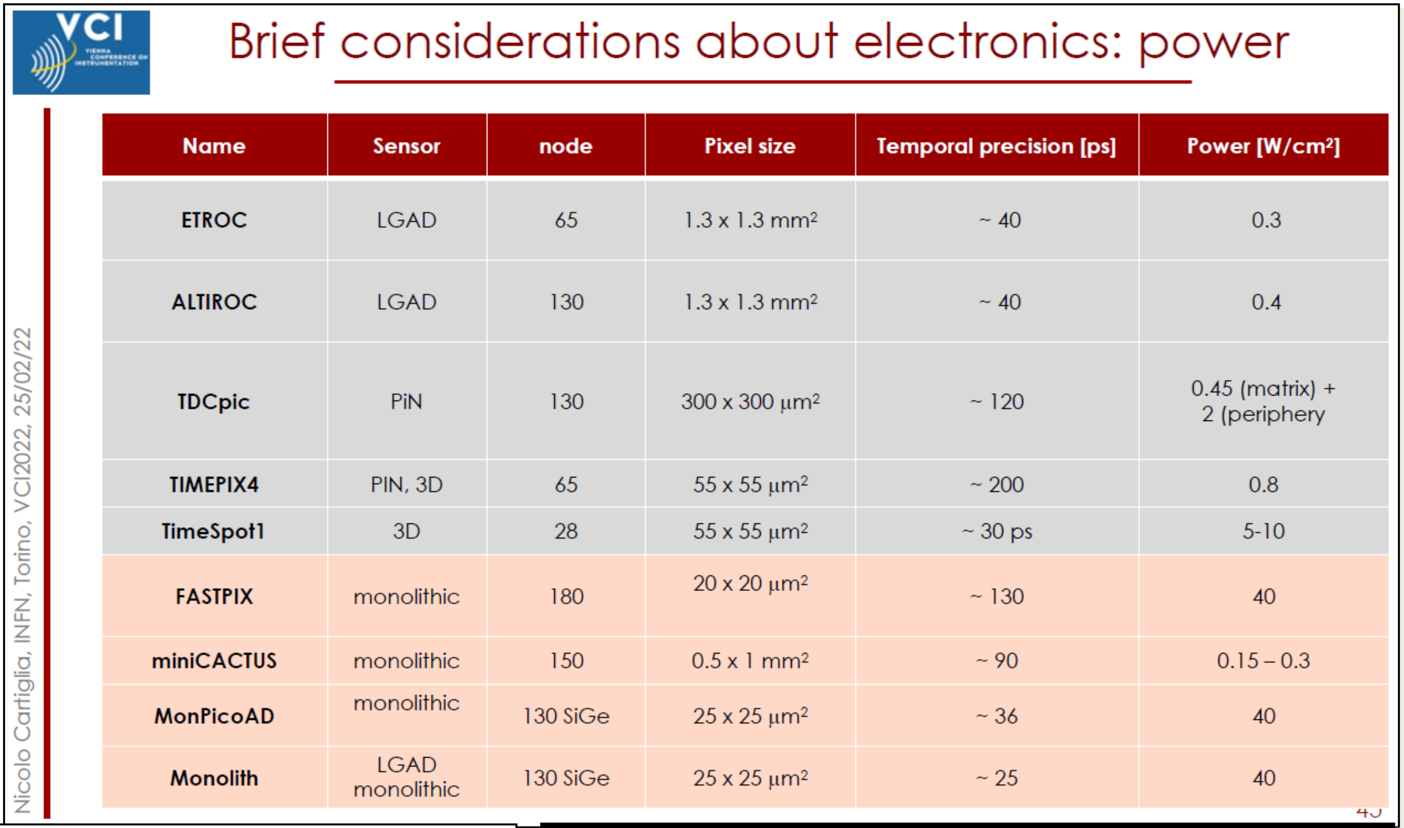
20 ns Z

Beam Background rejection ?
~ 10 ns

Particle ID

- Time resolution Δt
  - ✓ Bunch separation (3 μs / 1 μs / 20 ns @ FCCee)
  - ✓ Background rejection ? (1-10 ns range)
  - ✓ Particle ID (10-100 ps)
- Usual drawbacks to go faster
  - ✓ Power consumption
  - ✓ Active Cooling & geometrical acceptance due to services
  - ✓ In pixel circuitry ⇨ larger pixels (or multipixels)
  - ✓ Fill factor, dead time
  - ✓ PID Restricted to low momentum particles (~< few GeV/c)
- Still
  - ✓ Forward region not covered by a central gazeous detector
  - ✓ Added value for intermediate radii (e.g. LLPs ?)

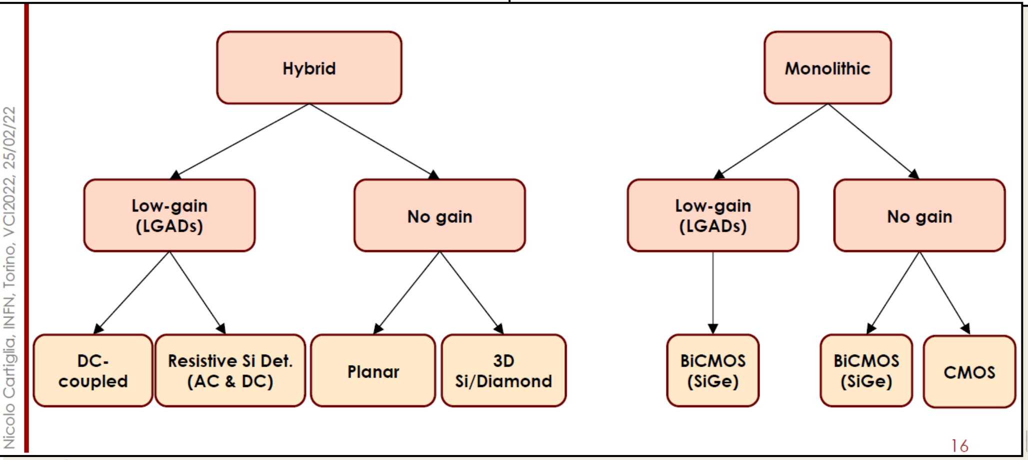
Power vs fast timing vs pixel size



Brief considerations about electronics: power

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm^2]
ETROC	LGAD	65	1.3 x 1.3 mm^2	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm^2	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm^2	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm^2	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm^2	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm^2	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm^2	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm^2	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm^2	~ 25	40

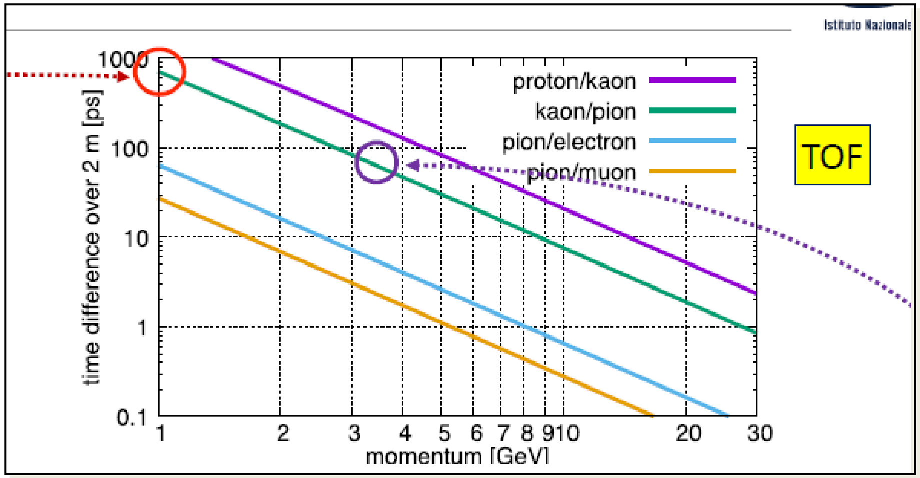
Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

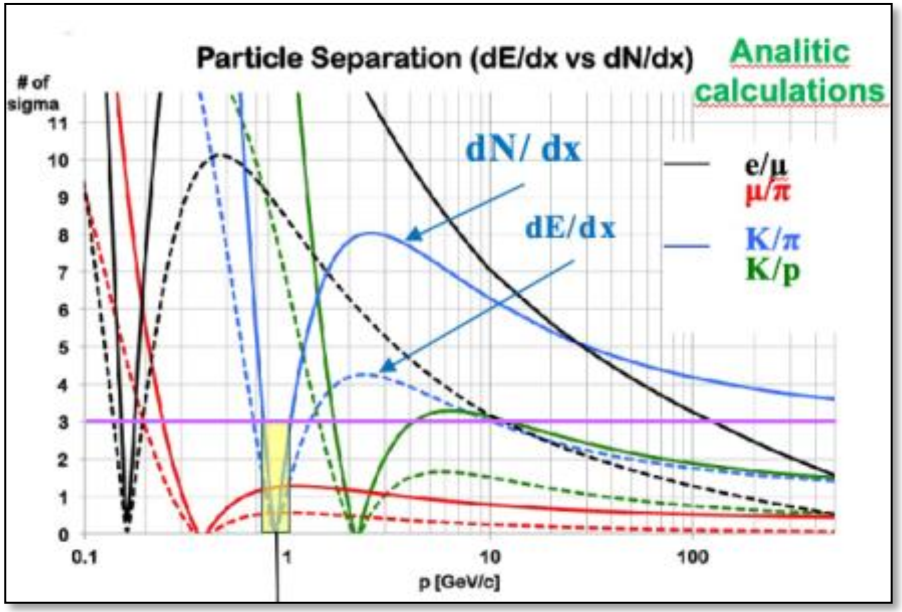


Price to pay: additionnal cooling system (addtionnal material)

Fast timing

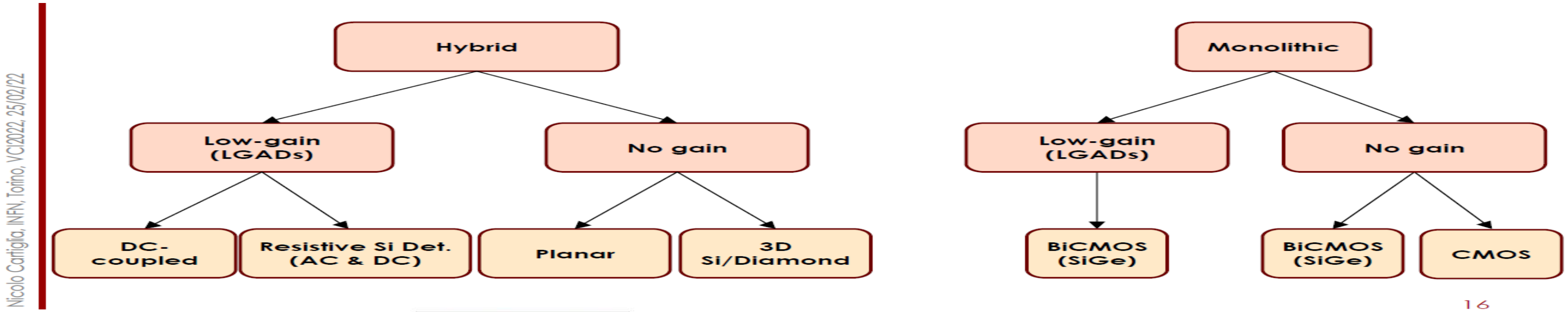
- Extremely active domain
  - ✓ Interest to push beyond 10 ps resolution
- PID not discussed here (covered by TF4)
  - ✓ dE/dX ; dN_{cl}/dx and timing for PID
  - ✓ Fast timing not proper to silicon (also scintillation, gazeous, Cerenkov)





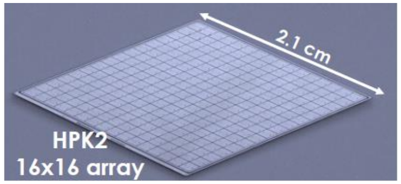
- Specialized layers
  - ✓ Doesn't compromise the other requirements (material budget and granularity)
    - Probably not in the most inner layers
  - ✓ Dedicated studies needed for design optimization

Timing Landscape in semi-conductor technologies

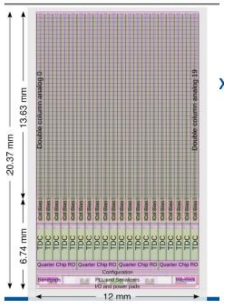

- Hybrid
  - Low-gain (LGADs)
    - DC-coupled
    - Resistive Si Det. (AC & DC)
  - No gain
    - Planar
    - 3D Si/Diamond
- Monolithic
  - Low-gain (LGADs)
    - BiCMOS (SiGe)
  - No gain
    - BiCMOS (SiGe)
    - CMOS

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

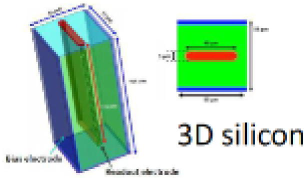
Low gain to minimize jitter



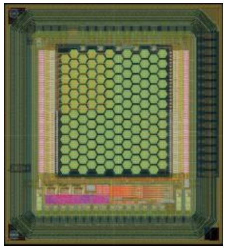
CMS & ATLAS
(LGAD DC coupled)



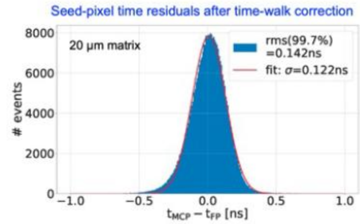
NA62 Gigatracker
(planar)



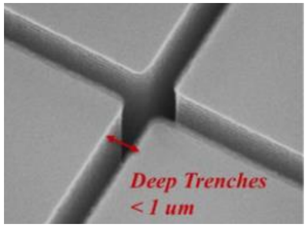
3D silicon



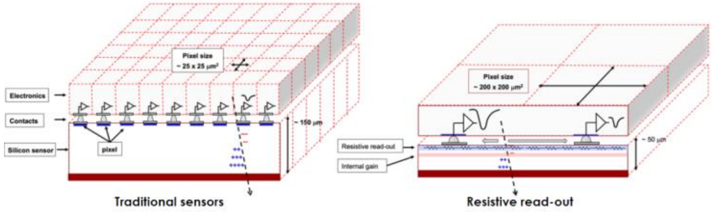
MonPicoAd
(BiCMOS)



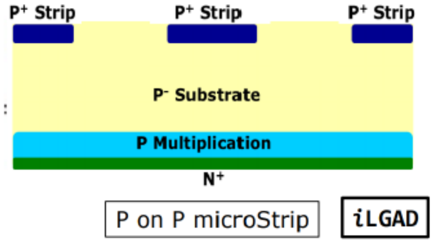
FastPix
(CMOS)



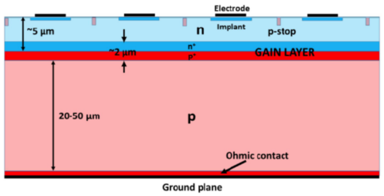
Trench Isolated-LGAD
(reduces no gain region)



Resistive read-out
AC-LGADS
(signal sharing)



Inverse ILGAD



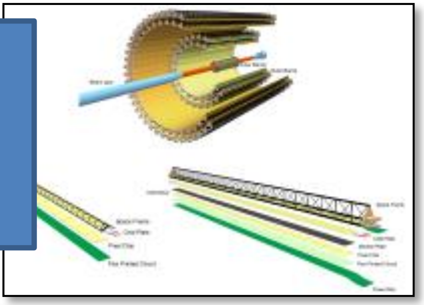
Deep Junction
DJ-LGAD

See e.g. ECFA-TF4 Time of flight technologies (R. Forty)

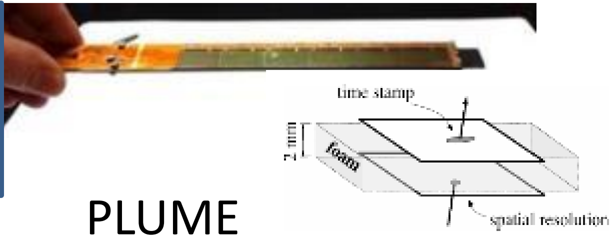
Challenge 3: material budget

Material budget: starting from the layers

Classical single sided layers (e.g. ALICE ITS-2)



Double sided layers



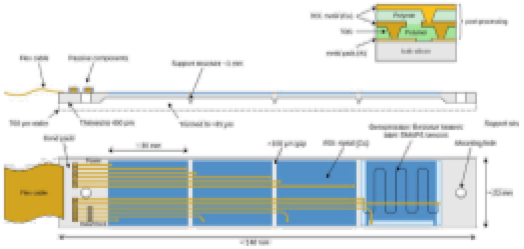
PLUME

(Bristol, DESY, IPHC)

Double sided ladders with minimized material budget 0.35% X_0 reached ⇨ ~0.3 X_0 doable (with air flow cooling)

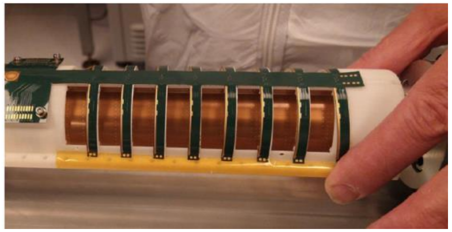
Self supported silicon (Belle-2 upgrade)

7.1x1.5 cm^2
Thickness (edge/center)
430/90 µm
Planarity ~17 µm



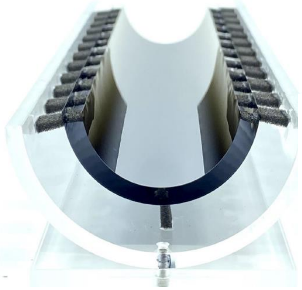
Pseudo stitching + bent sensors (superALPIDE)

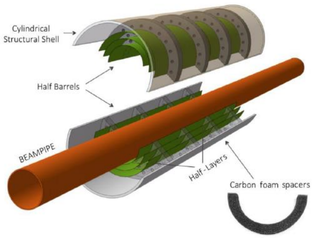
- 1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)



Stitching + bent sensors ALICE-ITS3

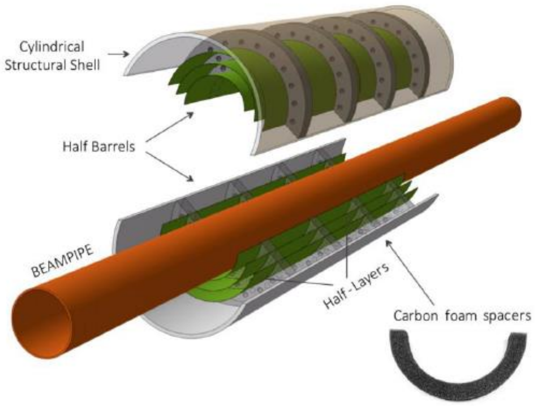
Layers 2+1

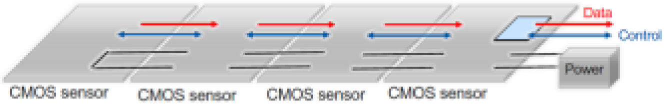


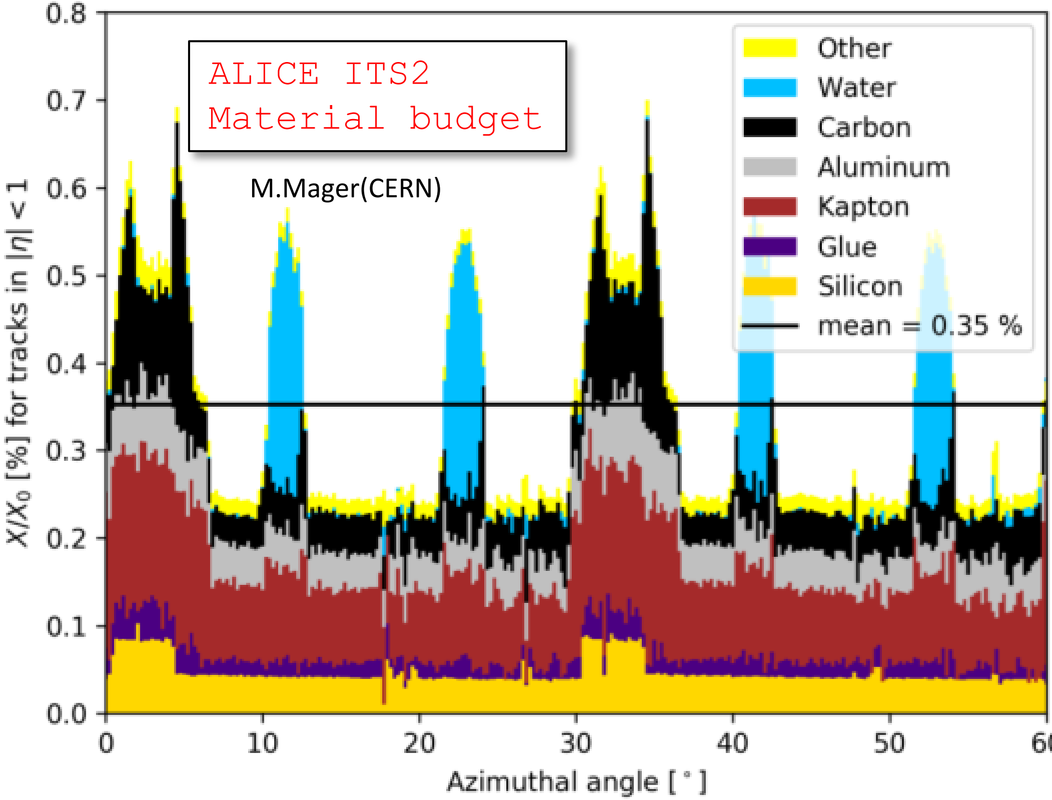


Inputs for engineering studies

ALICE ITS3: Bent sensors & stitching

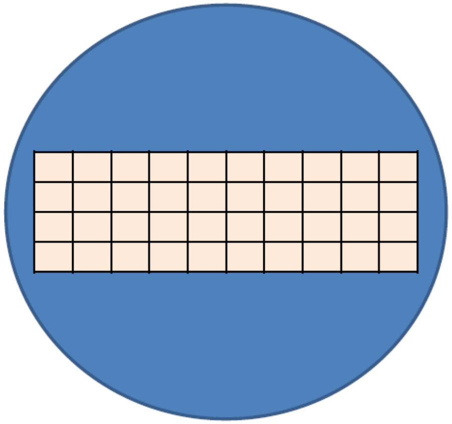






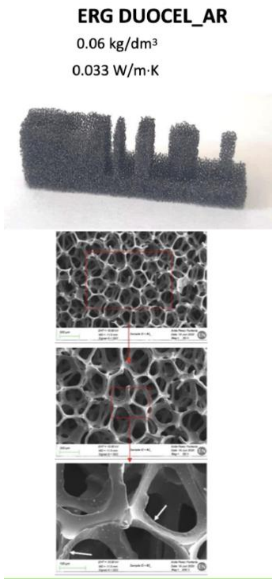
https://indico.cern.ch/event/1071914/

- ALICE-ITS3/CERN drives the R&D on Stitching + bent sensors:
  - ✓ Sensor part ~15% of total material budget
  - ✓ Sensors thinned down to 50 µm
  - ✓ Minimizing overlapping regions, minimizing minimal radius around the beam pipe
- Challenges and caveats (for e+e- colliders)
  - ✓ Mechanics ? Bonding ? Air cooling only ?
  - ✓ Design: Minimizing peripheral circuits (Fill factor ~90%)
  - ✓ Bent sensor performances ? Yield
  - ⇨ design rules constraints the minimal pitch (~22 µm)
  - ✓ ITS-3 do not have disk (chip periphery adds Z position constraint)
  - ✓ Approach validated in a limited radius range (R> 18mm)

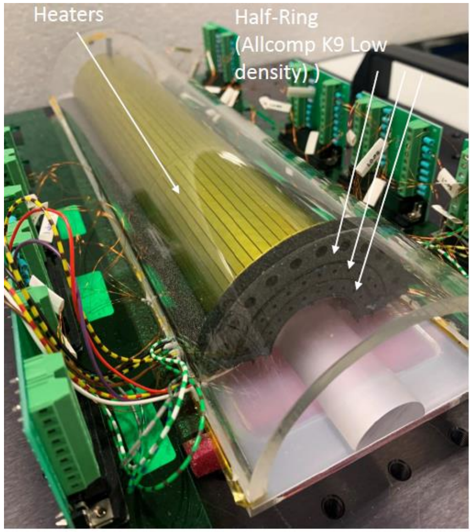


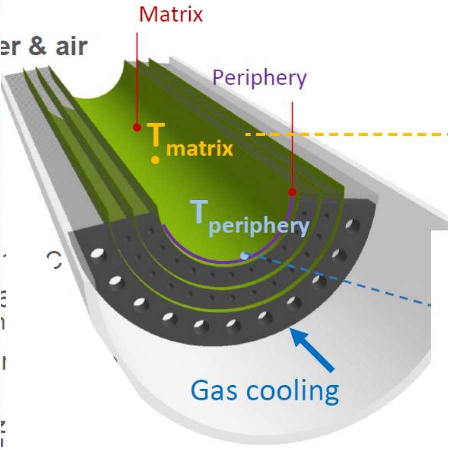
ALICE ITS3 tests


A. Kluge
on behalf of the ALICE collaboration
22 February, 2022
VCI

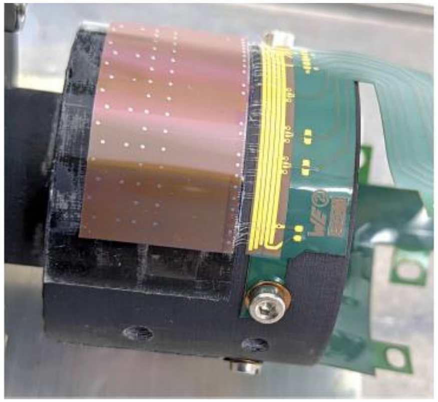


Carbon fiber foam spacer





Integration and cooling studies



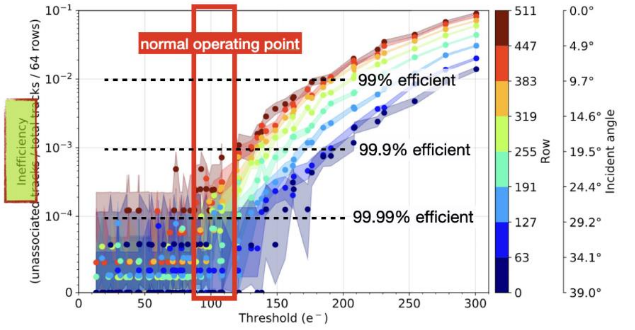
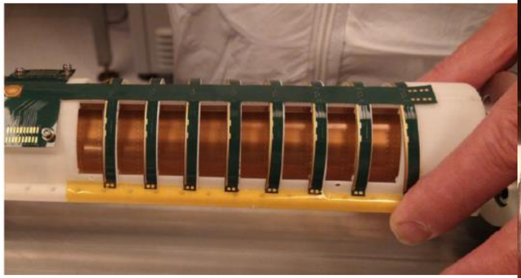


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

Bent sensors in test beam

- **1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)**

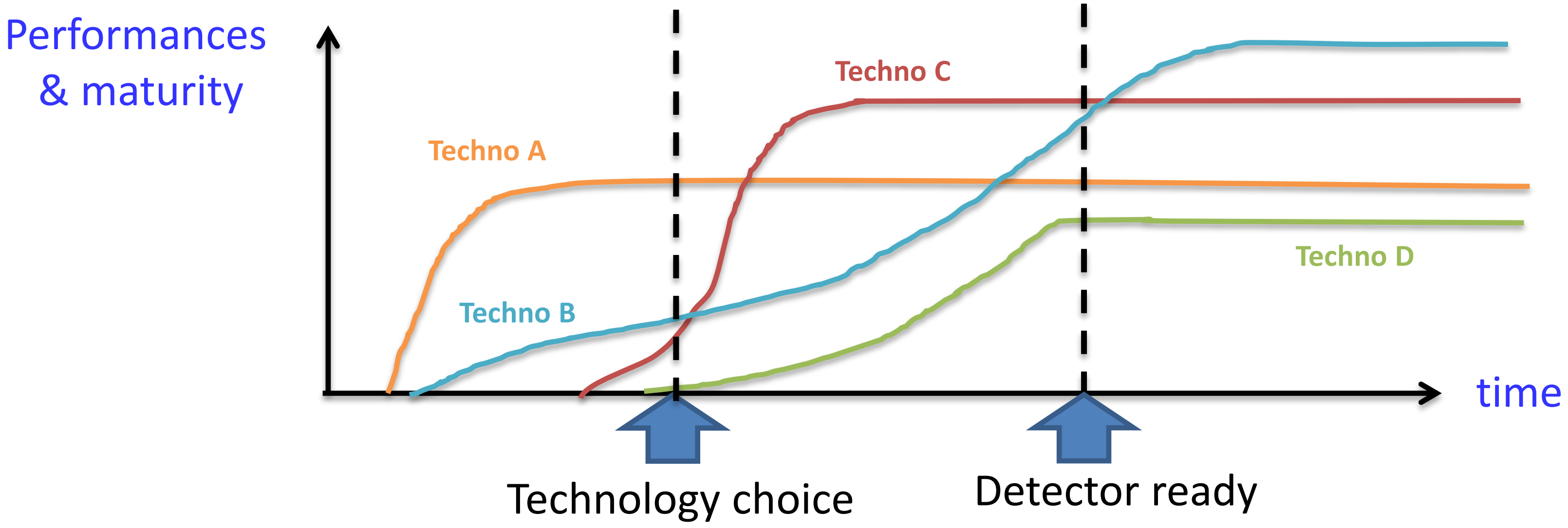


Inteconnexion tests (superALPIDE)

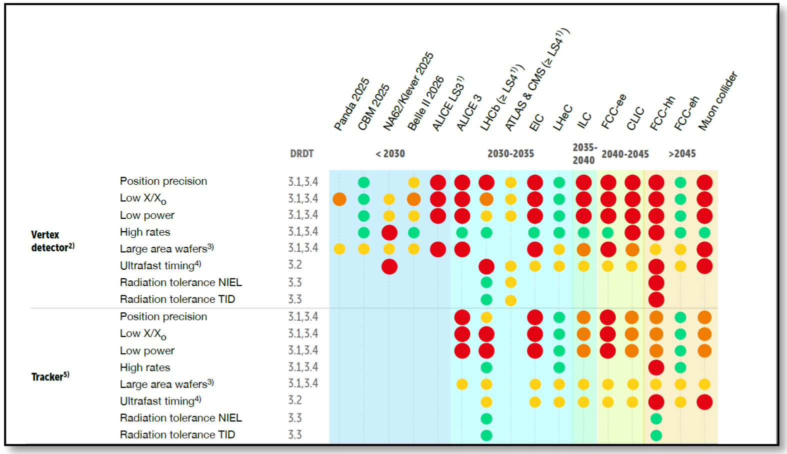
On going experiments pave the road for Higgs factory detectors
(many other examples)

Challenge 4: Time scale

Challenge: the time scale



- Vertex detectors are small and relatively fast to build
  - ✓ ~ 4-5 years projects
- Complete Silicon trackers need more time
- Avoid the Never Ending R&D syndrom
- Do not be too conservative
- Right balance to find between
  - ✓ Exploring technologies
  - ✓ Focusing on the most promising ones
- Mid-term applications provides invaluable milestones
  - ✓ CBM, ALICE ITS-3, Belle-2 upgrade, LHCb, EIC, etc.
  - ✓ e.g. OBELIX for Belle-2 inherited from TJ-Monopix-2



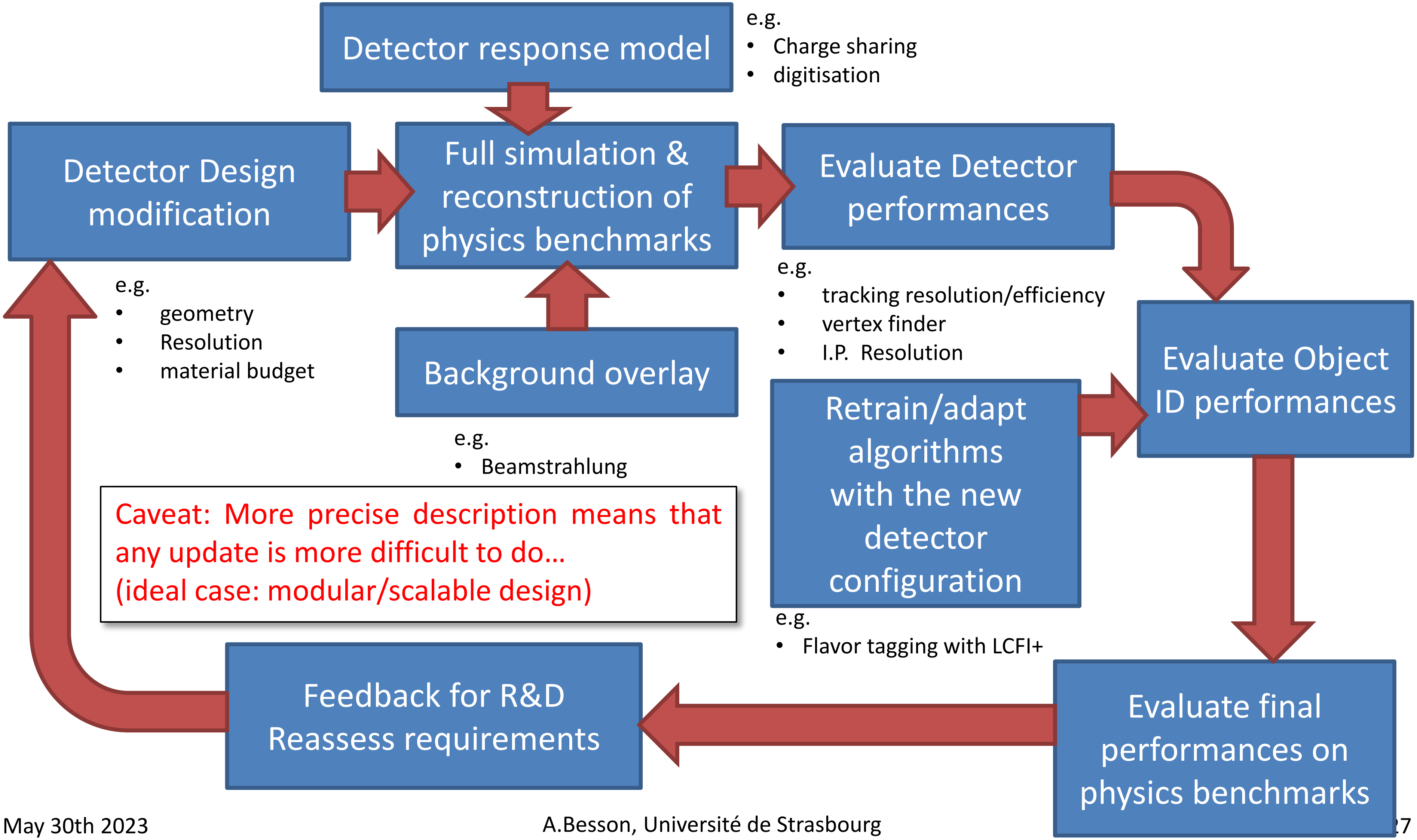
		DRDT	Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3[1]	ALICE 3	LHCb (≥ LS4[1])	ATLAS & CMS (≥ LS4[1])	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
			< 2030					2030-2035					2035-2040	2040-2045		>2045		
Vertex detector[2]	Position precision	3.1,3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X_o	3.1,3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1,3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1,3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers[3]	3.1,3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing[4]	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker[5]	Position precision	3.1,3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X_o	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1,3.4							🟢			🟢				🔴	🟢	
	Large area wafers[3]	3.1,3.4						🟡	🟡		🟡	🟡	🟡	🟡	🟡	🟡	🟡	🟡
	Ultrafast timing[4]	3.2							🟡		🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		

🔴 Must happen or main physics goals cannot be met 🟠 Important to meet several physics goals 🟡 Desirable to enhance physics reach 🟢 R&D needs being met

Challenge 5: Detector optimization and simulations

Challenge: optimization of the detector

- Example: Shall we target 18 or 22 µm pitch ?
- Caveat: One can not decouple detector optimization and algorithm optimization



Detector response model

e.g.
- Charge sharing
- digitisation

Detector Design modification

e.g.
- geometry
- Resolution
- material budget

Full simulation & reconstruction of physics benchmarks

Background overlay

e.g.
- Beamstrahlung

Evaluate Detector performances

e.g.
- tracking resolution/efficiency
- vertex finder
- I.P. Resolution

Retrain/adapt algorithms with the new detector configuration

e.g.
- Flavor tagging with LCFI+

Evaluate Object ID performances

Evaluate final performances on physics benchmarks

Feedback for R&D Reassess requirements

Caveat: More precise description means that any update is more difficult to do…
(ideal case: modular/scalable design)

Optimization of the detector: pragmatic approach

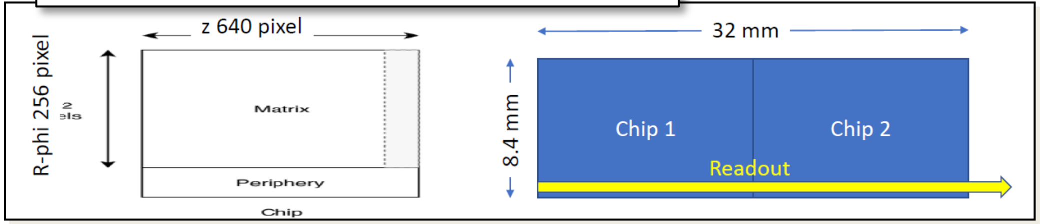
- One does not need to target the best performances from the beginning

- Added value of mockups / demonstrators / engineering designs
  - ✓ Relatively cheap but realistic enough
  - ✓ Study conflicting requirements (material, cooling, services, mechanics, etc.)
  - ✓ Check issues difficult to anticipate (e.g. available space for services, etc.)
  - ✓ Reinforce the cooperation between different expertises (e.g. chip design/mechanics/DAQ)
  - ✓ Integrated test beams possible
  - ⇨ DRDs should be the place to do it !

A pragmatic approach: mechanical/simulation studies for the IDEA vertex detector

- Starts from a detector concept and chip modules
  - ✓ Based on ARCADIA design

Chip model based on ARCADIA



Fabrizio Palla[1]

Manuela Boscolo [2], Filippo Bosi [1], Francesco Fransesini [2], Stefano Lauciani [2]

[1]*INFN Sezione di Pisa, Italy*

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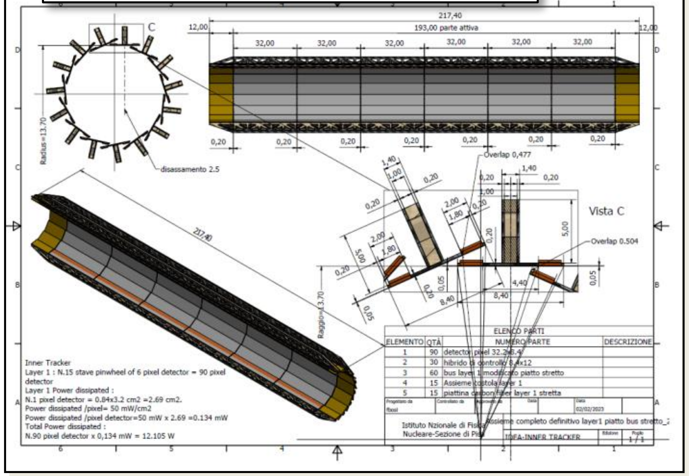
First Annual U.S. Future Circular Collider Workshop

BNL, April 24-26, 2023

Single layer description



Inner Tracker
Layer 1 : N.15 stave pinwheel of 6 pixel detector = 90 pixel detector
Layer 1 Power dissipated :
N.1 pixel detector = 0.84x3.2 cm2 =2.69 cm2.
Power dissipated /pixel= 50 mW/cm2
Power dissipated /pixel detector=50 mW x 2.69 =0.134 mW
Total Power dissipated :
N.90 pixel detector x 0,134 mW = 12.105 W

Layer 1

15 overlapping staves of 6 modules each

Pinwheel geometry: all modules at the same (smallest) radius

Power budget ~12 W

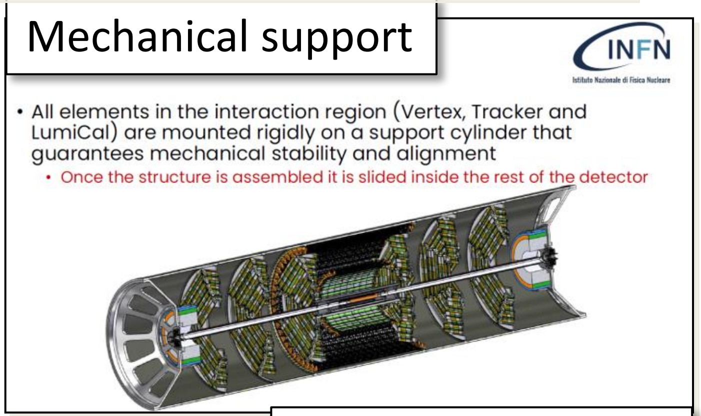
Total weight ~22 grams

Total thickness 0.25% X_0

Silicon: 0.053% X_0

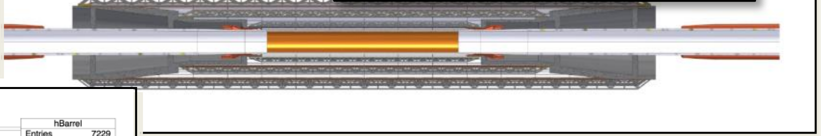
Power and readout bus: 0.056% X_0

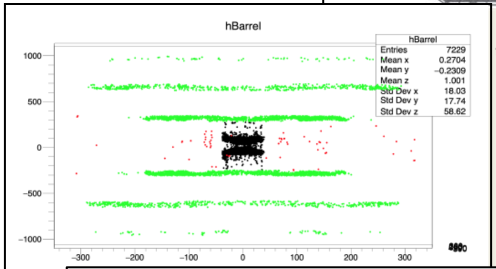
Mechanical support



- All elements in the interaction region (Vertex, Tracker and LumiCal) are mounted rigidly on a support cylinder that guarantees mechanical stability and alignment
  - Once the structure is assembled it is slided inside the rest of the detector

Vertex + beam pipe





Figur
Z →
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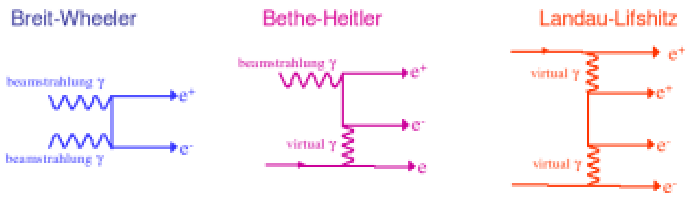
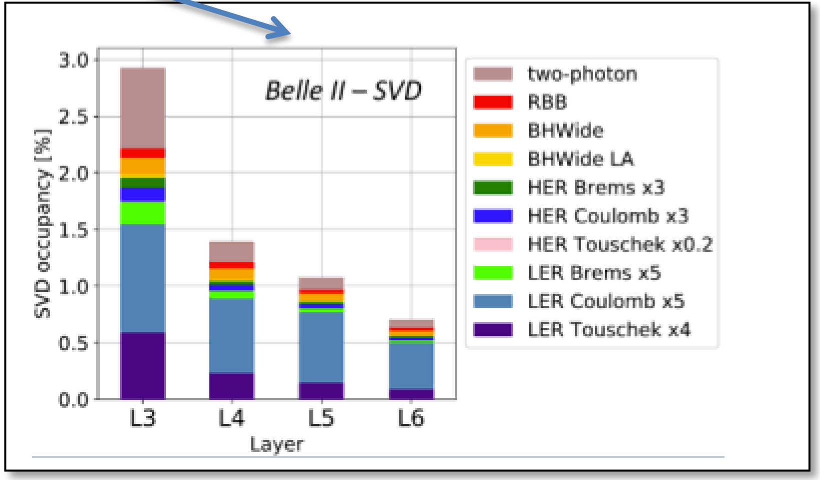
Model implemented in Key4hep
A. Ilg Fcee MDI Meeting 15.05.2023

Challenge 6: understanding beam related background

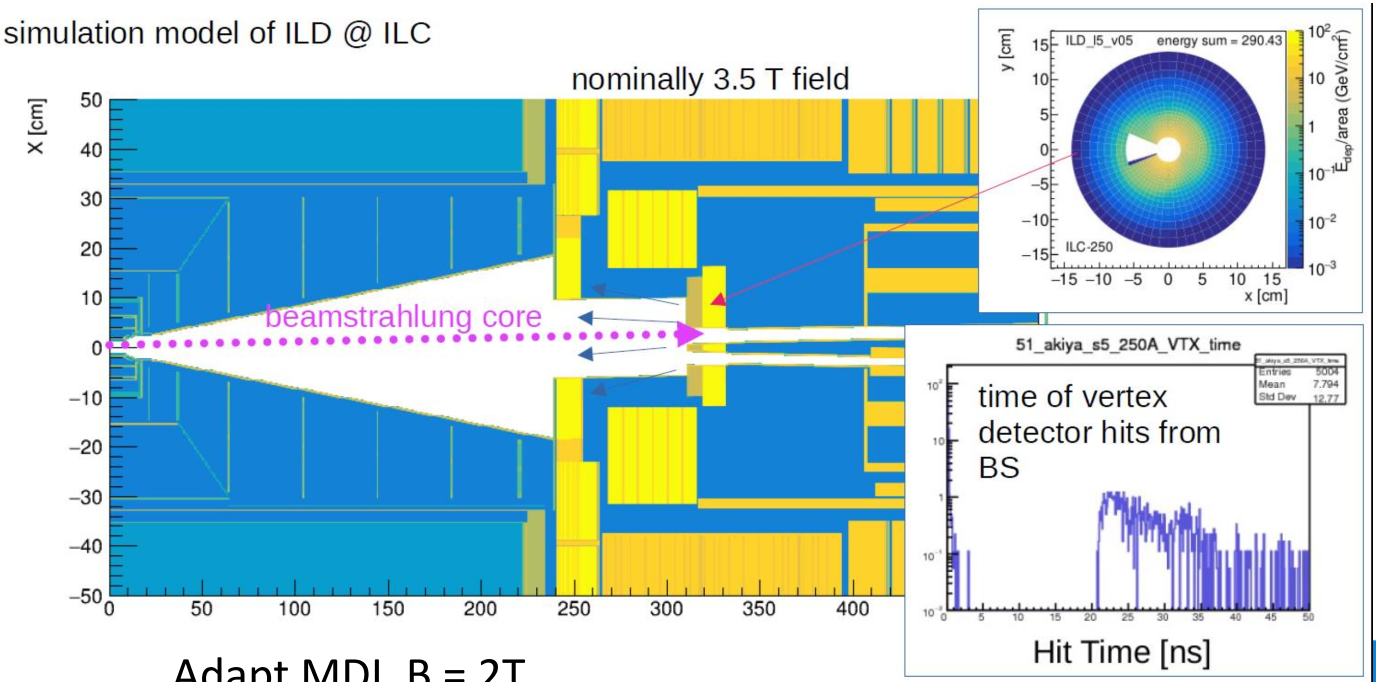
Challenge: understand beam related backgrounds



- Sources:
  - Incoherent pairs (« beamstrahlung »)
  - Synchrotron
  - Beam loss (circular machines)
  - Radiative bhabha
  - Beam gas, etc.
- Usually one considers that occupancy ~< 10^{-2}-10^{-3} is safe for tracking/vertexing purposes
- Experience from ILC studies over 20 years
  - Any modification in the Interaction region (beam scheme, beam pipe design, B field) might bring surprises
  - One should not consider that a 10^{-4} occupancy estimation means that there is no issue.
    - The robustness is questionnable
    - Large possible variations in some acceptance corners (asymmetries in φ or z)
    - Safety factor absolutely mandatory
    - 2 independant simulation tools would be welcome (GuineaPig, Fluka, etc.)
- Experience from Belle-2
  - Discrepancies observed between simulations and first collisions
- Direct beam background vs backscattered background
  - Generally the backscattered ones are more sensitive to any MDI change.
- What about timing information to reject background ?
  - Need ~ 5 ns to reject backscattered particles
  - Is it worth paying the price in terms of additionnal power ?
- What about cluster shape to reject background ?
  - Need very good sensitive thickness/pitch ratio (> 2).
  - Charge information helps.
  - (you actually reject very low pT particles)



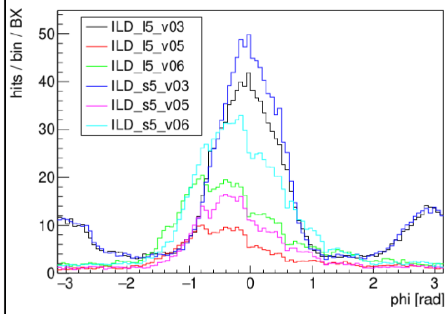
Example of background study: ILD, from linear to circular


simulation model of ILD @ ILC

nominally 3.5 T field

time of vertex detector hits from BS

[D. Jeans LCWS2023](#)



Adapt MDI, B = 2T,

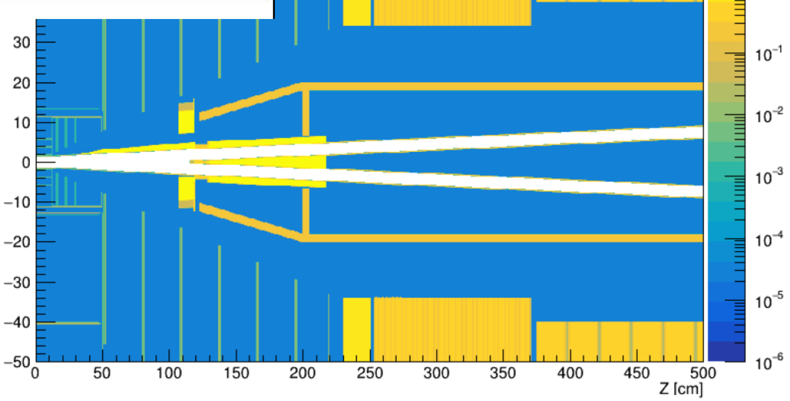
Sensitive to precise B-field map

Adapt Beam structure

Effect in TPC also being studied

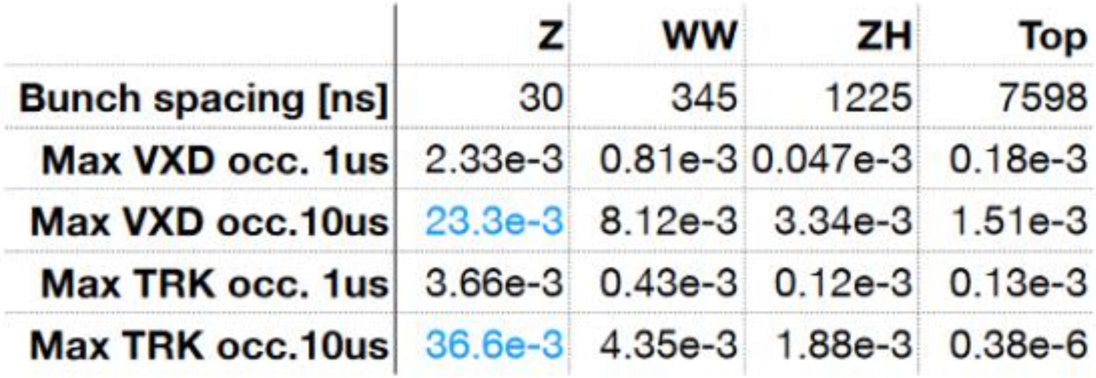
at FCCee,

quasi-continuous ion cloud from ~14M bunch crossings



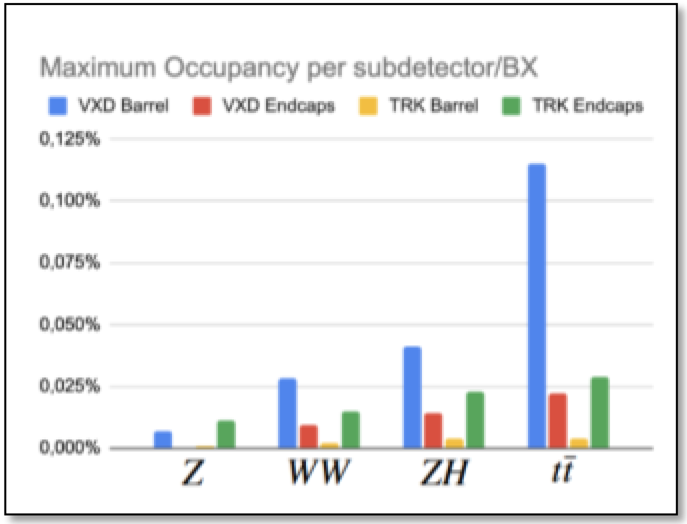
- at FCCee, MDI extends to ~1m from IP
  → 6 times more beamstrahlung background hits in TPC

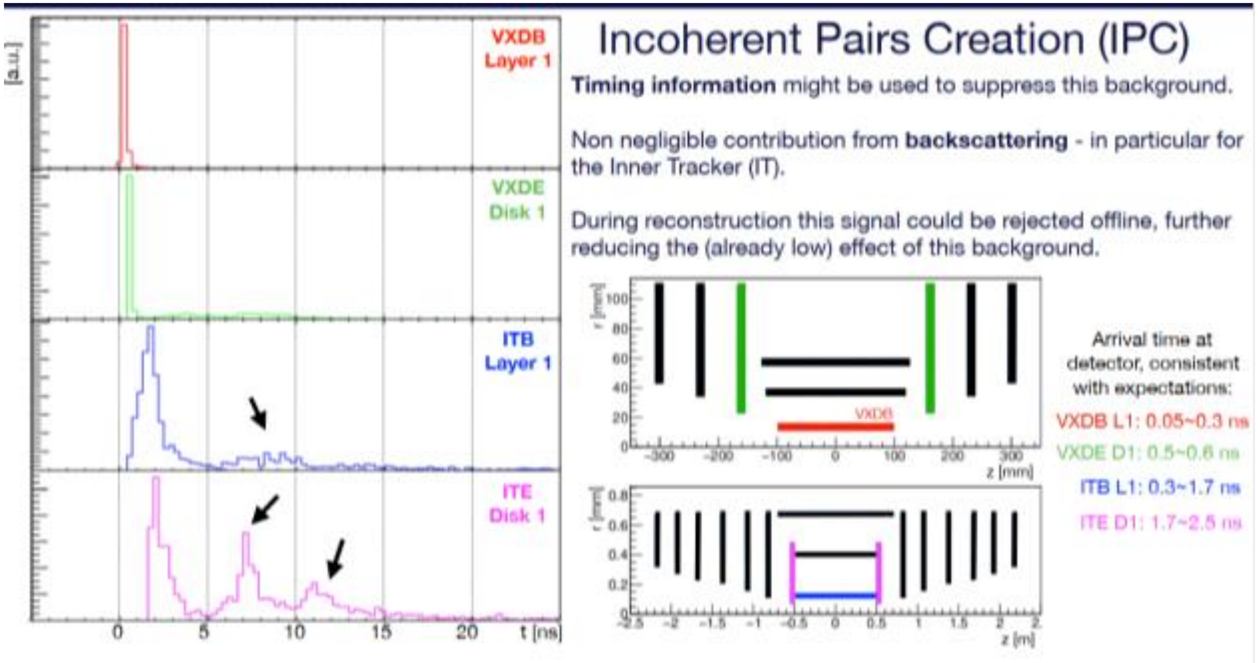
Example of study in CLD



	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

US FCC workshop 25/04/2023 Ciarma





Incoherent Pairs Creation (IPC)

Timing information might be used to suppress this background.

Non negligible contribution from **backscattering** - in particular for the Inner Tracker (IT).

During reconstruction this signal could be rejected offline, further reducing the (already low) effect of this background.

Arrival time at detector, consistent with expectations:

VXDB L1: 0.05~0.3 ns

VXDE D1: 0.5~0.8 ns

ITB L1: 0.3~1.7 ns

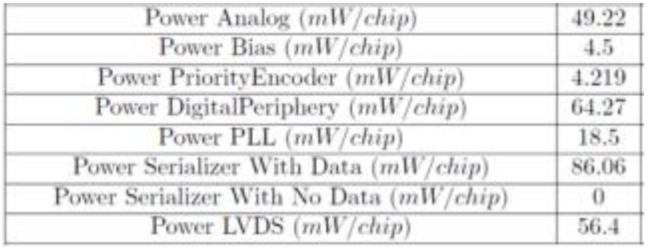
ITE D1: 1.7~2.5 ns

BX rate might be an issue at the Z-pole

Timing resolution range to reject background ~ 1 ns

Challenge 7: The Power

Power challenges

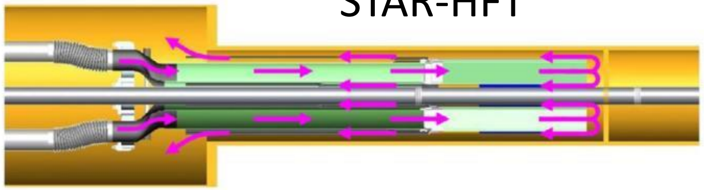


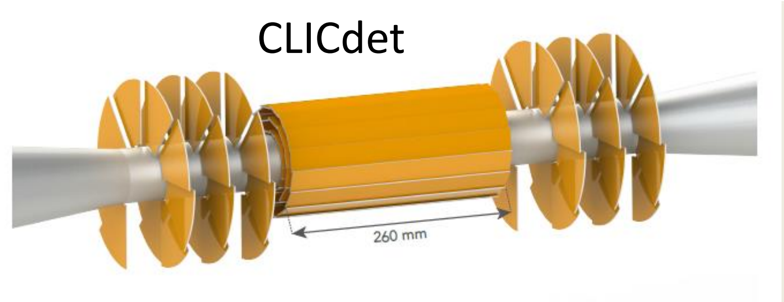
Power Analog ($mW/chip$)	49.22
Power Bias ($mW/chip$)	4.5
Power PriorityEncoder ($mW/chip$)	4.219
Power DigitalPeriphery ($mW/chip$)	64.27
Power PLL ($mW/chip$)	18.5
Power Serializer With Data ($mW/chip$)	86.06
Power Serializer With No Data ($mW/chip$)	0
Power LVDS ($mW/chip$)	56.4

MIMOSIS like architecture, 180 nm

- Power is in conflict with all other parameters
- Baseline:
  - ✓ Air flow cooling only to minimize material budget
  - ✓ Up to ~ 20 mW/cm^2
    - what is the limit ? ~50 mW/cm^2 or even more ?
- Driving parameters:
  - ✓ # channels, Time resolution / data flux
  - ✓ Surface (VXD ~ 3500 cm^2 ; tracker O(10 m^2)
  - ✓ Power Pulsing (ILC/CLIC) ⇨ Constraints more relaxed w.r.t. FCCee
- The « Power paradox »
  - ✓ Small radius ⇨ Higher hit density and Power/cm^2 but small fraction of total power
  - ✓ Higher radius ⇨ less hit density but higher total power/layer
- Power sharing
  - ✓ Analog part: O(25-50%) ⇨ density of pixels, charge collection speed
  - ✓ Digital part: O(25-50%) ⇨ data flux, freq.
  - ✓ Output→DAQ: maximum flux. (25%)
- Architecture optimization is important
  - ✓ Priority encoder (limited by flux)
  - ✓ Asynchronous might be adapted (tot, etc.)
  - ✓ Etc.
- Technology feature size
  - ✓ e.g. 180nm to 65 nm: ~50% Power reduction
- Air extraction:
  - ✓ In conflict with disks and forward acceptance
    - (≠ALICE ITS2/3, Belle-2, STAR-HFT)

STAR-HFT





CLICdet

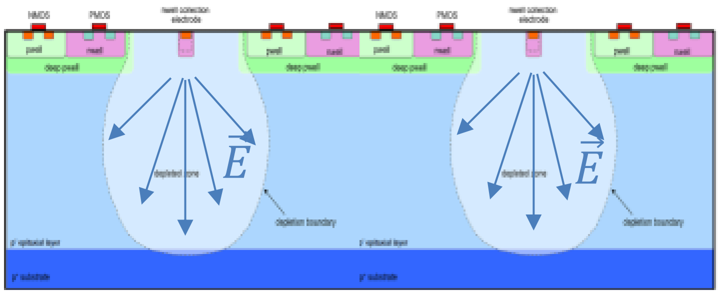
Challenge 8: Chip design

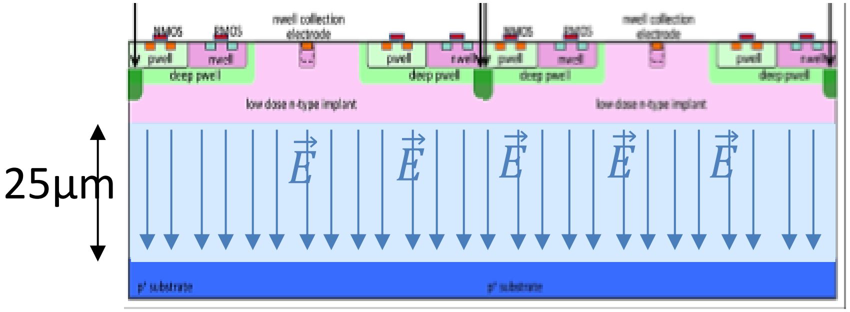
Design challenges: From new ideas to real chips

- How to really make it ?
  - ✓ R&D prototypes ≠ final production chip installed in real experiment
  - ✓ Submission cost issue for R&D
    - Trade-off between new (expensive) technologies and older (cheaper) technologies
- The complexity is growing
  - ✓ New read-out architecture, etc.
  - ✓ Work flow inspired from successfull chips installed in experiments (e.g. ALPIDE for ALICE-ITS2)
    - ⇨ push to concentrate on few technologies
  - ✓ Verification tools are absolutely crucial
    - « Digital on top »
    - Global support on tools DRD3/ DRD7 connexion !
- Connexion with foundries absolutely crucial
  - ✓ Contracts, confidentiality, etc.
  - ✓ Long term plans to maintain interest from fourndries (HEP is a small player)
  - ✓ Access to technology options to optimize it for HEP applications

Example: MIMOSIS (CBM-MVD) & Decision on options for sensing elements

Process modification: Standard? P-stop? N-Gap?





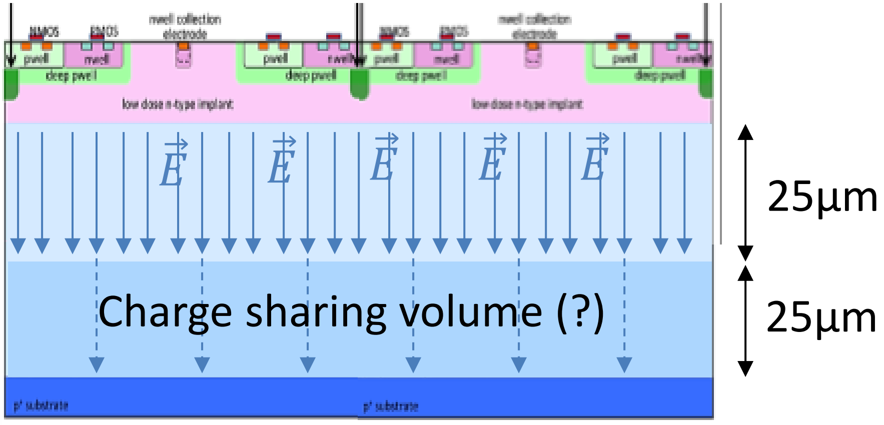
$\sigma = 4-5\ \mu\text{m}$
$> 3 \times 10^{13} n_{eq}/cm^2$

Spatial resolution
Rad. hardness

$\sigma = 5-7\ \mu\text{m}$
$> 30 \times 10^{13} n_{eq}/cm^2$

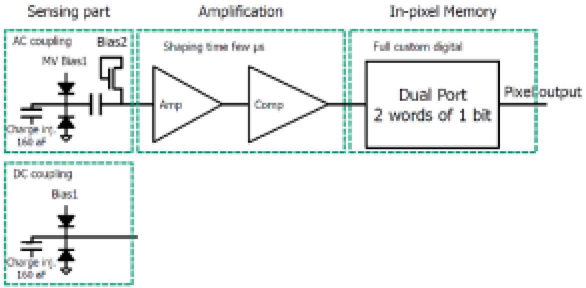
Process options inherited from ALPIDE

25 or 50 µm epi?



- Better spatial res. at given rad. tolerance?
- Higher S/N => Robustness to external noise?
- Nuclear fragment ID by dE/dx?

AC? DC? pixel



- DC pixel – limited rad. hardness.
- AC Pixel – more biasing lines.

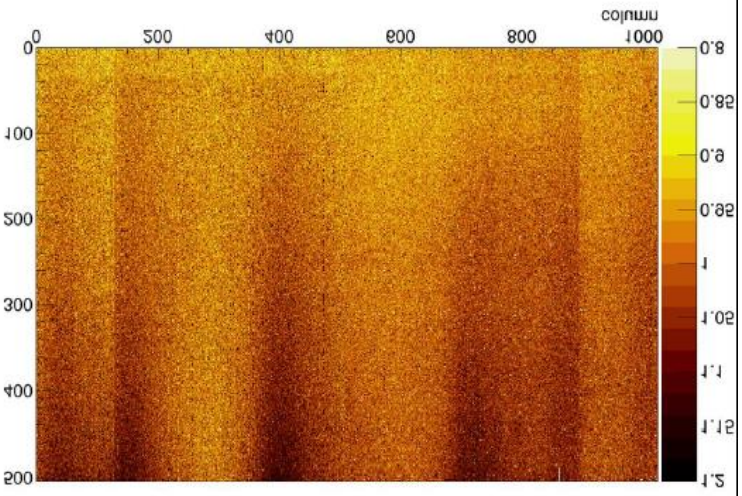
W. Snoeys et al., NIM-A Vol.871 (2017) 90–96.
Munker, Vertex 2018, Status of silicon detector R&D at CLIC

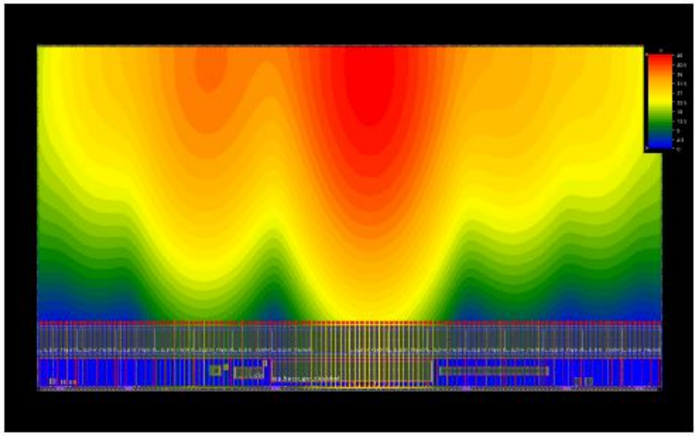
Mimosis-1 Verification tools example

- Large and complex designs need
  - ✓ A hierarchy in the work flow to keep submission on schedule
  - ✓ Verification tools that can be run in a reasonnable time
  - ✓ Knowledge of these tools is crucial
- Example Power-grid problem observed in MIMOSIS-1
  - ✓ Threshold shifts
  - ✓ Problem fixed quickly

F. Morel DRD7 kick-off meeting

Threshold shift of MIMOSIS-1 (measurements)

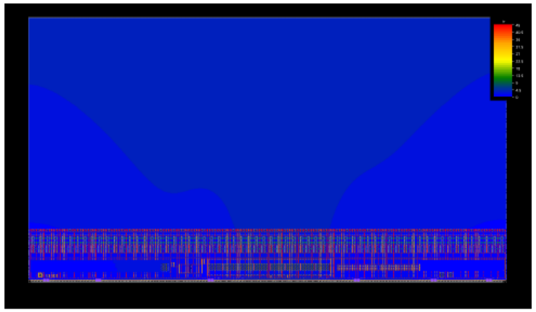




IR drop on AVDD (simulations)
0-45 mV scale

MIMOSIS-1
Mean= 26 mV

MIMOSIS-2
Mean = 3 mV



Summary

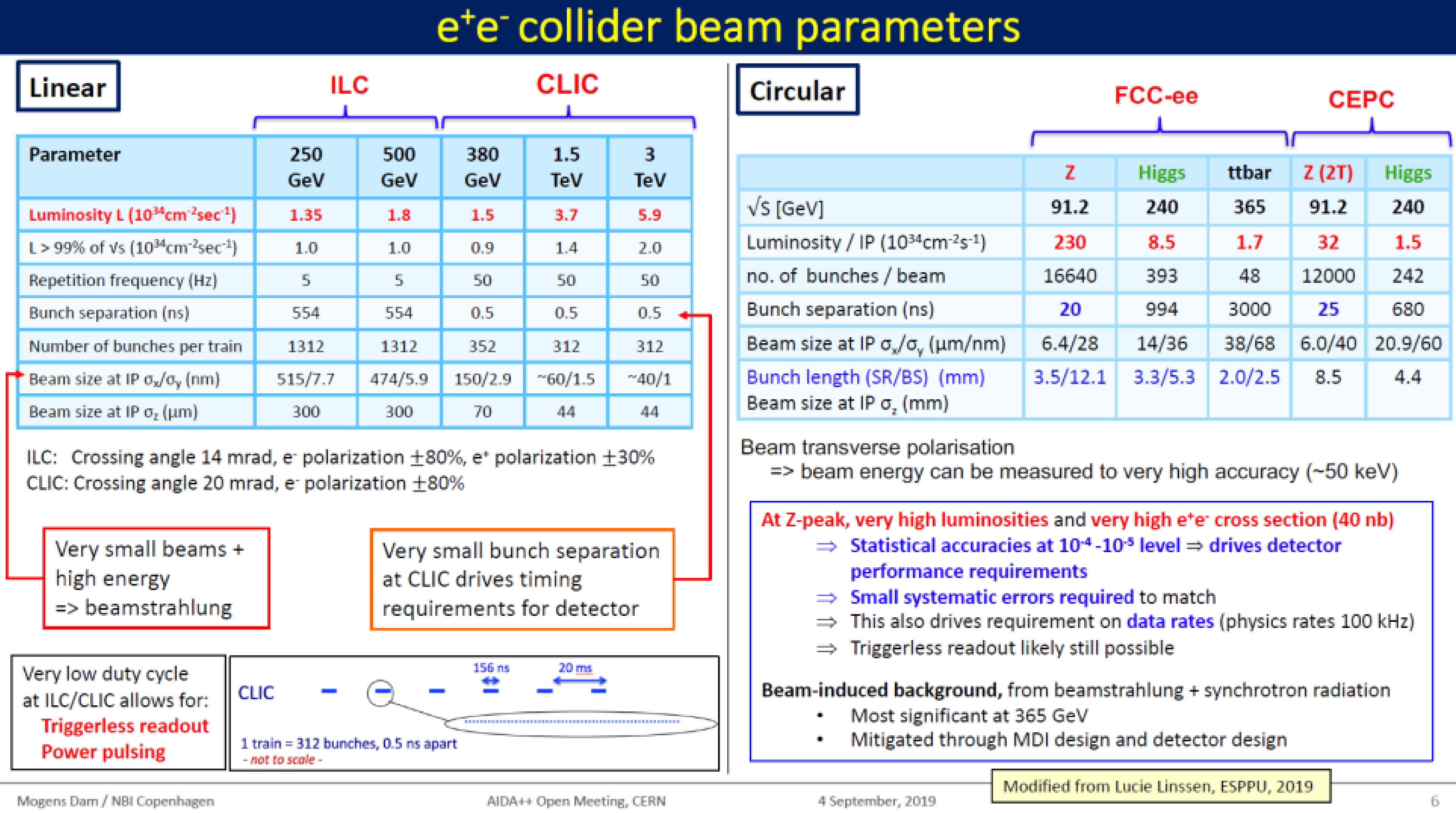
- Apologies for not covering
  - ✓ Many technologies and on going R&D
    - (FPCCD, SOI, DEPFET, BiCMOS (SiGe), etc.
  - ✓ Cooling R&D (MCC, etc.)
  - ✓ Read-out
  - ✓ Operation and monitoring (Built-in Self Test (BIST) approach ?)
  - ✓ Alignment

- The physics requirements impose a hierarchy between the conflicting parameters
  - ✓ Granularity and material budget first !
  - ✓ CMOS/MAPS Pixel sensors offer the best compromise for the inner vertexing/tracking layers
  - ✓ Specialized timing layers

- Integration R&D is a final performances driver !
  - ✓ Fill the gap between nice ideas and real detectors
    - e.g. Stitching & bent sensors developed in ALICE-ITS3 context

- Strategy
  - ✓ The right balance has to be found inside DRDs between defining priorities and allowing new ideas to emerge
  - ✓ Given the complex parameter space of R&D and detector design, a pragmatic approach should be privileged
    - Increasing complexity step by step, demonstrators, mock-ups, experience from mid-term experiments, etc.

backup



e^+e^- collider beam parameters

Linear

	ILC		CLIC		
Parameter	**250 GeV**	**500 GeV**	**380 GeV**	**1.5 TeV**	**3 TeV**
Luminosity L (10^{34}cm^{-2}sec^{-1})	**1.35**	**1.8**	**1.5**	**3.7**	**5.9**
L > 99% of √s (10^{34}cm^{-2}sec^{-1})	1.0	1.0	0.9	1.4	2.0
Repetition frequency (Hz)	5	5	50	50	50
Bunch separation (ns)	554	554	0.5	0.5	0.5
Number of bunches per train	1312	1312	352	312	312
Beam size at IP σ_x/σ_y (nm)	515/7.7	474/5.9	150/2.9	~60/1.5	~40/1
Beam size at IP σ_z (µm)	300	300	70	44	44

ILC: Crossing angle 14 mrad, e^- polarization ±80%, e^+ polarization ±30%
CLIC: Crossing angle 20 mrad, e^- polarization ±80%

Very small beams + high energy
=> beamstrahlung

Very small bunch separation at CLIC drives timing requirements for detector

Very low duty cycle at ILC/CLIC allows for:
Triggerless readout
Power pulsing

1 train = 312 bunches, 0.5 ns apart
- not to scale -

Circular

	FCC-ee			CEPC	
	Z	**Higgs**	**ttbar**	**Z (2T)**	**Higgs**
√s [GeV]	**91.2**	**240**	**365**	**91.2**	**240**
Luminosity / IP (10^{34}cm^{-2}s^{-1})	**230**	**8.5**	**1.7**	**32**	**1.5**
no. of bunches / beam	16640	393	48	12000	242
Bunch separation (ns)	**20**	994	3000	**25**	680
Beam size at IP σ_x/σ_y (µm/nm)	6.4/28	14/36	38/68	6.0/40	20.9/60
Bunch length (SR/BS) (mm) Beam size at IP σ_z (mm)	3.5/12.1	3.3/5.3	2.0/2.5	8.5	4.4

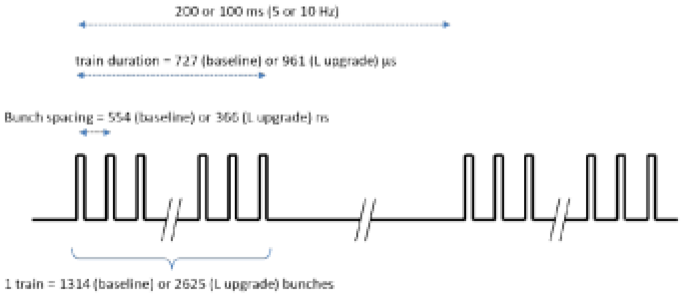
Beam transverse polarisation
=> beam energy can be measured to very high accuracy (~50 keV)

At Z-peak, very high luminosities and **very high e^+e^- cross section (40 nb)**
⇒ **Statistical accuracies at 10^{-4}-10^{-5} level ⇒ drives detector performance requirements**
⇒ **Small systematic errors required** to match
⇒ This also drives requirement on **data rates** (physics rates 100 kHz)
⇒ Triggerless readout likely still possible

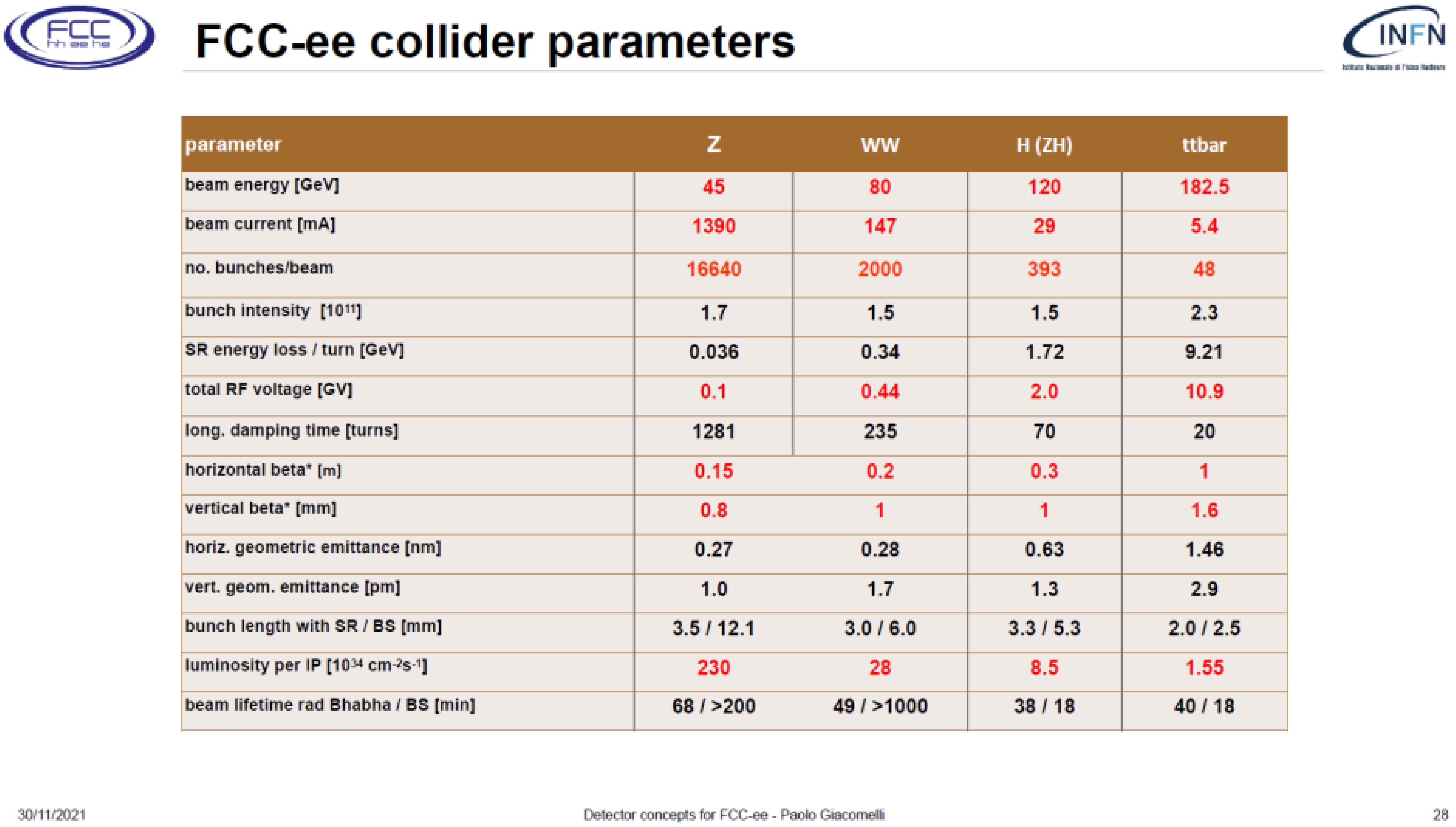
Beam-induced background, from beamstrahlung + synchrotron radiation
- Most significant at 365 GeV
- Mitigated through MDI design and detector design

Mogens Dam / NBI Copenhagen AIDA++ Open Meeting, CERN 4 September, 2019 Modified from Lucie Linssen, ESPPU, 2019 6

(slide from Mogens Dam/Lucie Linssen)



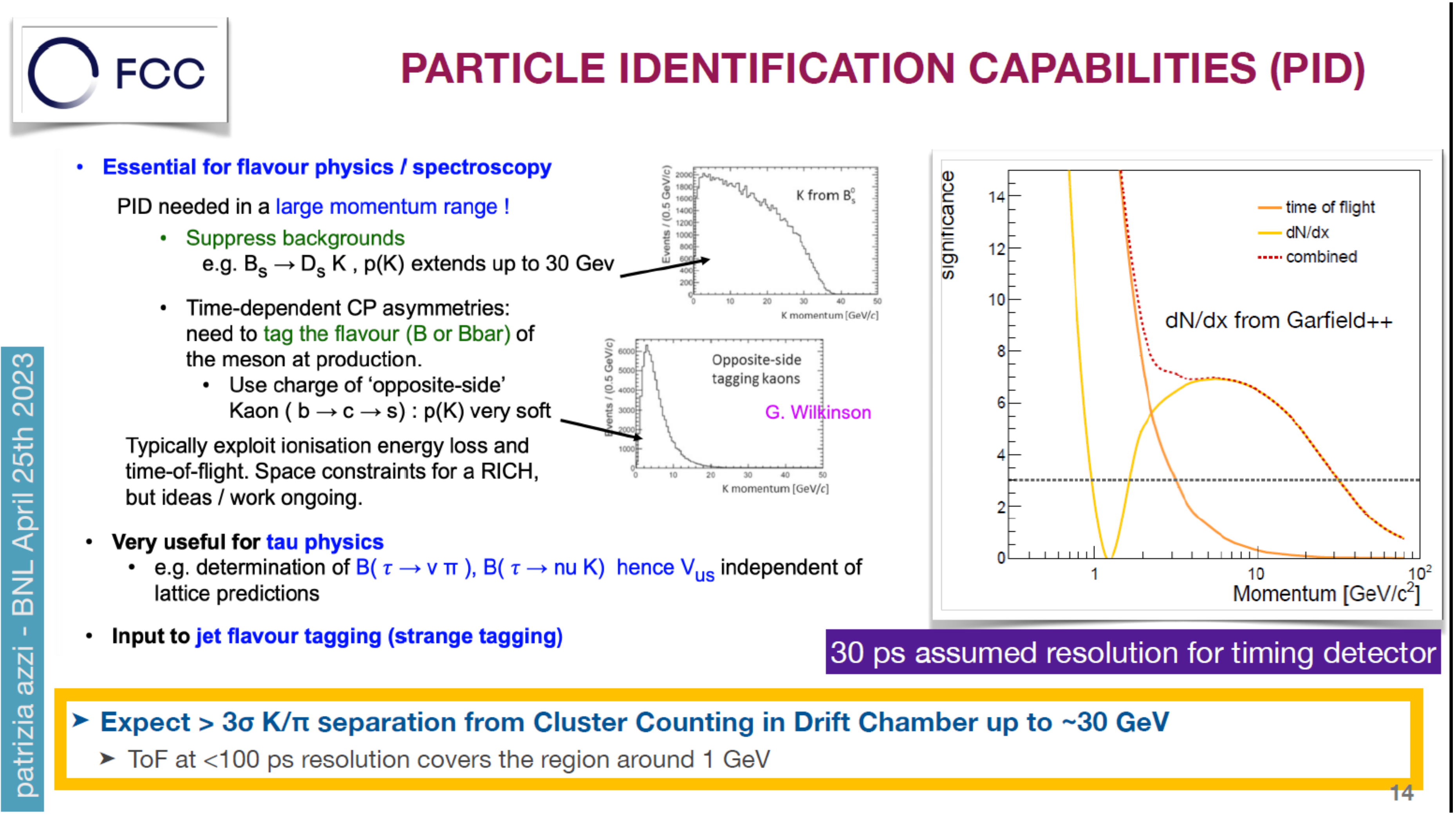
Collider parameters



FCC-ee collider parameters

parameter	Z	WW	H (ZH)	ttbar
beam energy [GeV]	45	80	120	182.5
beam current [mA]	1390	147	29	5.4
no. bunches/beam	16640	2000	393	48
bunch intensity [10^{11}]	1.7	1.5	1.5	2.3
SR energy loss / turn [GeV]	0.036	0.34	1.72	9.21
total RF voltage [GV]	0.1	0.44	2.0	10.9
long. damping time [turns]	1281	235	70	20
horizontal beta* [m]	0.15	0.2	0.3	1
vertical beta* [mm]	0.8	1	1	1.6
horiz. geometric emittance [nm]	0.27	0.28	0.63	1.46
vert. geom. emittance [pm]	1.0	1.7	1.3	2.9
bunch length with SR / BS [mm]	3.5 / 12.1	3.0 / 6.0	3.3 / 5.3	2.0 / 2.5
luminosity per IP [10^{34} cm^{-2}s^{-1}]	230	28	8.5	1.55
beam lifetime rad Bhabha / BS [min]	68 / >200	49 / >1000	38 / 18	40 / 18

30/11/2021 Detector concepts for FCC-ee - Paolo Giacomelli 28



FCC

PARTICLE IDENTIFICATION CAPABILITIES (PID)

- **Essential for flavour physics / spectroscopy**

PID needed in a large momentum range !

- Suppress backgrounds
  e.g. $B_s \rightarrow D_s K$, p(K) extends up to 30 Gev
- Time-dependent CP asymmetries: need to tag the flavour (B or Bbar) of the meson at production.
  - Use charge of ‘opposite-side’ Kaon ($b \rightarrow c \rightarrow s$) : p(K) very soft

Typically exploit ionisation energy loss and time-of-flight. Space constraints for a RICH, but ideas / work ongoing.

G. Wilkinson

- **Very useful for tau physics**
  - e.g. determination of $B(\tau \rightarrow \nu \pi)$, $B(\tau \rightarrow \text{nu } K)$ hence V_{us} independent of lattice predictions
- **Input to jet flavour tagging (strange tagging)**

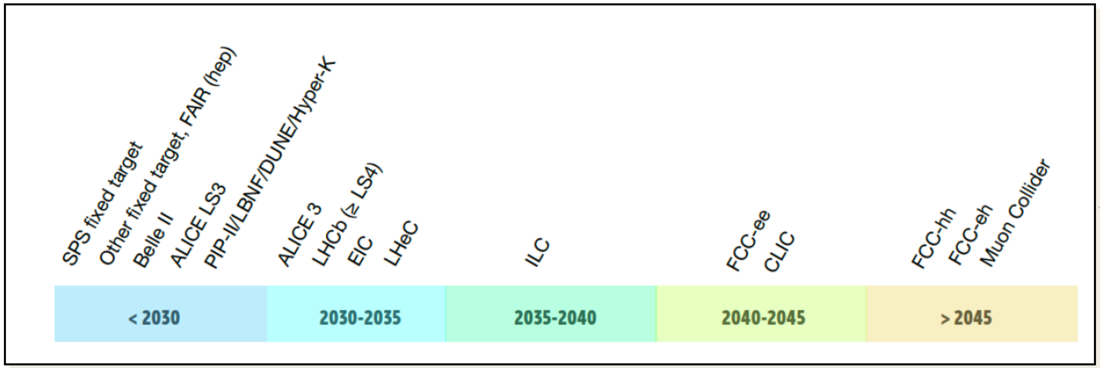
30 ps assumed resolution for timing detector

➤ **Expect > 3σ K/π separation from Cluster Counting in Drift Chamber up to ~30 GeV**
  ➤ ToF at <100 ps resolution covers the region around 1 GeV

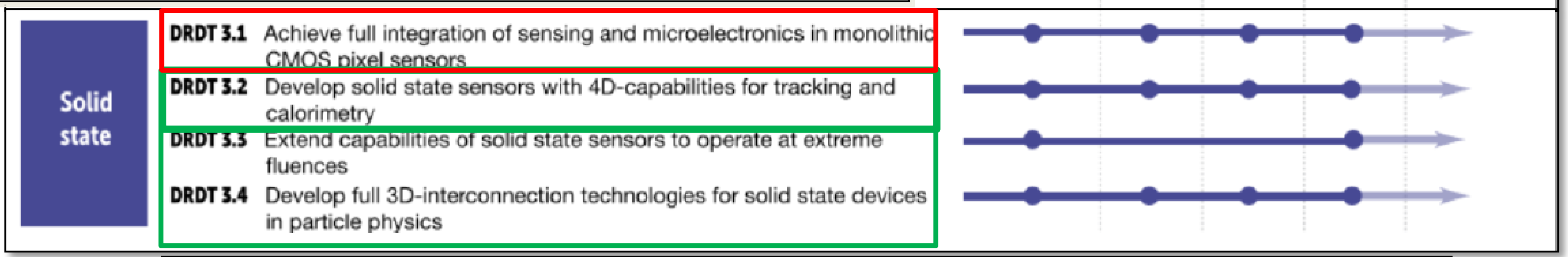
14

patrizia azzi - BNL April 25th 2023

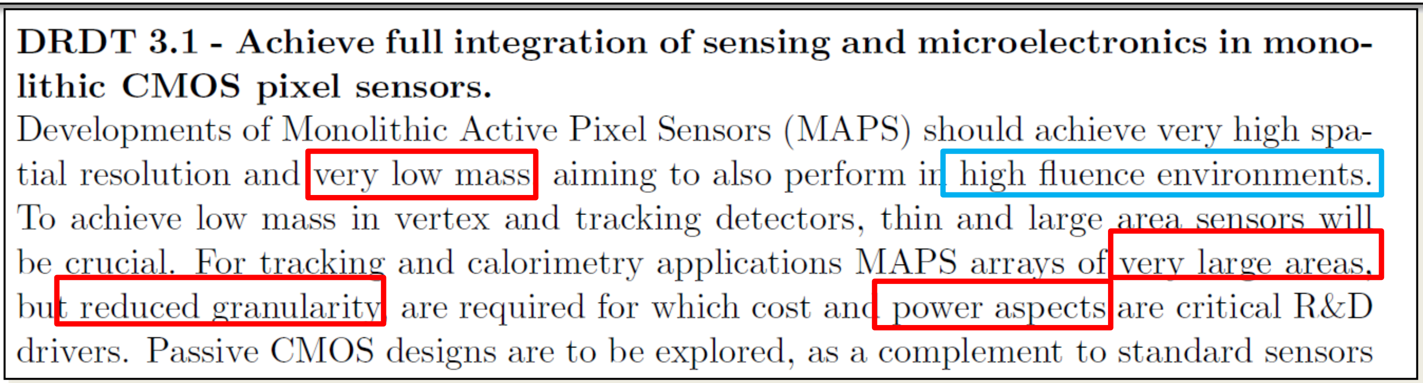
Detector R&D Roadmap: themes (DRDTs)



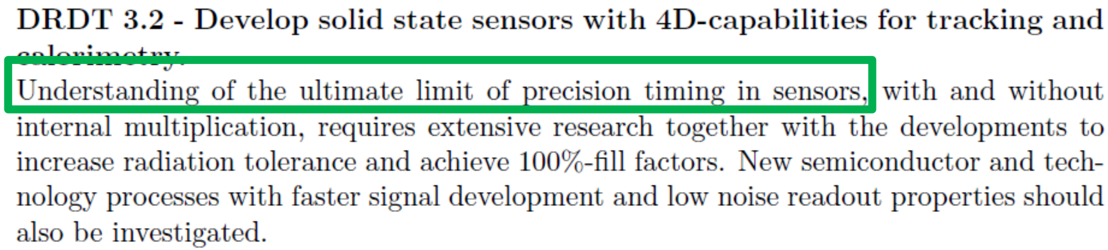
References: ECFA/RC/21/510
CERN-ESU-017
DOI: 10.17181/CERN.XDPL.W2EX



			< 2030	2030-2035	2035-2040	2040-2045	> 2045
Solid state	**DRDT 3.1**	Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors	●	●	●	●	→
	DRDT 3.2	Develop solid state sensors with 4D-capabilities for tracking and calorimetry	●	●	●	●	→
	DRDT 3.3	Extend capabilities of solid state sensors to operate at extreme fluences	●			●	→
	DRDT 3.4	Develop full 3D-interconnection technologies for solid state devices in particle physics	●	●	●	●	→



DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors



DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
Understanding of the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research together with the developments to increase radiation tolerance and achieve 100%-fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.

Synergies

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. ***ECFA supports a series of workshops*** *with the aim to* ***share challenges and expertise, to explore synergies in their efforts*** *and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).*

Goal: bring the entire e^+e^- Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

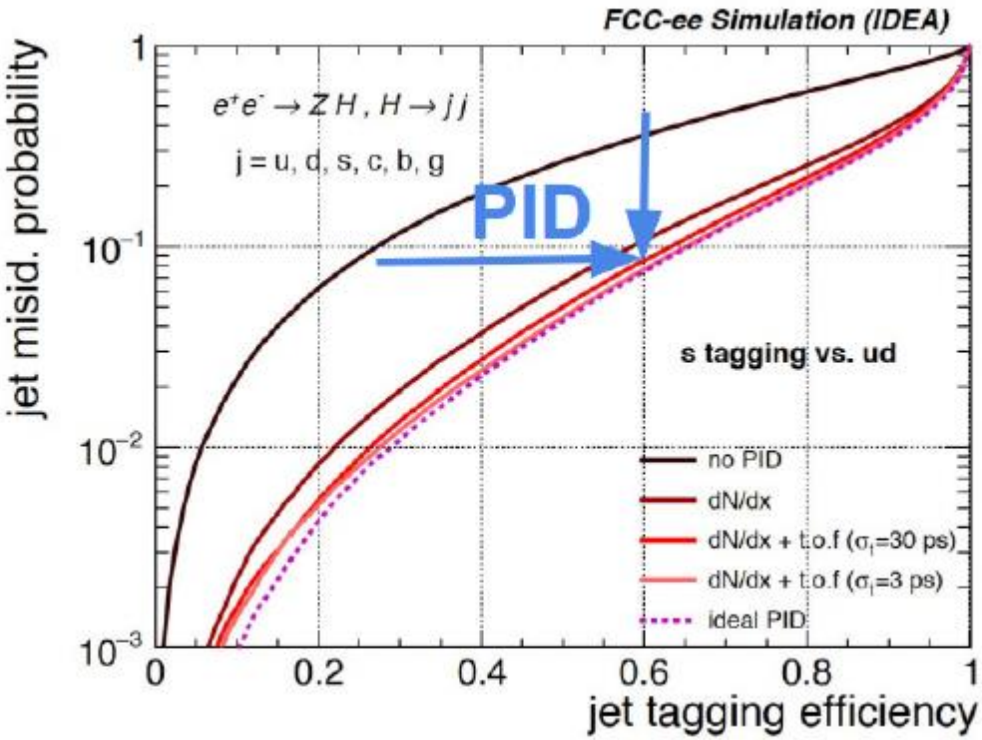
K. Jakobs, FCC Physics Workshop, Feb 2022

		DRDT	Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3[1]	ALICE 3	LHCb (≥ LS4[1])	ATLAS & CMS (≥ LS4[1])	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
			< 2030					2030-2035					203[illegible] 2040	2040-2045		>2045		
Vertex detector[2]	Position precision	3.1,3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X_0	3.1,3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1,3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1,3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers[3]	3.1,3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing[4]	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker[5]	Position precision	3.1,3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X_0	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1,3.4							🟢			🟢				🔴	🟢	
	Large area wafers[3]	3.1,3.4						🟡	🟡		🟡	🟡	🟡	🟡	🟡	🟡	🟡	🟡
	Ultrafast timing[4]	3.2							🟡		🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		
Time of flight[7]	Position precision	3.1,3.4				🟡		🟡		🟡	🟡	🟡		🟡			🟡	
	Low X/X_0	3.1,3.4				🟡		🟡		🟡	🟡	🟡		🟡			🟡	
	Low power	3.1,3.4				🟡		🟡		🟡	🟡	🟡		🟡			🟡	
	High rates	3.1,3.4																
	Large area wafers[3]	3.1,3.4				🟡		🟡		🟡	🟡			🟡				
	Ultrafast timing[4]	3.2				🔴		🔴		🟡	🔴	🔴		🟠			🔴	
	Radiation tolerance NIEL	3.3								🟡								
	Radiation tolerance TID	3.3								🟡								

🔴 **Must happen or main physics goals cannot be met** 🟠 **Important to meet several physics goals** 🟡 **Desirable to enhance physics reach** 🟢 **R&D needs being met**

Important similarities between FCCee requirements & Heavy ions experiments (ALICE ITS3, ALICE3, EIC, etc.)

s-tagging


FCC-ee Simulation (IDEA)
$e^+e^- \to ZH,\ H \to jj$
j = u, d, s, c, b, g
PID
s tagging vs. ud
no PID
dN/dx
dN/dx + t.o.f (σ_t=30 ps)
dN/dx + t.o.f (σ_t=3 ps)
ideal PID
jet misid. probability
jet tagging efficiency
1
10^{-1}
10^{-2}
10^{-3}
0
0.2
0.4
0.6
0.8
1

HV-MAPS for the LHCb Upgrade-II
Mighty Tracker

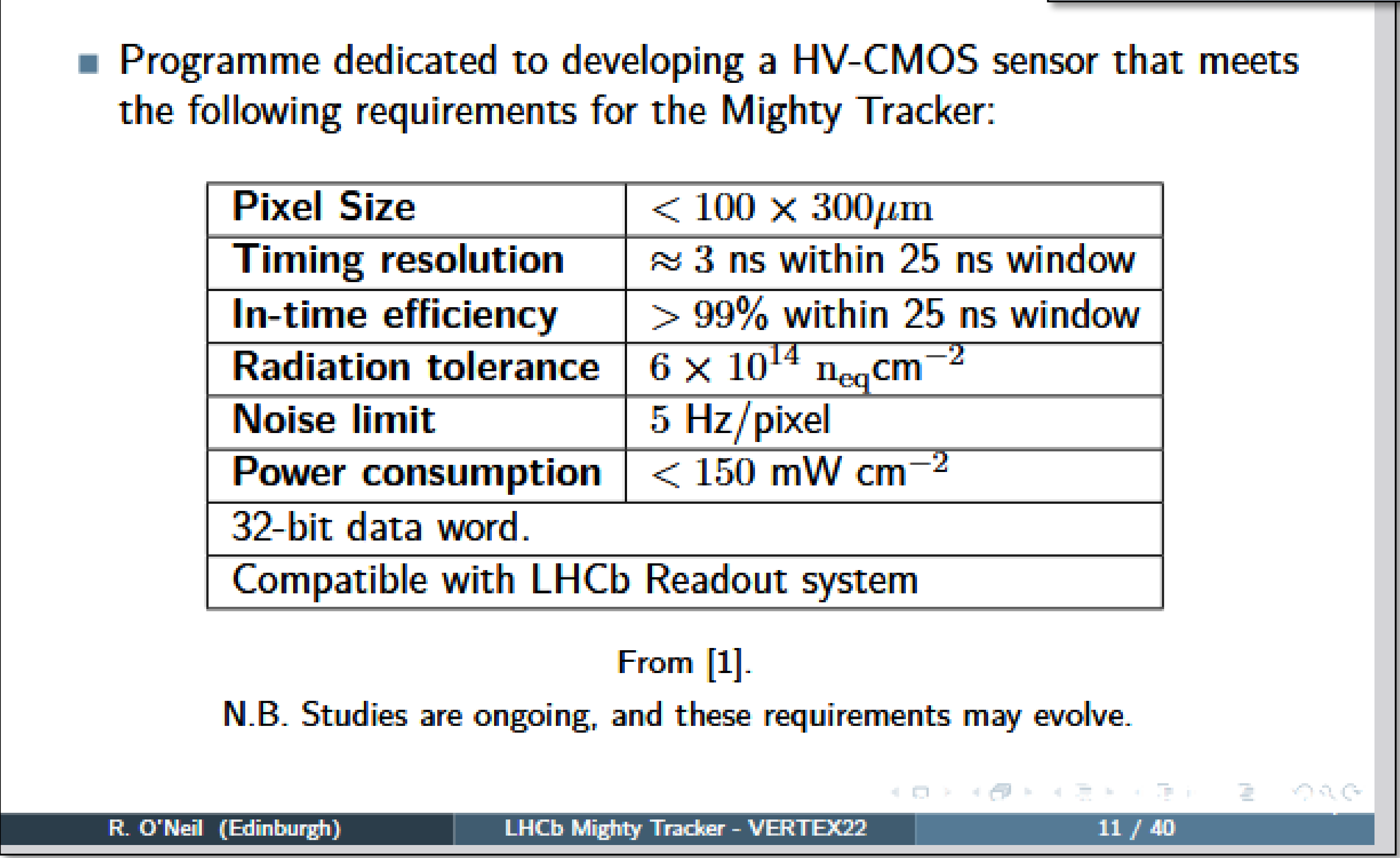
Ryunosuke O'Neil

The University of Edinburgh
r.oneil@cern.ch

on behalf of the LHCb Collaboration and Mighty Tracker Group

25th October 2022
VERTEX 2022, Tateyama, Japan

R. O'Neil (Edinburgh) LHCb Mighty Tracker - VERTEX22 1 / 40



Introduction | The MightyPix and friends

MightyPix R&D: requirements

- Programme dedicated to developing a HV-CMOS sensor that meets the following requirements for the Mighty Tracker:

Pixel Size	$< 100 \times 300\mu m$
Timing resolution	$\approx$ 3 ns within 25 ns window
In-time efficiency	$>$ 99% within 25 ns window
Radiation tolerance	6×10^{14} $n_{eq}cm^{-2}$
Noise limit	5 Hz/pixel
Power consumption	$<$ 150 mW cm^{-2}
32-bit data word.	
Compatible with LHCb Readout system	

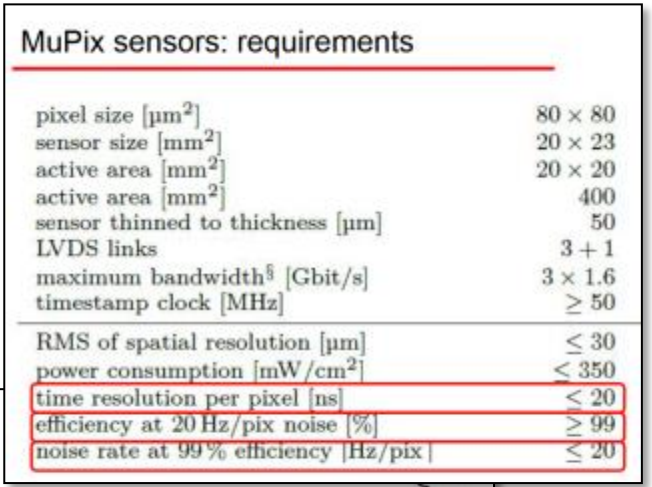
From [1].

N.B. Studies are ongoing, and these requirements may evolve.

R. O'Neil (Edinburgh) LHCb Mighty Tracker - VERTEX22 11 / 40

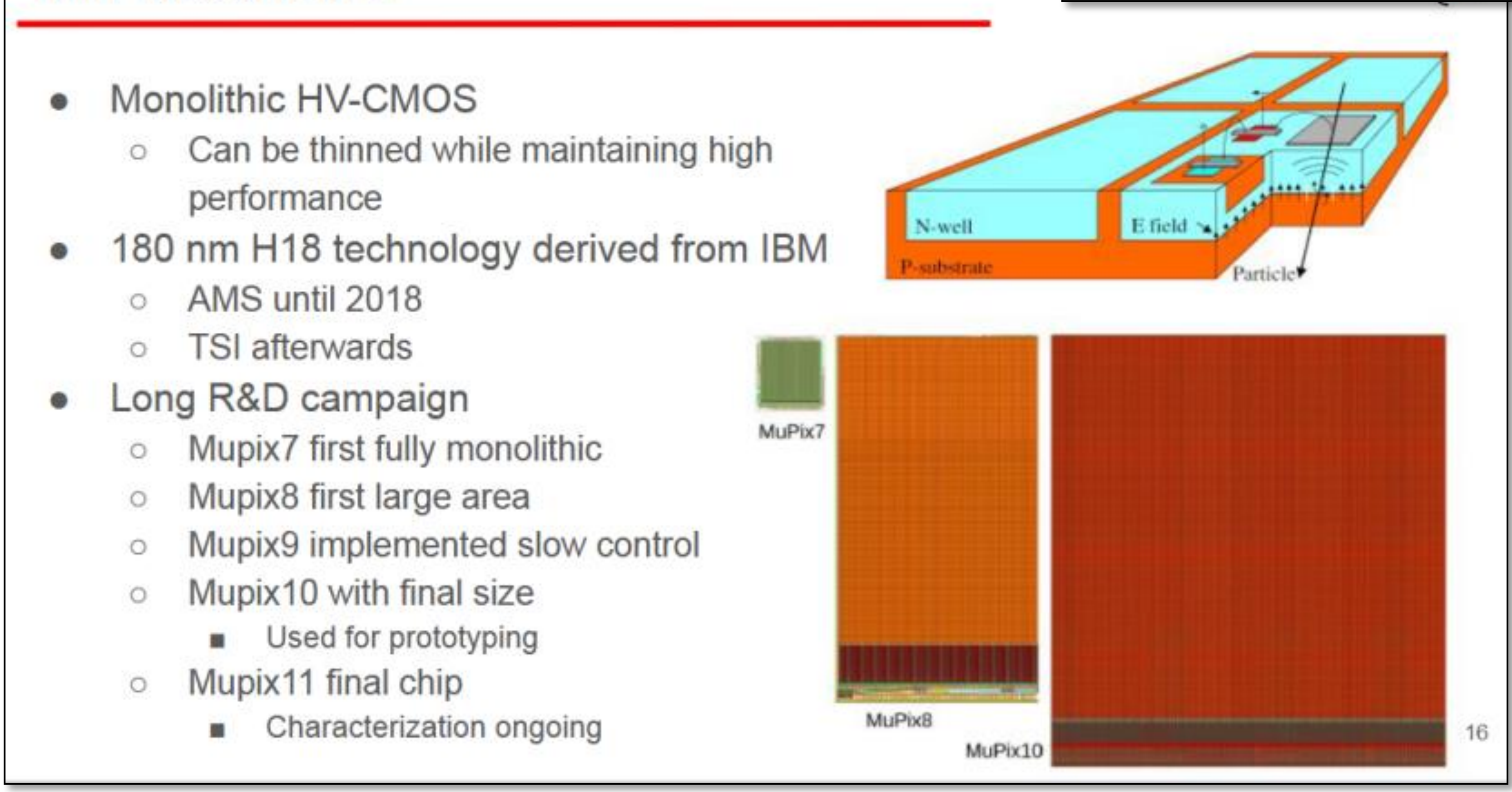
Mupix: Monolithic sensors for the Mu3e experiment

Luigi Vigani
University of Heidelberg
Vertex 2022
25/10/2022



MuPix sensors: requirements

pixel size [μm^2]	80×80
sensor size [mm^2]	20×23
active area [mm^2]	20×20
active area [mm^2]	400
sensor thinned to thickness [μm]	50
LVDS links	$3 + 1$
maximum bandwidth§ [Gbit/s]	3×1.6
timestamp clock [MHz]	≥ 50
RMS of spatial resolution [μm]	$\lesssim 30$
power consumption [mW/cm^2]	$\lesssim 350$
time resolution per pixel [ns]	$\lesssim 20$
efficiency at 20 Hz/pix noise [%]	≥ 99
noise rate at 99 % efficiency [Hz/pix]	$\lesssim 20$



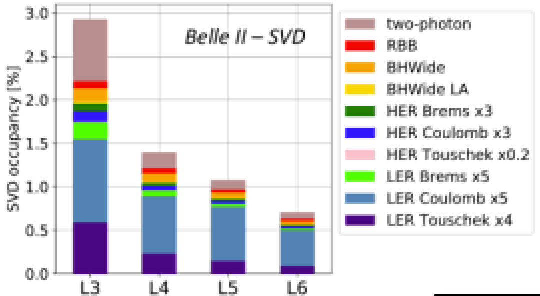
MuPix sensors

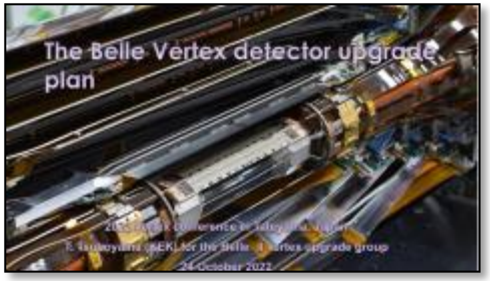
- Monolithic HV-CMOS
  - Can be thinned while maintaining high performance
- 180 nm H18 technology derived from IBM
  - AMS until 2018
  - TSI afterwards
- Long R&D campaign
  - Mupix7 first fully monolithic
  - Mupix8 first large area
  - Mupix9 implemented slow control
  - Mupix10 with final size
    - Used for prototyping
  - Mupix11 final chip
    - Characterization ongoing

16

The Silicon Vertex Detector of the Belle II Experiment

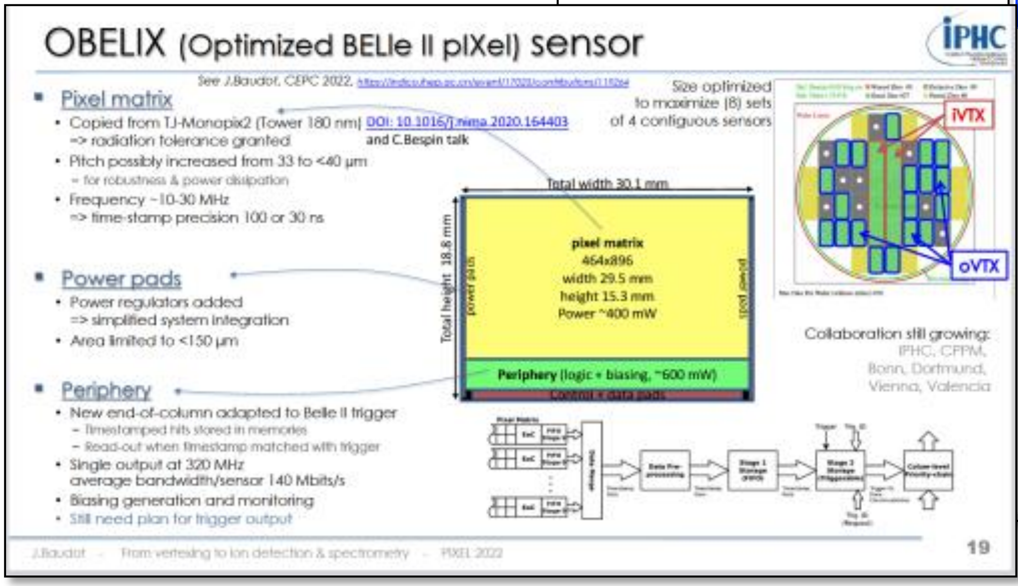
Kookhyun Kang - Kavli IPMU
on behalf of the Belle II SVD Collaboration
VERTEX 2022 Oct 24, 2022





The Belle Vertex detector upgrade plan

2022 VERTEX conference in Tateyama, Japan
T. Tsuboyama (KEK) for the Belle II vertex upgrade group
24 October 2022



OBELIX (Optimized BELle II pIXel) sensor

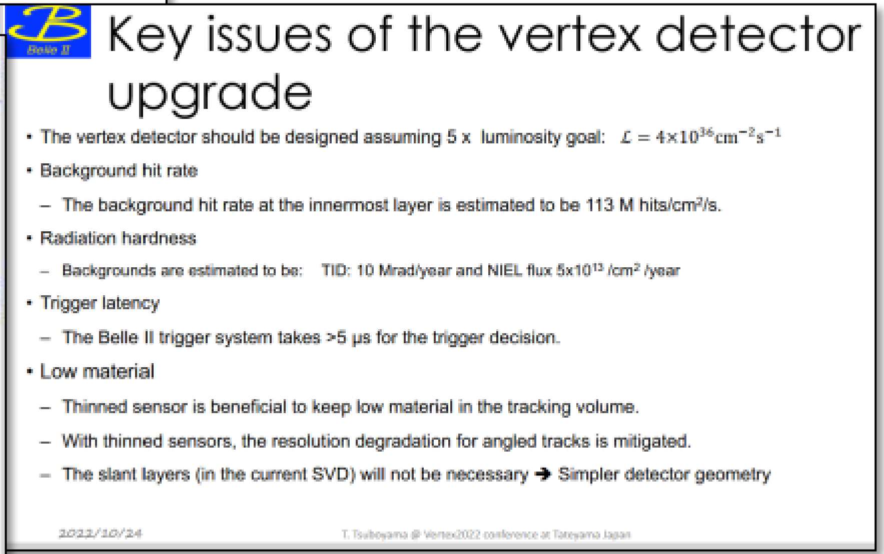
See J.Baudot, CEPC 2022, https://indico.ihep.ac.cn/event/17020/contributions/118264

- Pixel matrix
  - Copied from TJ-Monopix2 (Tower 180 nm) DOI: 10.1016/j.nima.2020.164403 and C.Bespin talk
    => radiation tolerance granted
  - Pitch possibly increased from 33 to <40 µm
    – for robustness & power dissipation
  - Frequency ~10-30 MHz
    => time-stamp precision 100 or 30 ns
- Power pads
  - Power regulators added
    => simplified system integration
  - Area limited to <150 µm
- Periphery
  - New end-of-column adapted to Belle II trigger
    – Timestamped hits stored in memories
    – Read-out when timestamp matched with trigger
  - Single output at 320 MHz
    average bandwidth/sensor 140 Mbits/s
  - Biasing generation and monitoring
  - Still need plan for trigger output

Size optimized to maximize (8) sets of 4 contiguous sensors

Collaboration still growing: IPHC, CPPM, Bonn, Dortmund, Vienna, Valencia

J.Baudot – From vertexing to ion detection & spectrometry – PIXEL 2022 19



Key issues of the vertex detector upgrade

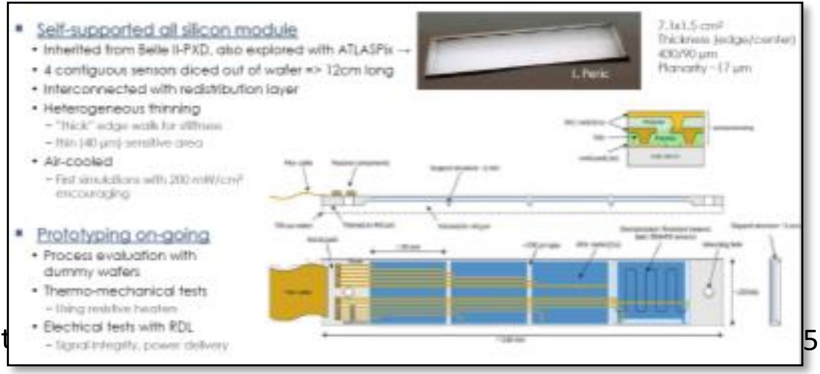
- The vertex detector should be designed assuming 5 x luminosity goal: $\mathcal{L} = 4\times10^{36}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- Background hit rate
  - The background hit rate at the innermost layer is estimated to be 113 M hits/cm²/s.
- Radiation hardness
  - Backgrounds are estimated to be: TID: 10 Mrad/year and NIEL flux 5×10^{13} /cm² /year
- Trigger latency
  - The Belle II trigger system takes >5 µs for the trigger decision.
- Low material
  - Thinned sensor is beneficial to keep low material in the tracking volume.
  - With thinned sensors, the resolution degradation for angled tracks is mitigated.
  - The slant layers (in the current SVD) will not be necessary ➔ Simpler detector geometry

2022/10/24 T. Tsuboyama @ Vertex2022 conference at Tateyama Japan

https://indico.cern.ch/event/1140707/contributions/5036352/attachments/2533480/4359729/tsuboyama-Belle2-vertex-upgrade-S3.pdf

https://indico.cern.ch/event/1140707/contributions/4988213/attachments/2533474/4359608/Vertex2022_khkang_v3.pdf

https://indico.cern.ch/event/829863/contributions/5062886/attachments/2568342/4428391/baudot-pixel2022.pdf



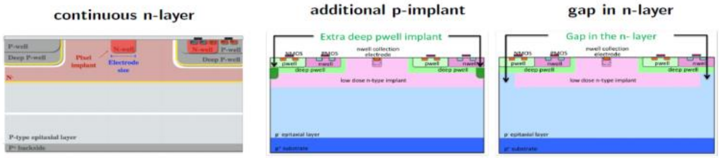
- Self-supported all silicon module
  - Inherited from Belle II-PXD, also explored with ATLASPix →
  - 4 contiguous sensors diced out of wafer => 12cm long
  - Interconnected with redistribution layer
  - Heterogeneous thinning
    – "Thick" edge walls for stiffness
    – thin (40 µm) sensitive area
  - Air-cooled
    – First simulations with 200 mW/cm² encouraging
- Prototyping on-going
  - Process evaluation with dummy wafers
  - Thermo-mechanical tests
    – Using resistive heaters
  - Electrical tests with RDL
    – Signal integrity, power delivery

Example of trade off: MIMOSIS

- MIMOSIS-1 chip for CBM-MVD @ FAIR

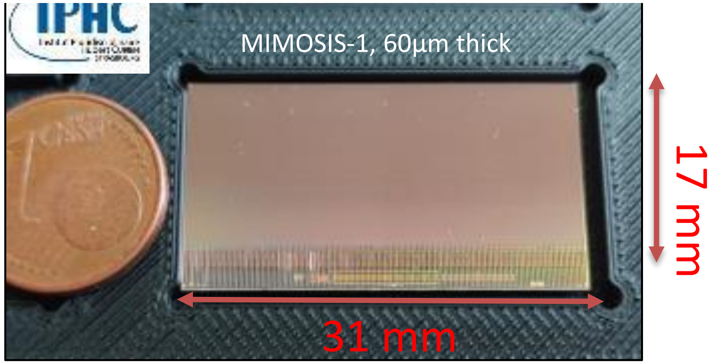
Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	$\sim 25\,\mu\text{m}$
Epi layer resistivity	$> 1 k\Omega cm$
Sensor thickness	$60\,\mu\text{m}$
Pixel size	$26.88\,\mu\text{m} \times 30.24\,\mu\text{m}$
Matrix size	1024×504 (516096 pix)
Matrix area	$\approx 4.2\,\text{cm}^2$
Matrix readout time	$5\,\mu\text{s}$ (event driven)
Power consumption	$40\text{-}70\,\text{mW/cm}^2$

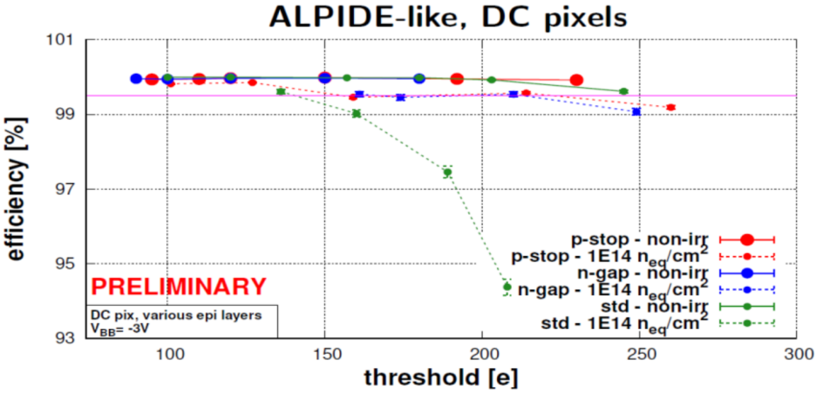
- ✓ Based on ALPIDE architecture
  - Multiple data concentration steps
  - Elastic output buffer
  - 8 x 320 Mbps links (switchable)
  - Triple redundant electronics
- ✓ Pixel variants: DC/AC (top bias up to >20V)
- ✓ Different epitaxial variants tested

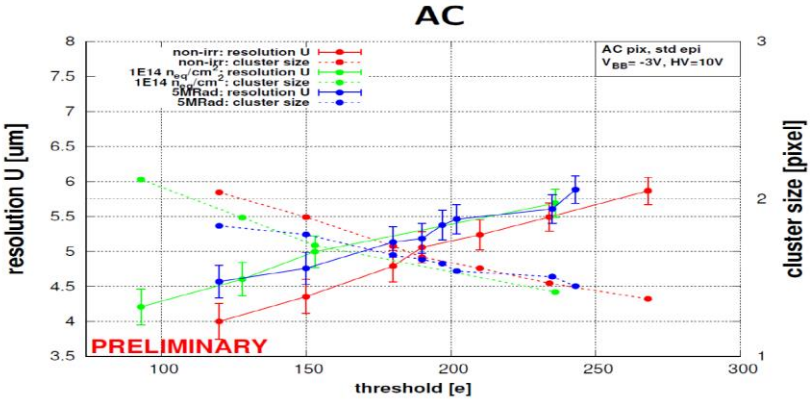


Pic from: Munker, Vertex 2018, Status of silicon detector R&D at CLIC
Carlos, TREDI 2019, Results of the Malta CMOS pixel detector prototype for the ATLAS Pixel ITK

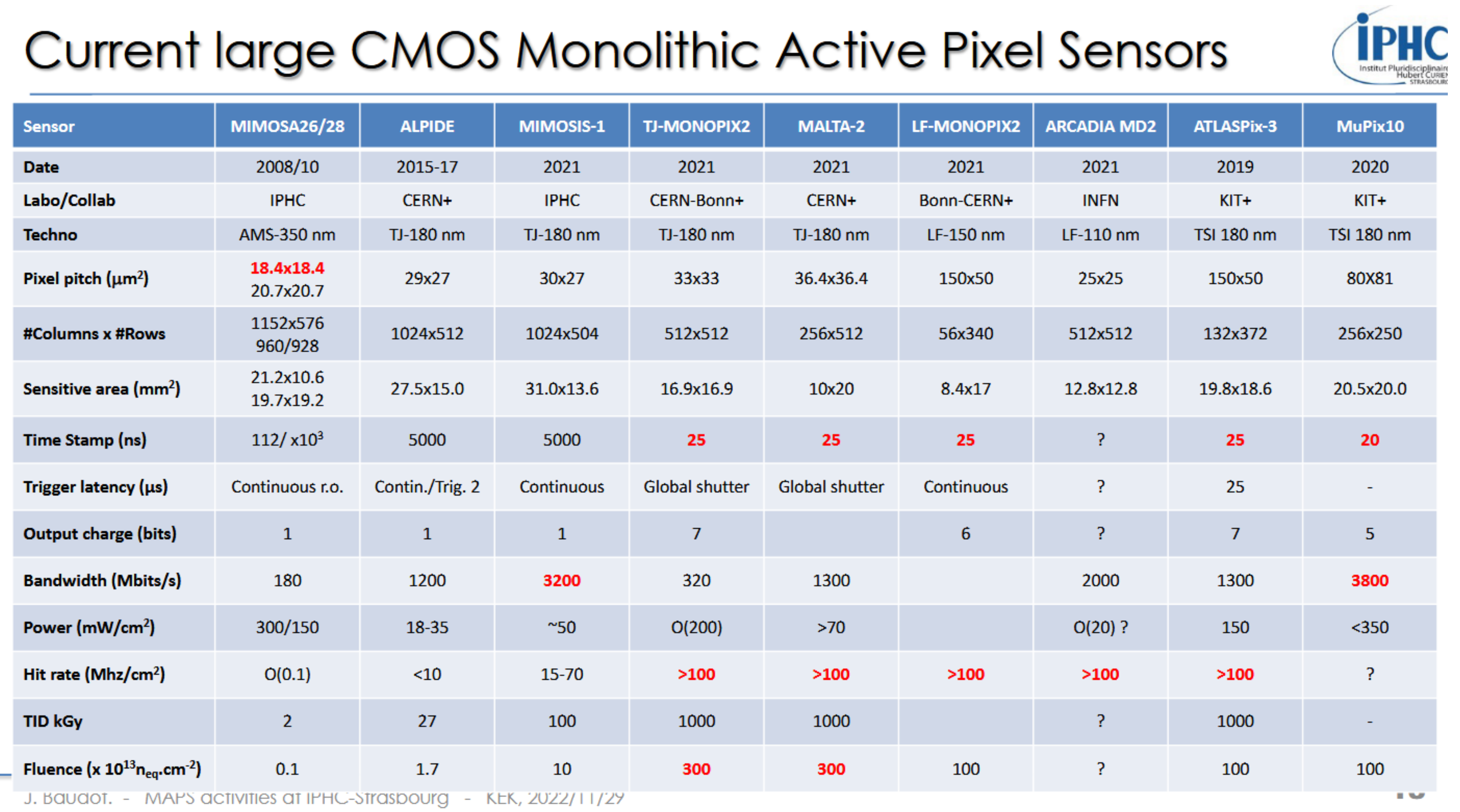
- Intense test beam campaign(2021-22)
  - ✓ Mimosis-2 submission these weeks
    - Thicker epi layer tests
    - Test prototype for 1 µs readout time





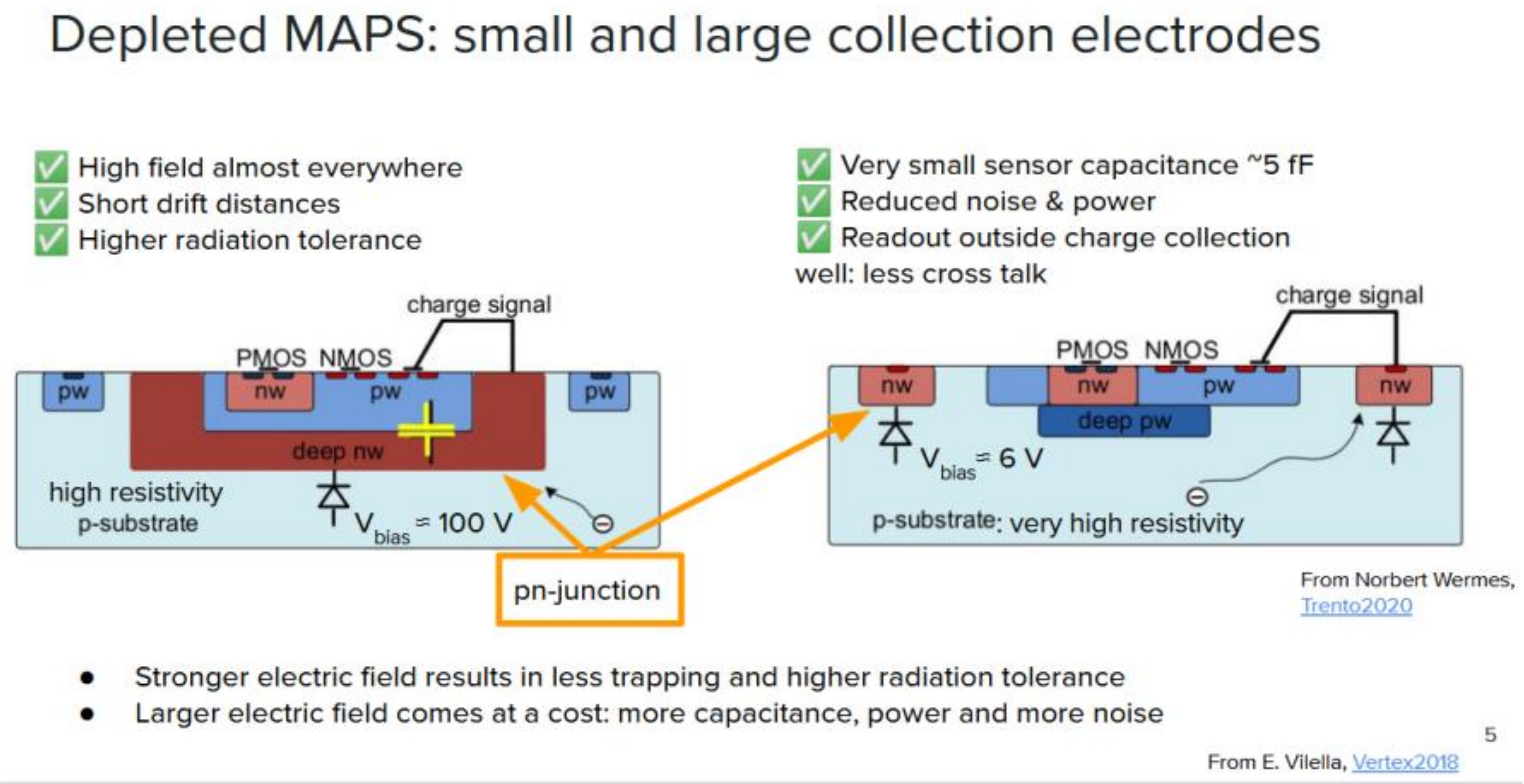


`MIMOSIS = a milestone for Higgs factories (5 µm / ≤5 µs)`



Current large CMOS Monolithic Active Pixel Sensors

Sensor	MIMOSA26/28	ALPIDE	MIMOSIS-1	TJ-MONOPIX2	MALTA-2	LF-MONOPIX2	ARCADIA MD2	ATLASPix-3	MuPix10
Date	2008/10	2015-17	2021	2021	2021	2021	2021	2019	2020
Labo/Collab	IPHC	CERN+	IPHC	CERN-Bonn+	CERN+	Bonn-CERN+	INFN	KIT+	KIT+
Techno	AMS-350 nm	TJ-180 nm	TJ-180 nm	TJ-180 nm	TJ-180 nm	LF-150 nm	LF-110 nm	TSI 180 nm	TSI 180 nm
Pixel pitch (μm^2)	**18.4x18.4** 20.7x20.7	29x27	30x27	33x33	36.4x36.4	150x50	25x25	150x50	80X81
#Columns x #Rows	1152x576 960/928	1024x512	1024x504	512x512	256x512	56x340	512x512	132x372	256x250
Sensitive area (mm^2)	21.2x10.6 19.7x19.2	27.5x15.0	31.0x13.6	16.9x16.9	10x20	8.4x17	12.8x12.8	19.8x18.6	20.5x20.0
Time Stamp (ns)	112/ x10^3	5000	5000	**25**	**25**	**25**	?	**25**	**20**
Trigger latency (μs)	Continuous r.o.	Contin./Trig. 2	Continuous	Global shutter	Global shutter	Continuous	?	25	-
Output charge (bits)	1	1	1	7		6	?	7	5
Bandwidth (Mbits/s)	180	1200	**3200**	320	1300		2000	1300	**3800**
Power (mW/cm^2)	300/150	18-35	~50	O(200)	>70		O(20) ?	150	<350
Hit rate (Mhz/cm^2)	O(0.1)	<10	15-70	**>100**	**>100**	**>100**	**>100**	**>100**	?
TID kGy	2	27	100	1000	1000		?	1000	-
Fluence (x 10^{13}n$_{eq}$.cm^{-2})	0.1	1.7	10	**300**	**300**	100	?	100	100



Depleted MAPS: small and large collection electrodes

- ✅ High field almost everywhere
- ✅ Short drift distances
- ✅ Higher radiation tolerance

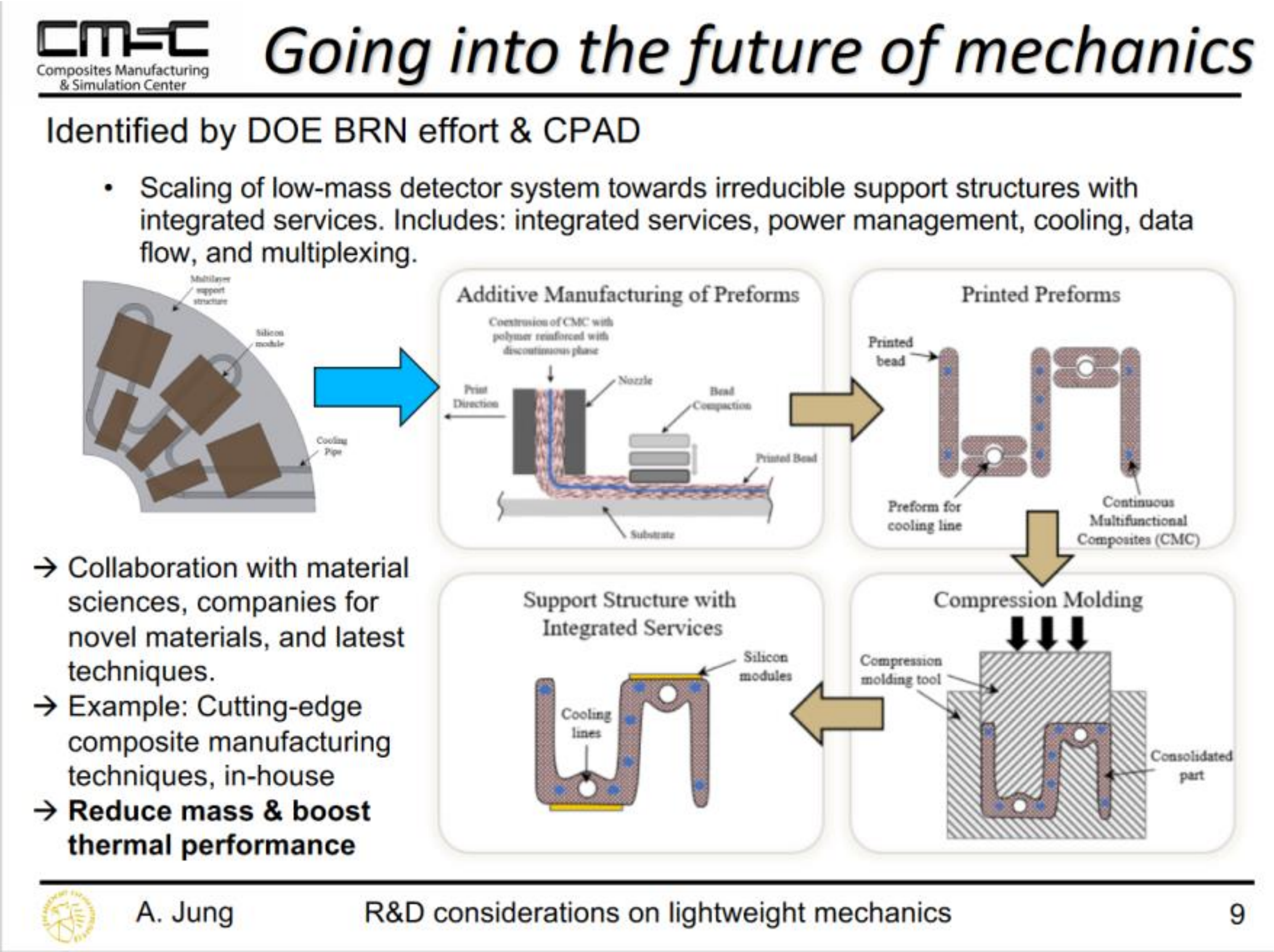
- ✅ Very small sensor capacitance ~5 fF
- ✅ Reduced noise & power
- ✅ Readout outside charge collection well: less cross talk

From Norbert Wermes, Trento2020

- Stronger electric field results in less trapping and higher radiation tolerance
- Larger electric field comes at a cost: more capacitance, power and more noise

From E. Vilella, Vertex2018

Mechanics



Going into the future of mechanics

Identified by DOE BRN effort & CPAD

- Scaling of low-mass detector system towards irreducible support structures with integrated services. Includes: integrated services, power management, cooling, data flow, and multiplexing.

Additive Manufacturing of Preforms

Printed Preforms

Compression Molding

Support Structure with Integrated Services

→ Collaboration with material sciences, companies for novel materials, and latest techniques.

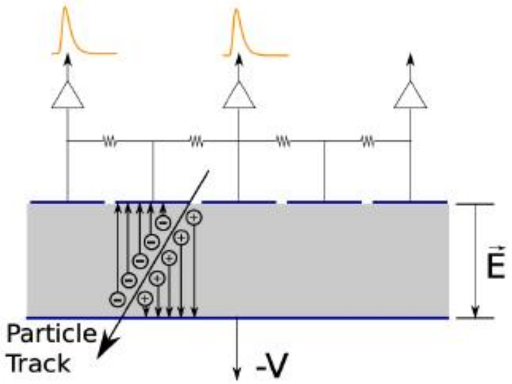
→ Example: Cutting-edge composite manufacturing techniques, in-house

→ **Reduce mass & boost thermal performance**

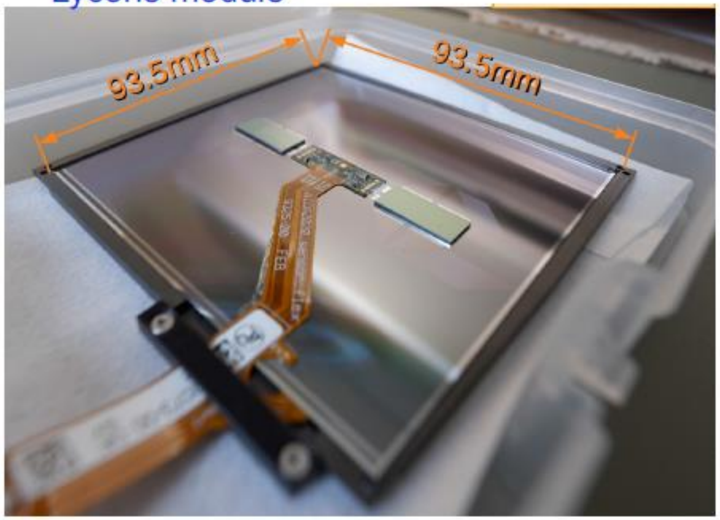
A. Jung R&D considerations on lightweight mechanics 9

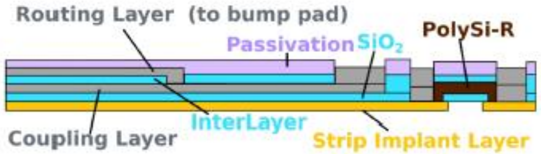
Hybrid strip detectors

Hybrid strip detectors:
- baseline for ILC trackers (also suitable for CLIC outer layers)
- Well-established technology (e.g. HL-LHC)
  - low material + power (sparse readout)
  - large and fast signals (dE/dx)
  - high spatial resolution (charge interpolation) in R/phi direction
  - Allows for testing of advanced sensor concepts (e.g. stitched passive CMOS strip sensors)
  - Challenges: not for high occupancy regions; complex interconnect

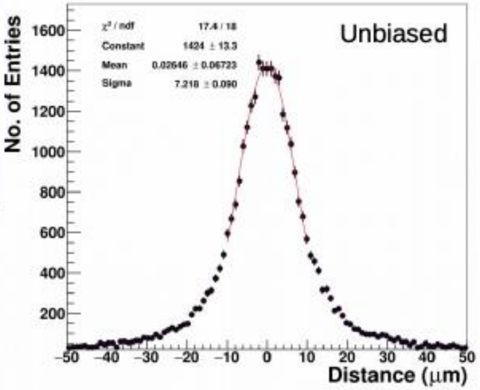


Lycoris module



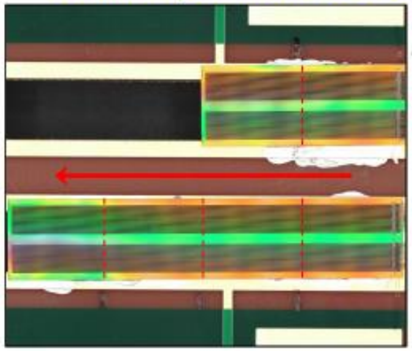


- Lycoris development DESY / SLAC:
  - 320 µm thick SiD strip sensors, 25 µm pitch
  - KPiX r/o ASIC
  - Chip bump-bonded on-sensor → high fill factor
  - 7 µm single-point resolution achieved in test beam
  - Test-case: beam telescope for PCMAG@DESY



https://indico.cern.ch/event/995633/contributions/4259345/attachments/2210031/3740113/LCWS_2021.pdf

Stitched passive CMOS sensors



Freiburg,
DESY,
Bonn

https://indico.cern.ch/event/995633/contributions/4259384/attachments/2209268/3738710/Passive%20CMOS%20Strip%20Sensors.pdf

Dominik Dannheim (CERN)