ALICE Silicon Detectors

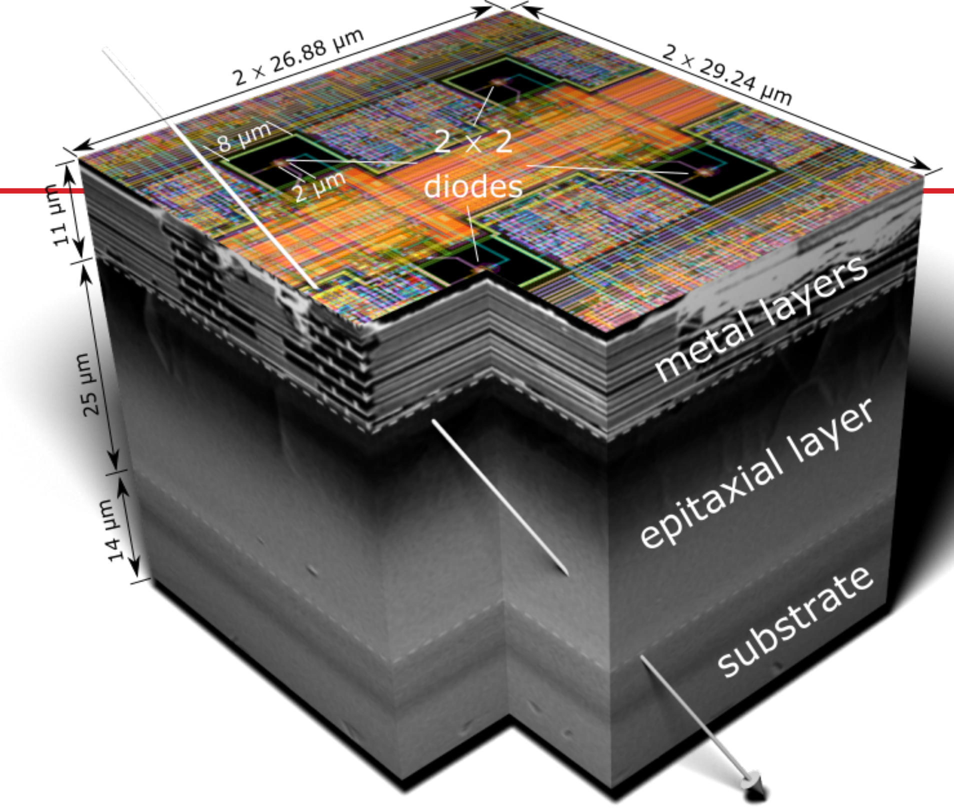
Monolithic Active Pixel Sensor from ITS2 via ITS3 to ALICE3

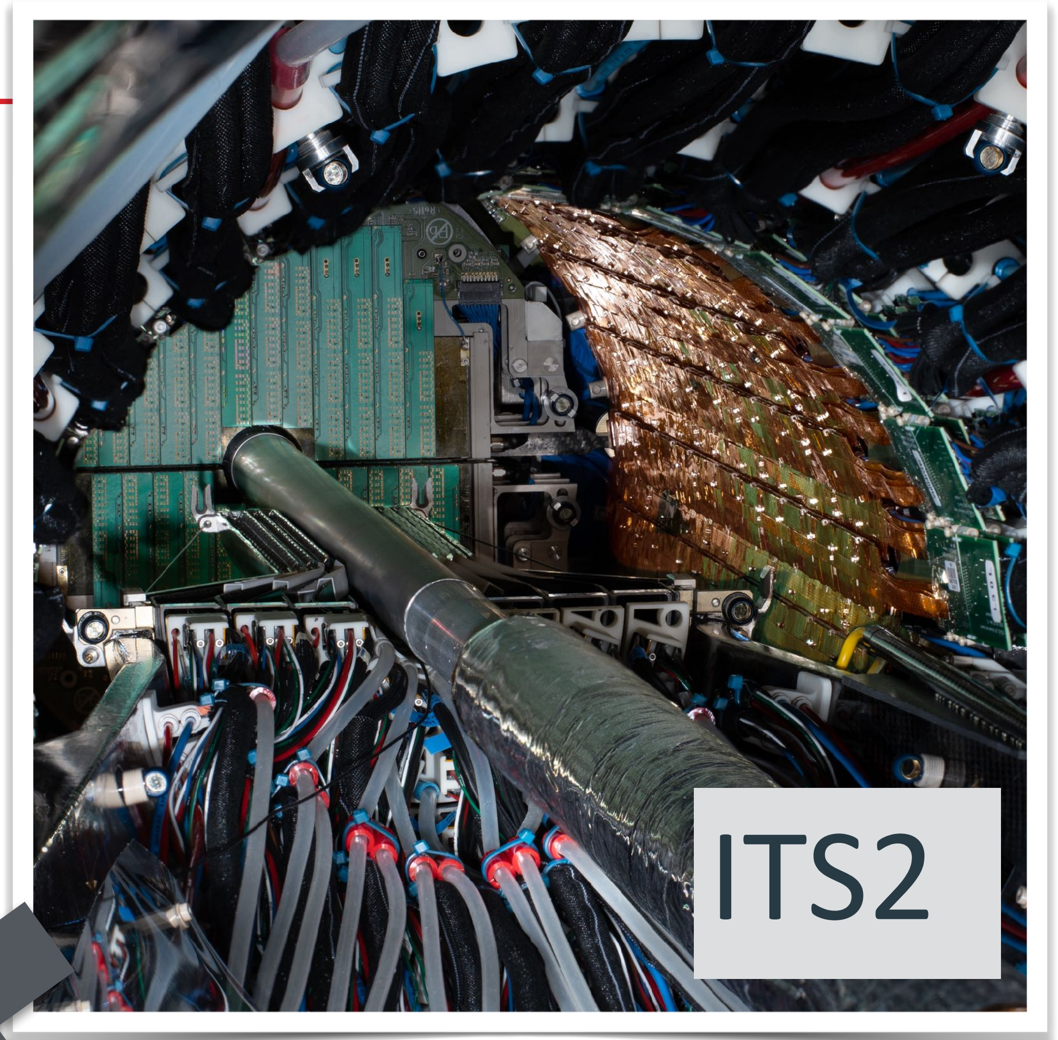
Felix Reidt (CERN)

Lecture, June 28th, 2023

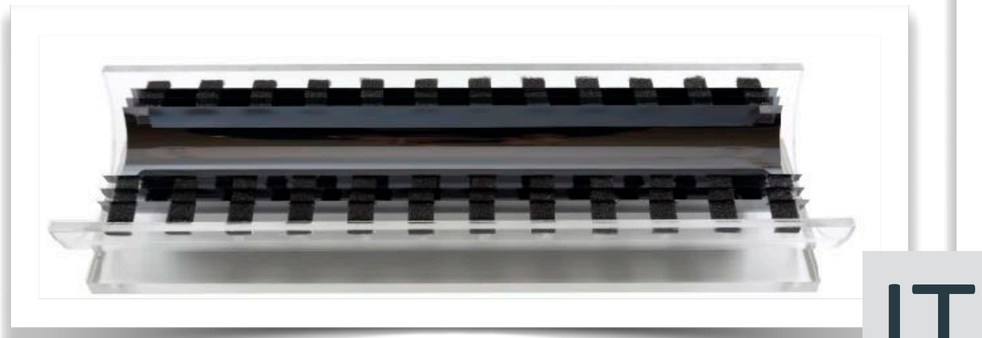
Outline

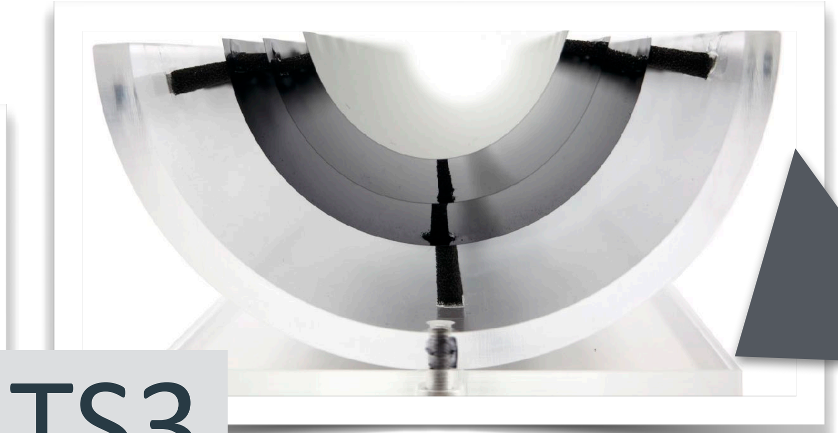
- Introduction to Silicon Detectors
- Inner Tracking System 2 (ITS2)
- Inner Tracking System 3 (ITS3)
- ALICE 3
  Vertex Detector
  and Tracking Detectors



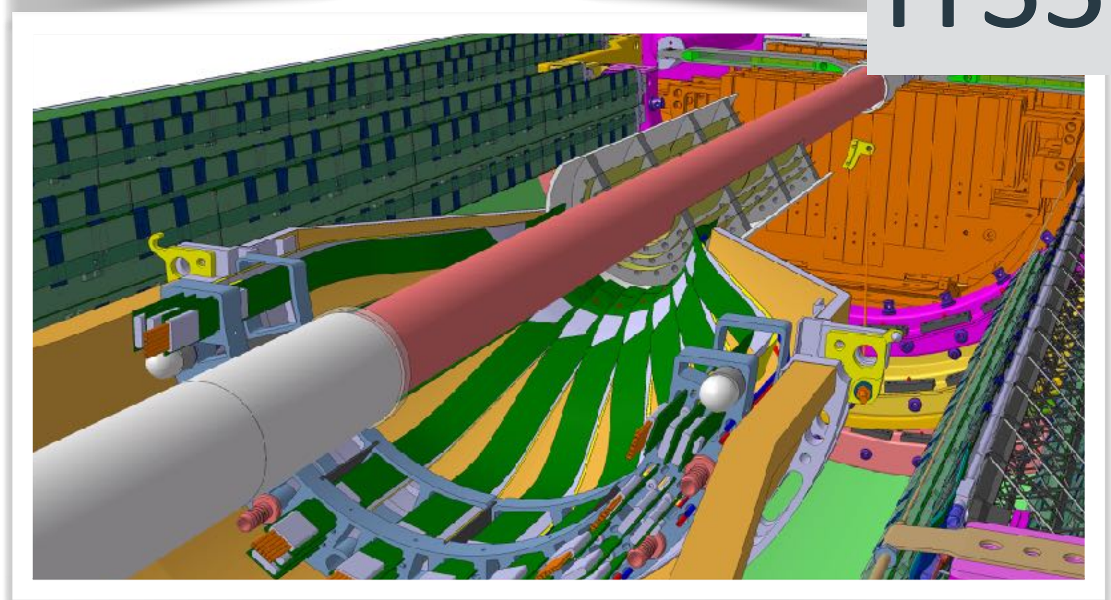


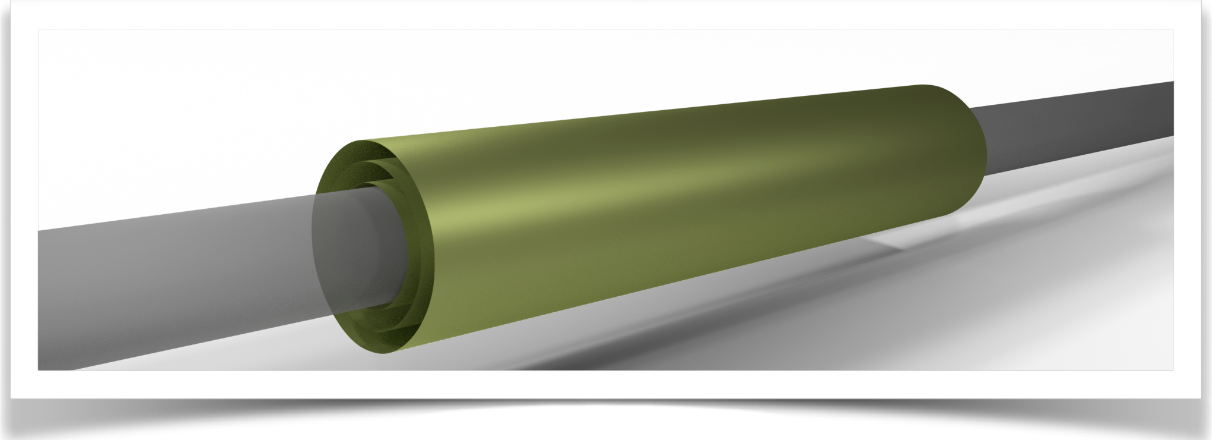
ITS2

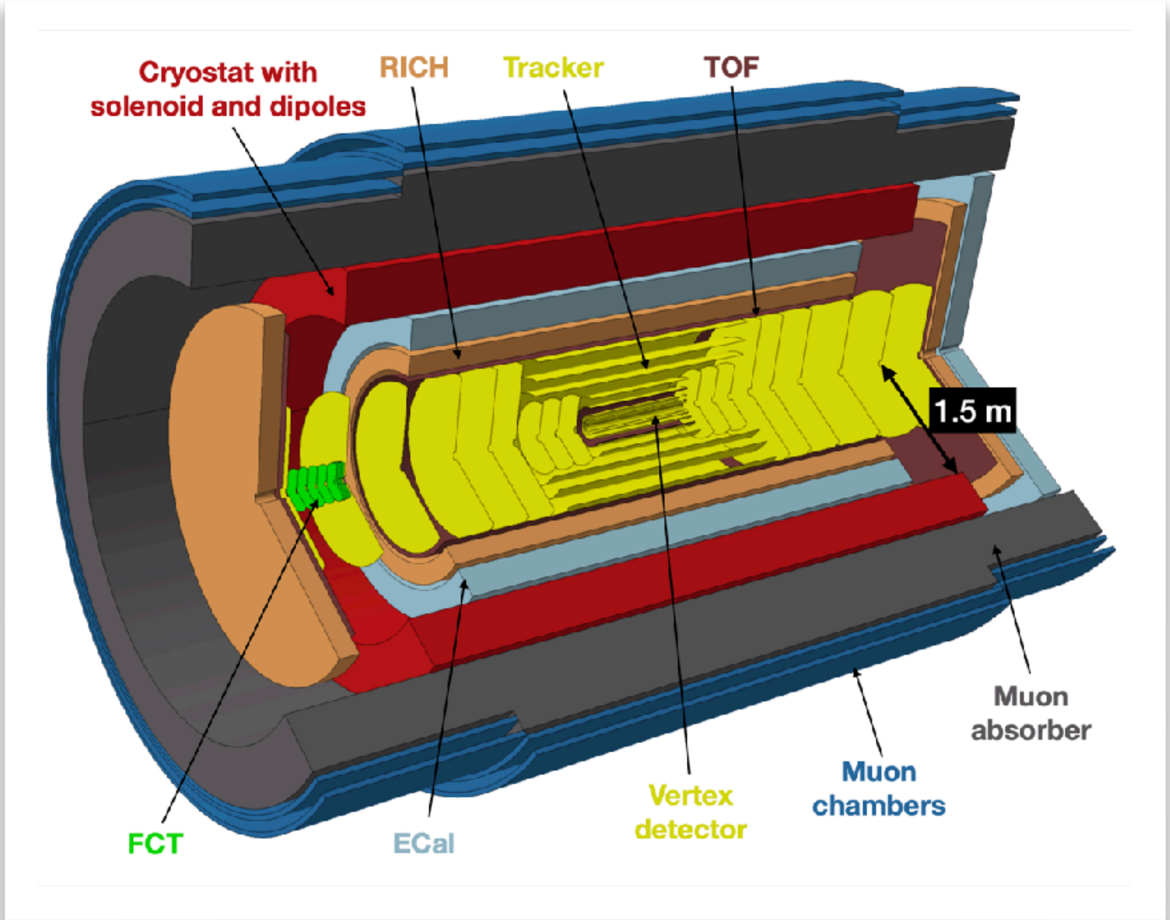




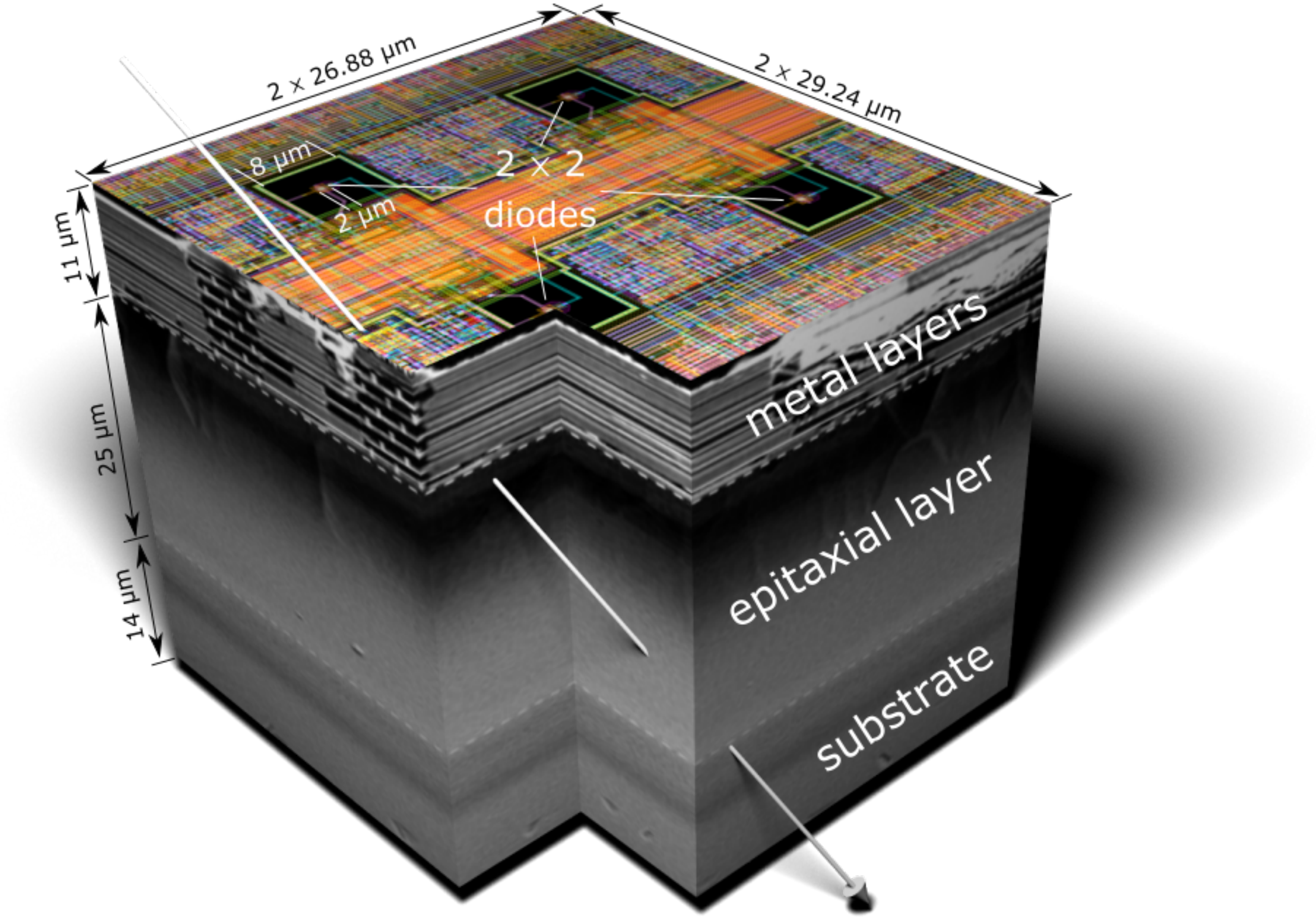
ITS3







ALICE3



Introduction to Silicon Detectors

Silicon Detectors in ALICE*

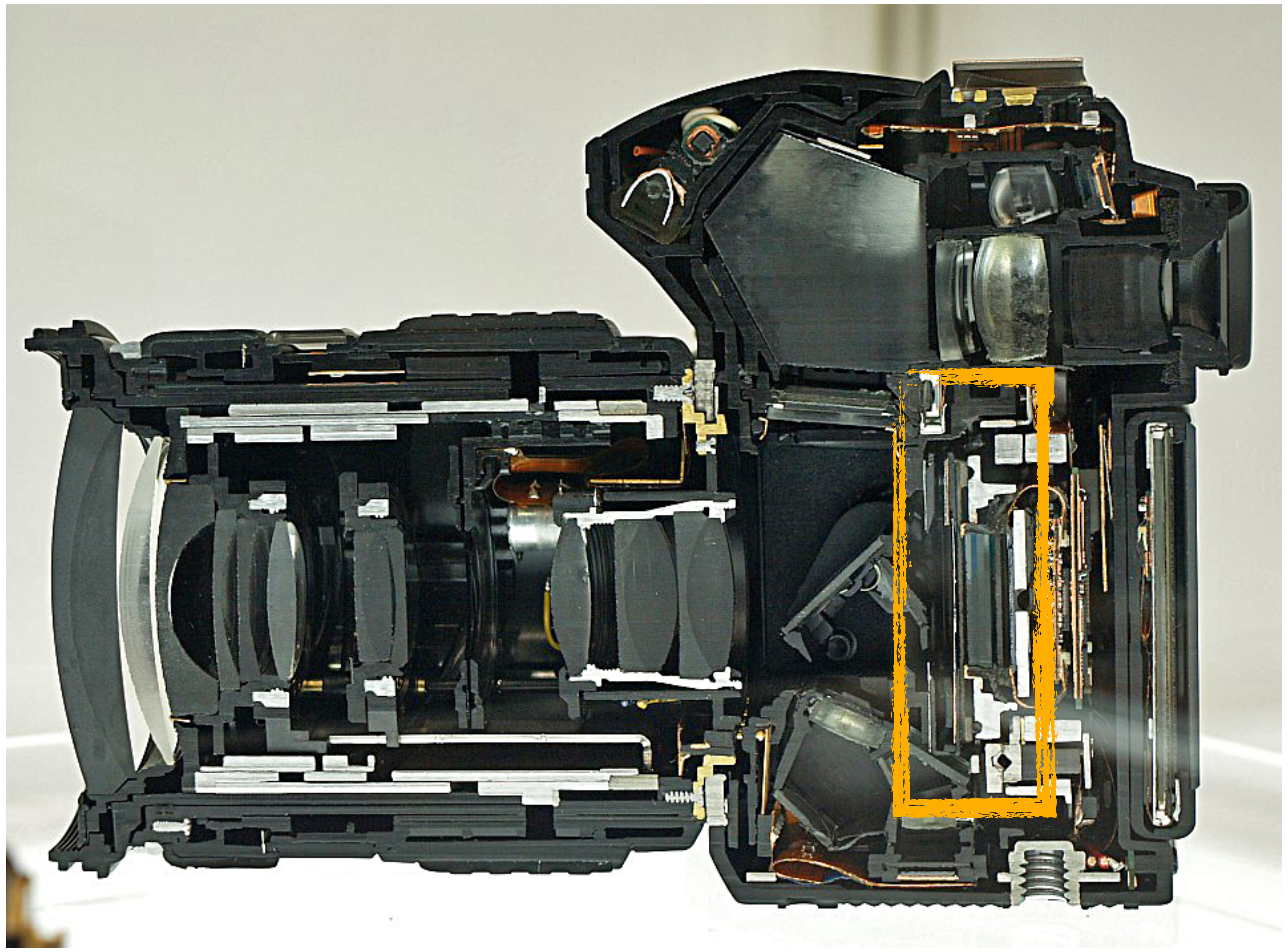
- Detectors closest to the interaction point
- Purpose:
  - Vertex reconstruction
  - Tracking
- Technology used in ALICE:
  Monolithic Active Pixel Sensors (MAPS)

* and in heavy-ion physics and particle physics experiments in general

Pixel detectors

… are nowadays present *everywhere*

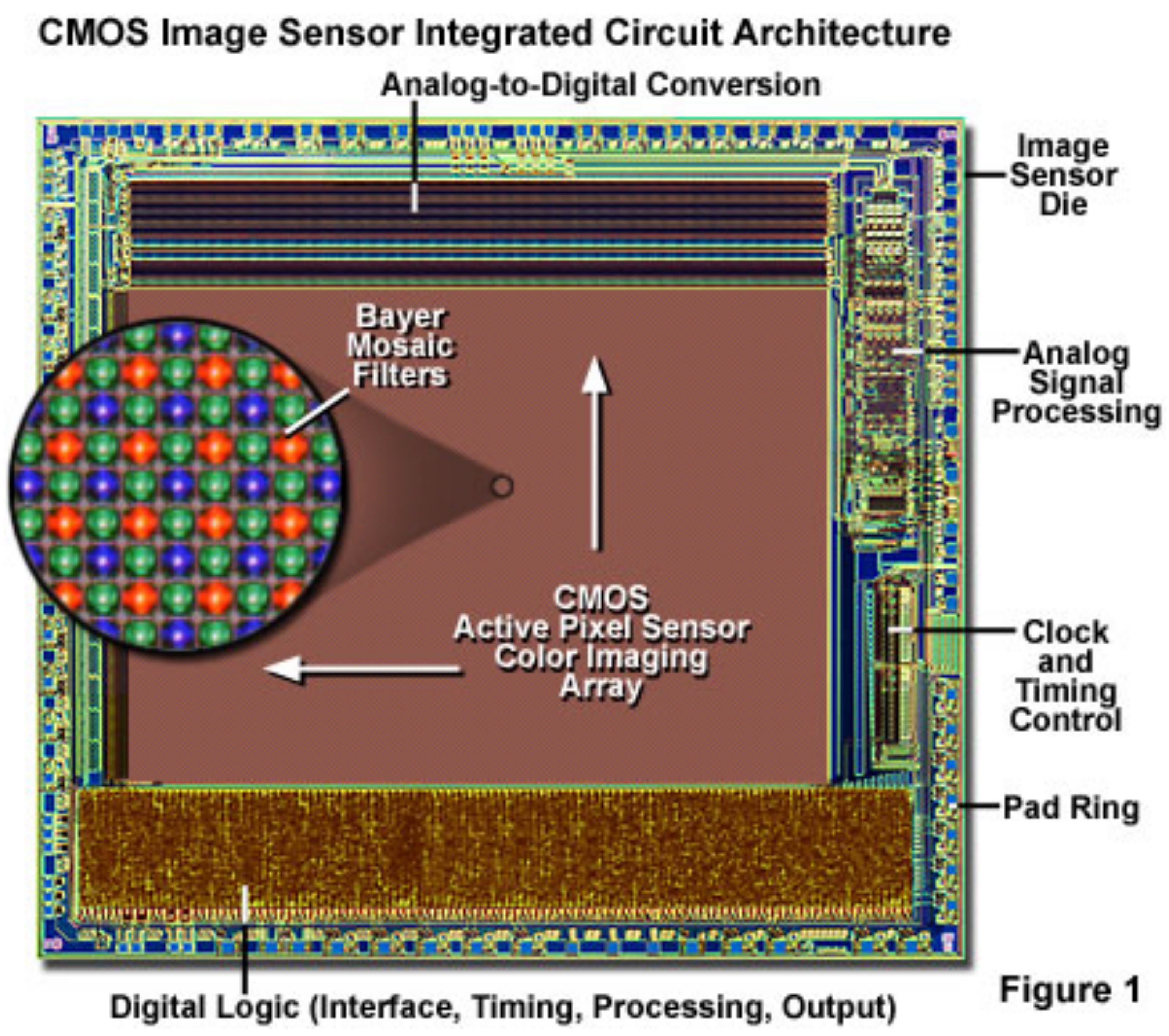
Nobel Prize in Physics 2009
Willard S. Boyle and George E. Smith
"for the invention of an imaging semiconductor circuit – the CCD sensor."

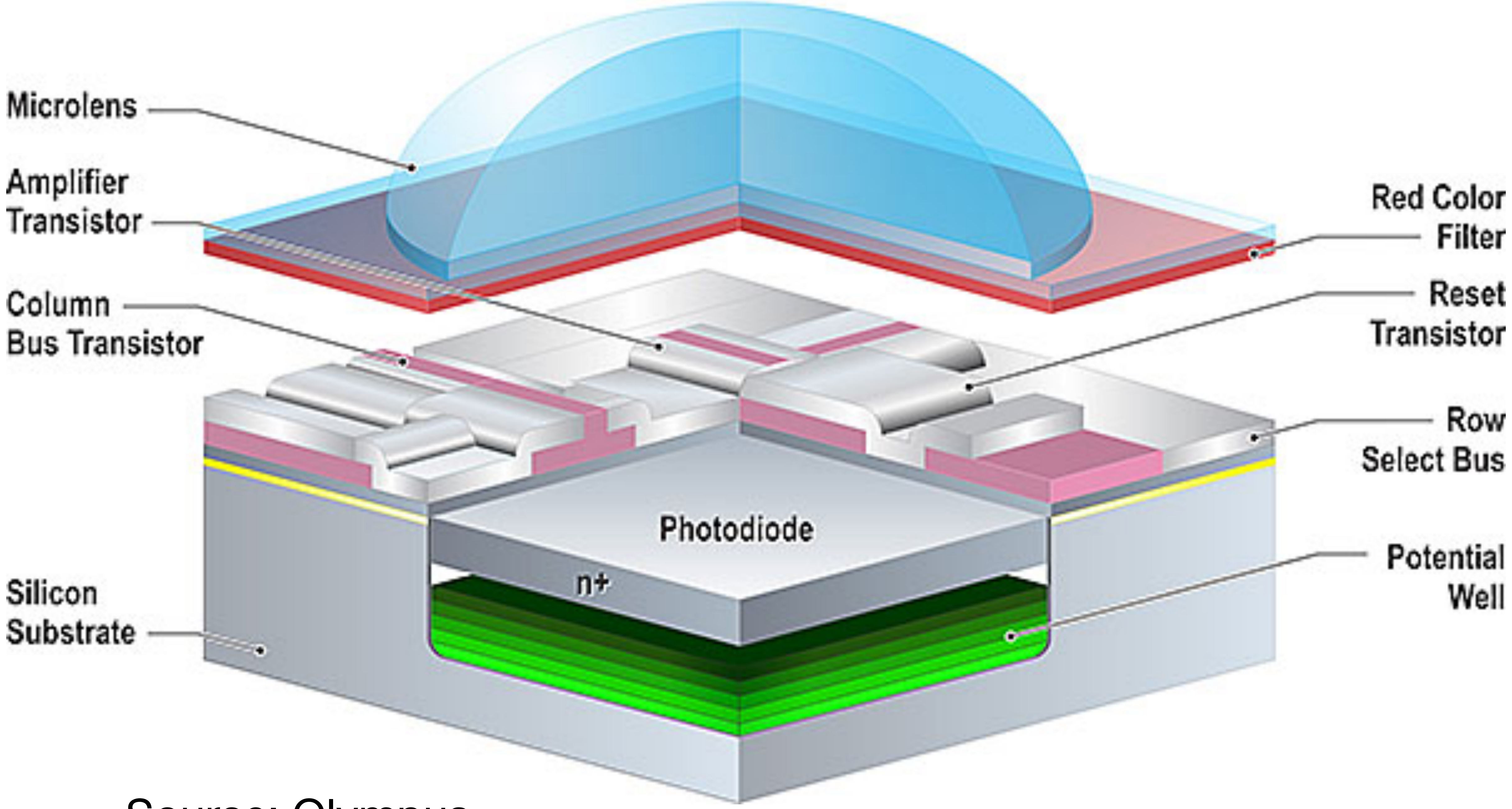


[https://commons.wikimedia.org/wiki/File:E-30-Cutmodel.jpg]

Cut through a modern DSLR
Pixel detectors are abundant (smartphones, surveillance, etc.)
though mostly for (visible) light

CMOS Image Sensors





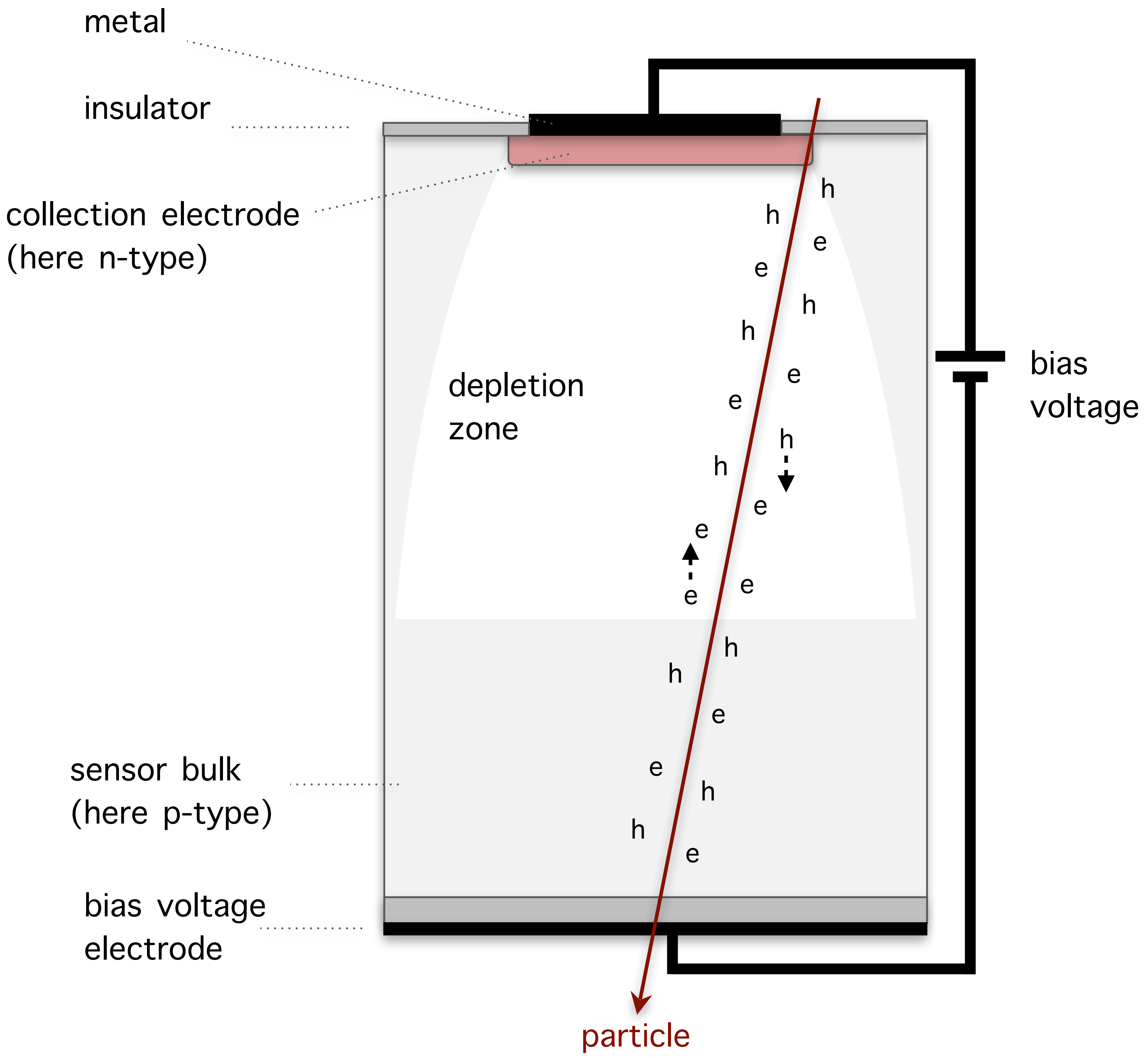
Source: Olympus

- Nowadays the most widespread implementation of image sensors
  - main advantage: price

- Light vs charged particles:
  - both generate electron/hole pairs
  - need to increase sensitive area to 100% (no focussing lenses for charged particles)

Silicon Pixel Detectors — In a nutshell

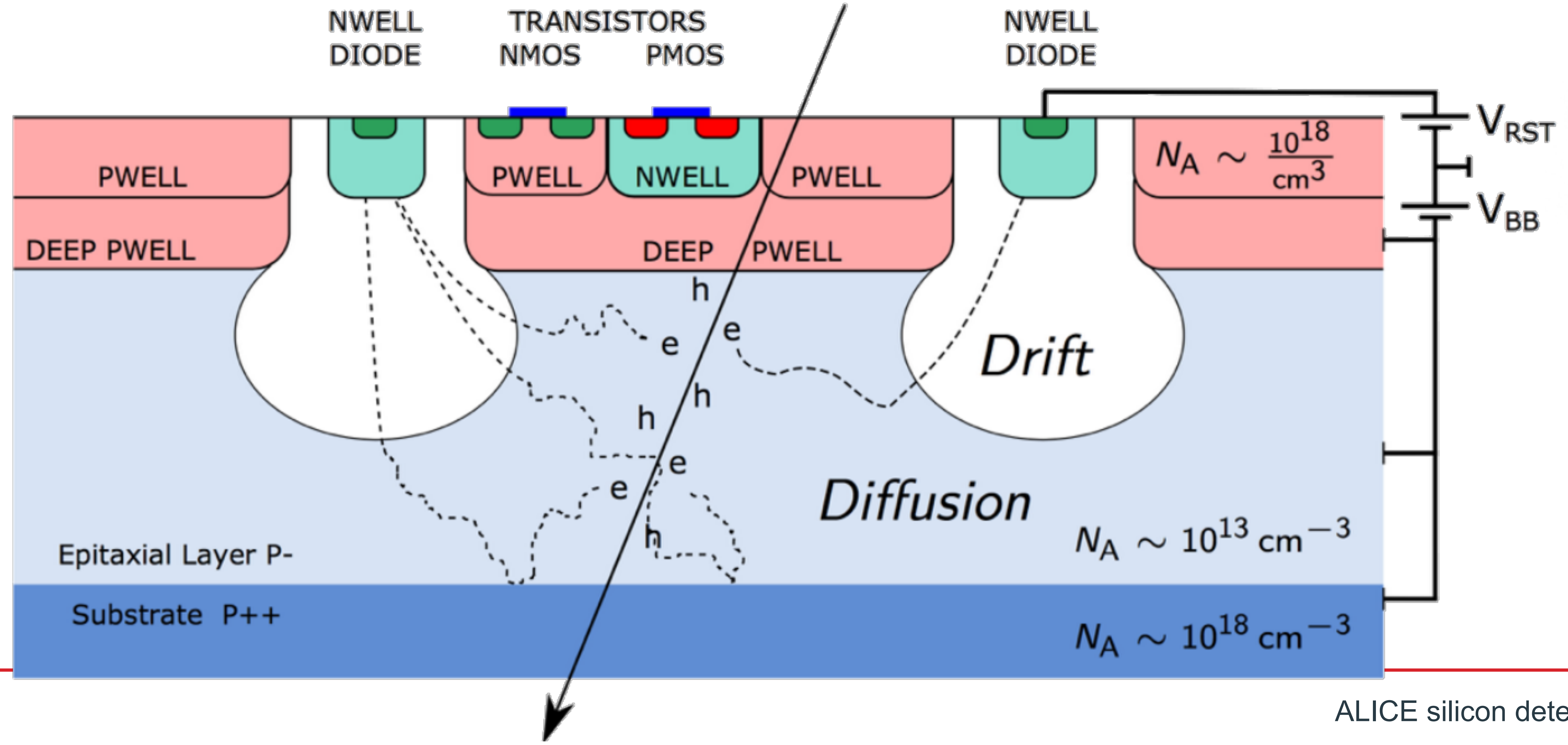
- Semiconductor detectors based doped silicon (Si)
- Operated as solid state ionisation chambers
  - Sensor based on reverse-biased p-n junction
  - Traversing particle ionises the sensor volume: generates electron-hole (e-h) pairs
  - Charges drift to the electrodes inducing a signal
- Key properties
  - High density → large energy loss in a short distance
  - Low ionisation energy of few eV per e-h pair
    (e-ion in gas detectors 10x more expensive)
  - Small patterns possible
    → position resolution below 10 μm reachable
    → high granularity leads to large channel counts, power consumption and in turn cost
  - Easy integration with readout electronics: same materials, very similar technology:
  - High cost per surface unit
- Large experience with semiconductors in the micro-chip industry

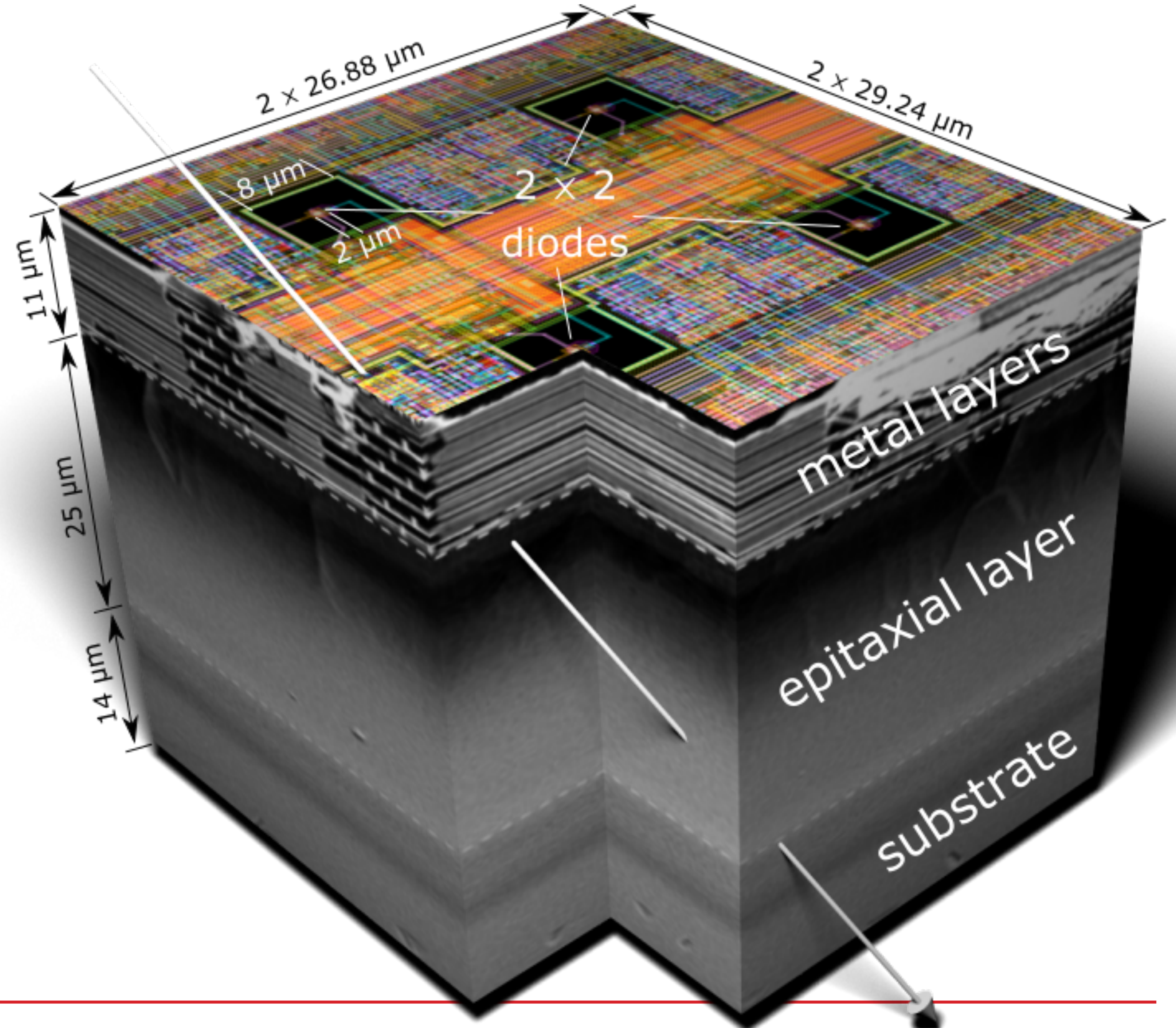


R.L. Workman *et al.* (Particle Data Group), Prog. Theor. Exp. Phys. **2022**, 083C01 (2022)
Review of Particle Physics, Chapter 34 ‘Passage of particles through matter’
L. Rossi, P. Fischer, T. Rohe, N. Wermes, Pixel Detectors
H. Kolanoski and N. Hermes, Particle Detectors - fundamentals and applications

Monolithic Active Pixel Sensors (MAPS)

- Single silicon chip contains both the detection volume and the readout electronics
  - as opposed to hybrid pixel sensors, which use two chips that need to be interconnected
- Advantages:
  - small pixel pitches: O(10-30 μm)
  - very low capacitances = low power O(10-100 mW/cm^2)
  - thin: <50 μm (0.05% X_0)
  - commercial process





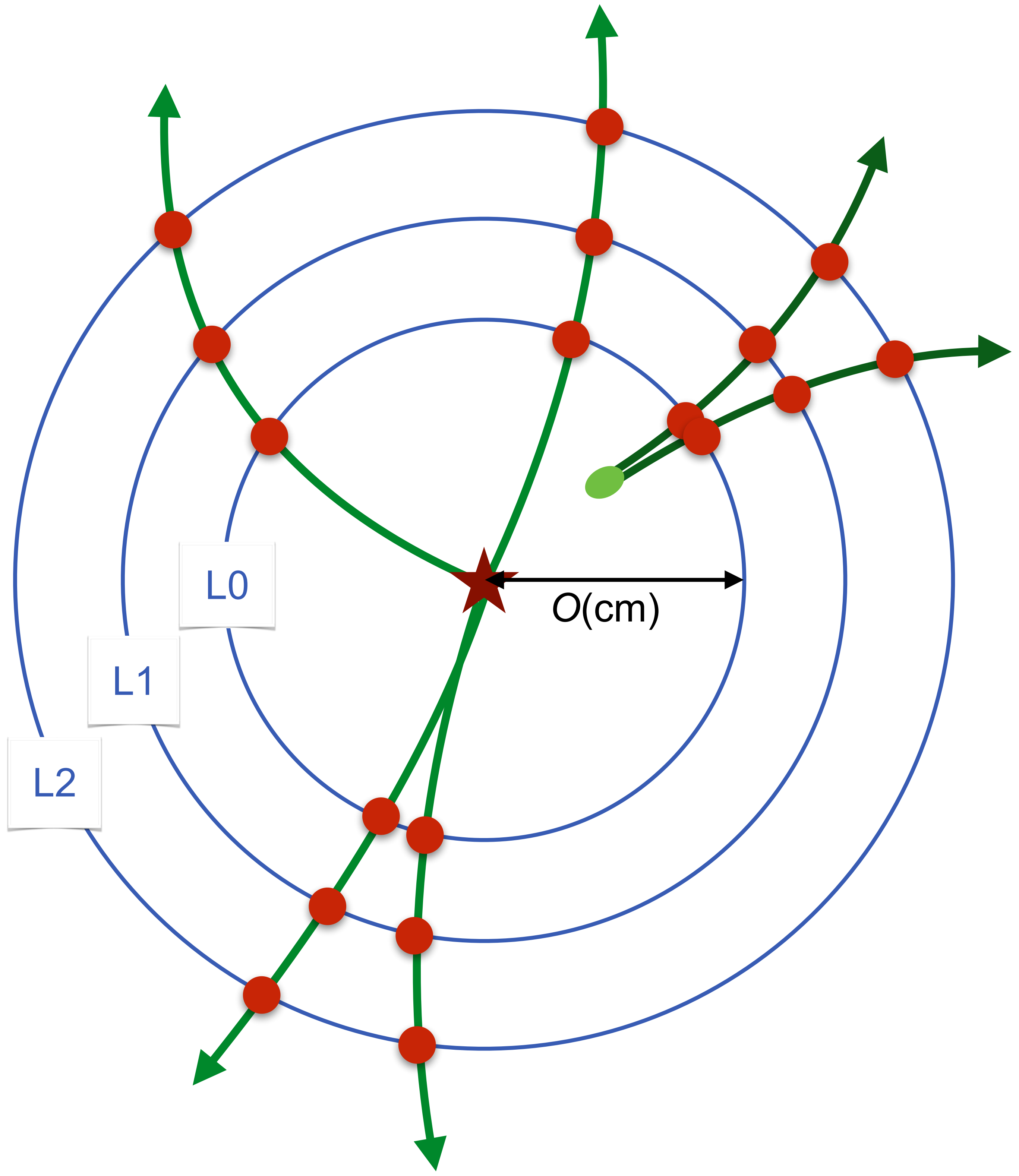
Main objectives of silicon pixel detectors

- **Vertex reconstruction**
  - Identification of primary and decay vertices
  - *Pointing resolution*:
    - low-p_T, multiple scattering regime (key for ALICE): $\sigma_{\text{pointing}} \propto r_0 \cdot \sqrt{x/X_0}$
    - high p_T: $\sigma_{\text{pointing}} \propto \sigma_{\text{pos}}$
  - Crucial to minimise radius and material of first layer (including the beam pipe)

- **Tracking and momentum measurement**
  - Measurement of space points in magnetic field
  - *Momentum resolution:*
    - limited by multiple scattering and lever arm: $\sigma_p/p \propto \frac{\sqrt{x/X_0}}{B \cdot L}$

      → maximise lever arm and magnetic field, minimise material
    - Linear contribution from position resolution of hit measurements: $\sigma_p/p \propto \frac{\sqrt{x/X_0}}{B \cdot L^2} \cdot p$

      → should be sub-dominant in region of interest



Schematic drawing of the reconstruction of a primary and secondary vertex

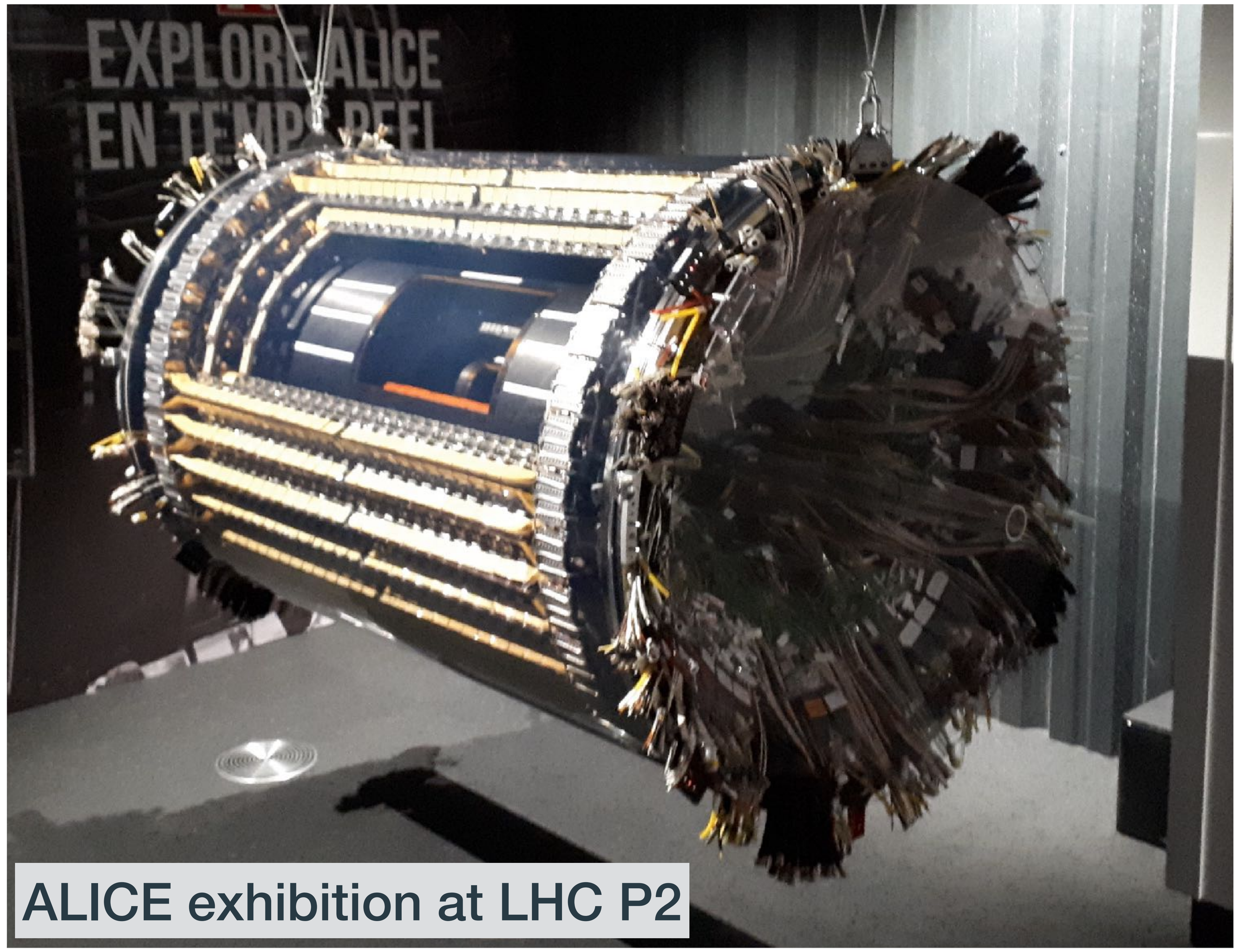
Radiation damage

- Non-Ionizing Energy Loss (NIEL)
  - Damage of the silicon crystal by particles impinging on the lattice
  - Dislocations of lattice atoms or more complex distortions of the crystal lattice
  - Affecting the charge collection properties (trapping), leakage current and the effective doping concentration
  - Usually expressed normalised to the damage level caused by 1 MeV neutrons (1 MeV n_{eq}/cm^2)

- Total Ionising Dose (TID)
  - Surface damage and damage of boundaries and interfaces (e.g. $Si\text{-}SiO_2$)
  - Charge build-up in the oxide layers and at the interfaces
  - Oxide charges influence the threshold characteristics of MOS transistors
  - Effects less pronounced in modern IC technologies due to their very thin oxide layers used for transistor gates

ITS1 in a nutshell

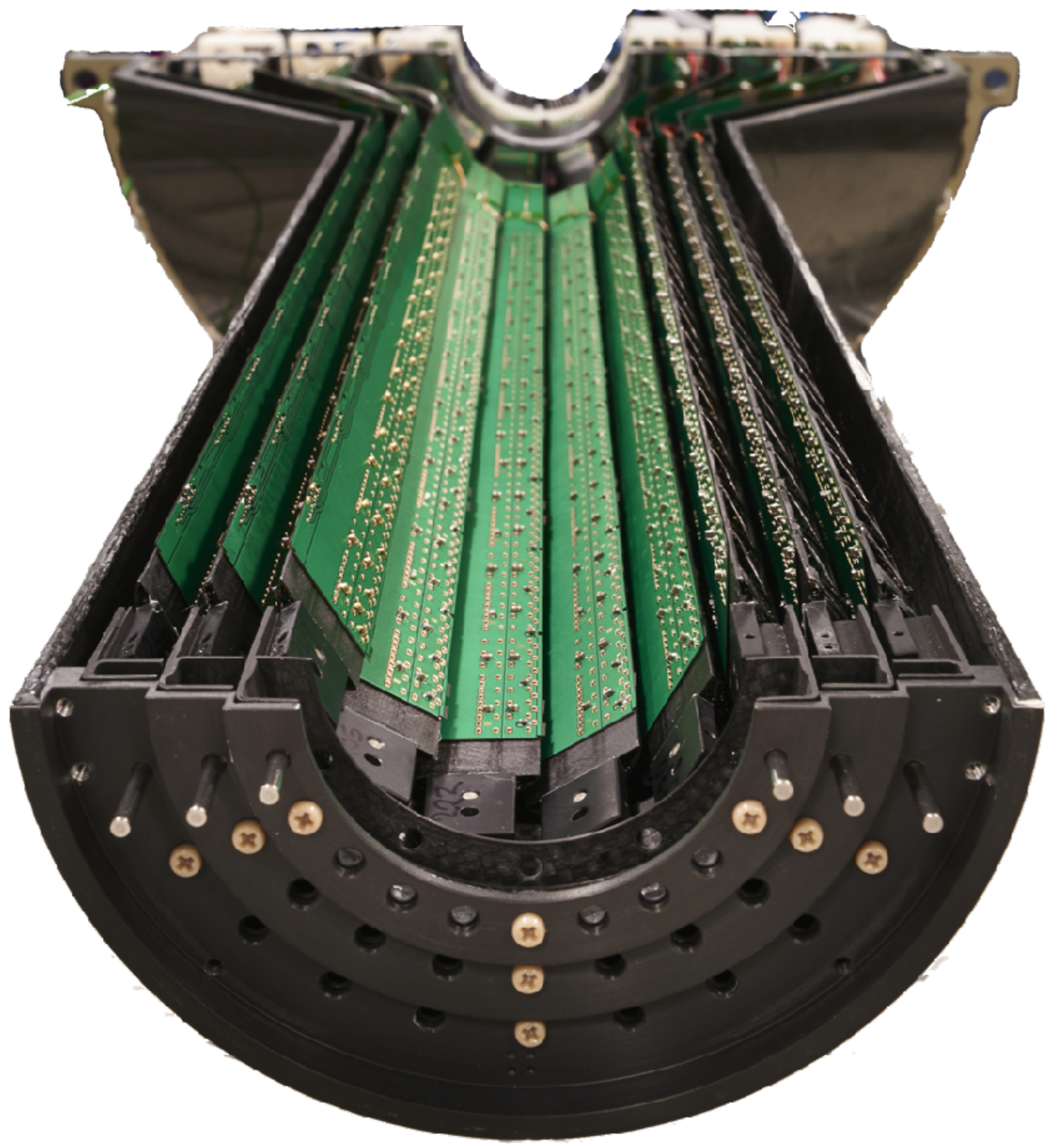
- 6 layers with 3 technologies
  - 2 Silicon Pixel Detector (SPD) layers
  - 2 Silicon Drift Detector (SDD) layers
  - 2 Silicon Strip Detector (SSD) layers
- Distance to interaction point: 39 mm
- Material budget: ~ 1.14% X_0
- Pixel pitch (SPD only): 50 x 425 μm^2
- Spatial resolution ($r\varphi$ x z): 11 x 100 μm^2
- Readout rate: 1 kHz

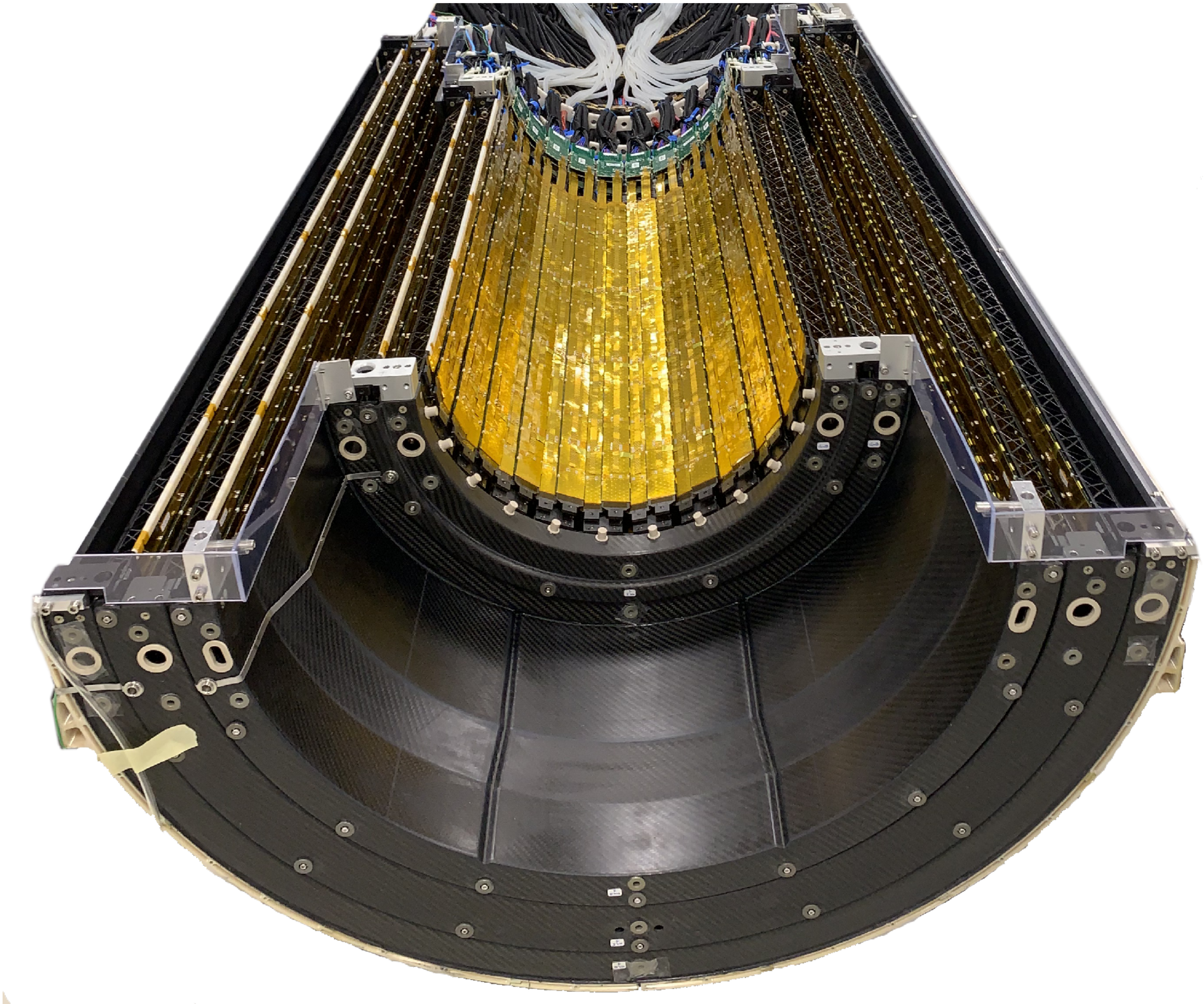


ALICE exhibition at LHC P2

It served some 10 years and was key to many analyses and publications…

… but technology has moved on!





ITS2

ITS2 Detector Seminar: https://indico.cern.ch/event/1210704/

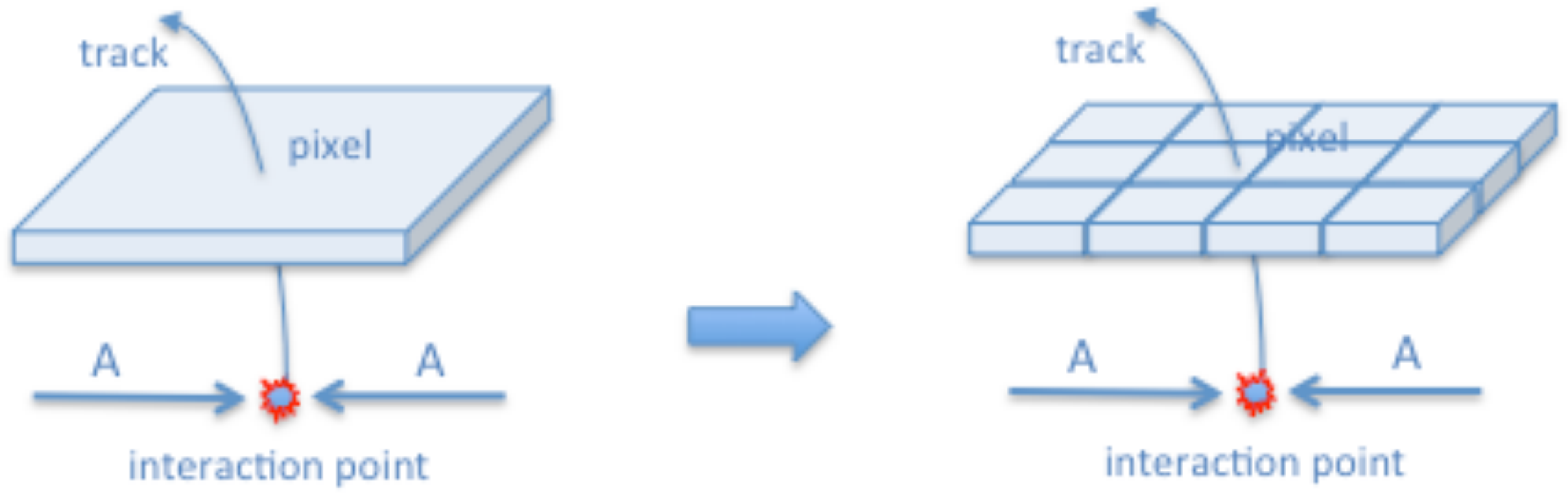
ITS2 design objectives

Improve impact parameter resolution
by a factor ~3 in rφ and ~5 in z at $p_{\mathrm{T}} = 500\ \mathrm{MeV}/c$

- Get closer to IP: 39mm ➔ 23mm (innermost layer)
- Reduce material budget:
  ~1.14% X_0 ➔ ~0.36% X_0 per layer (for the inner layers)
- Reduce pixel size: 50 x 425 μm^2 ➔ O(30 x 30 μm^2)

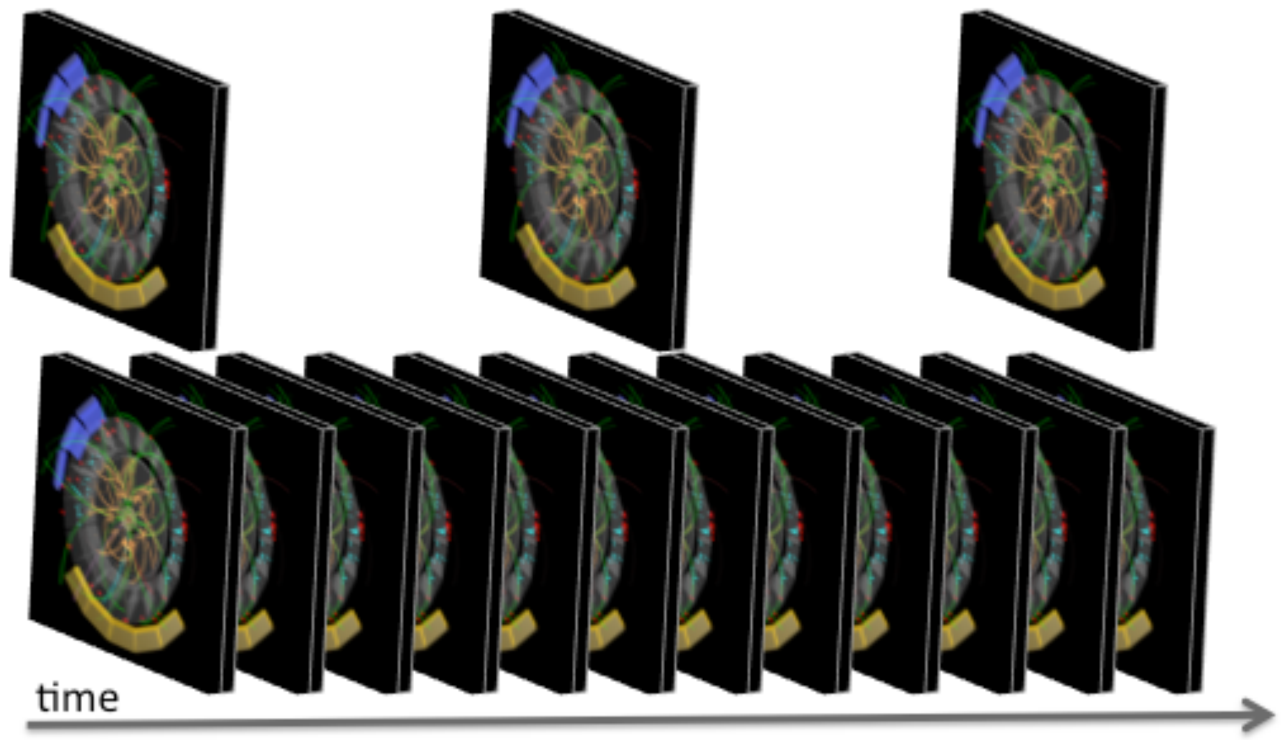
Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity: 6 layers ➔ 7 pixel layers

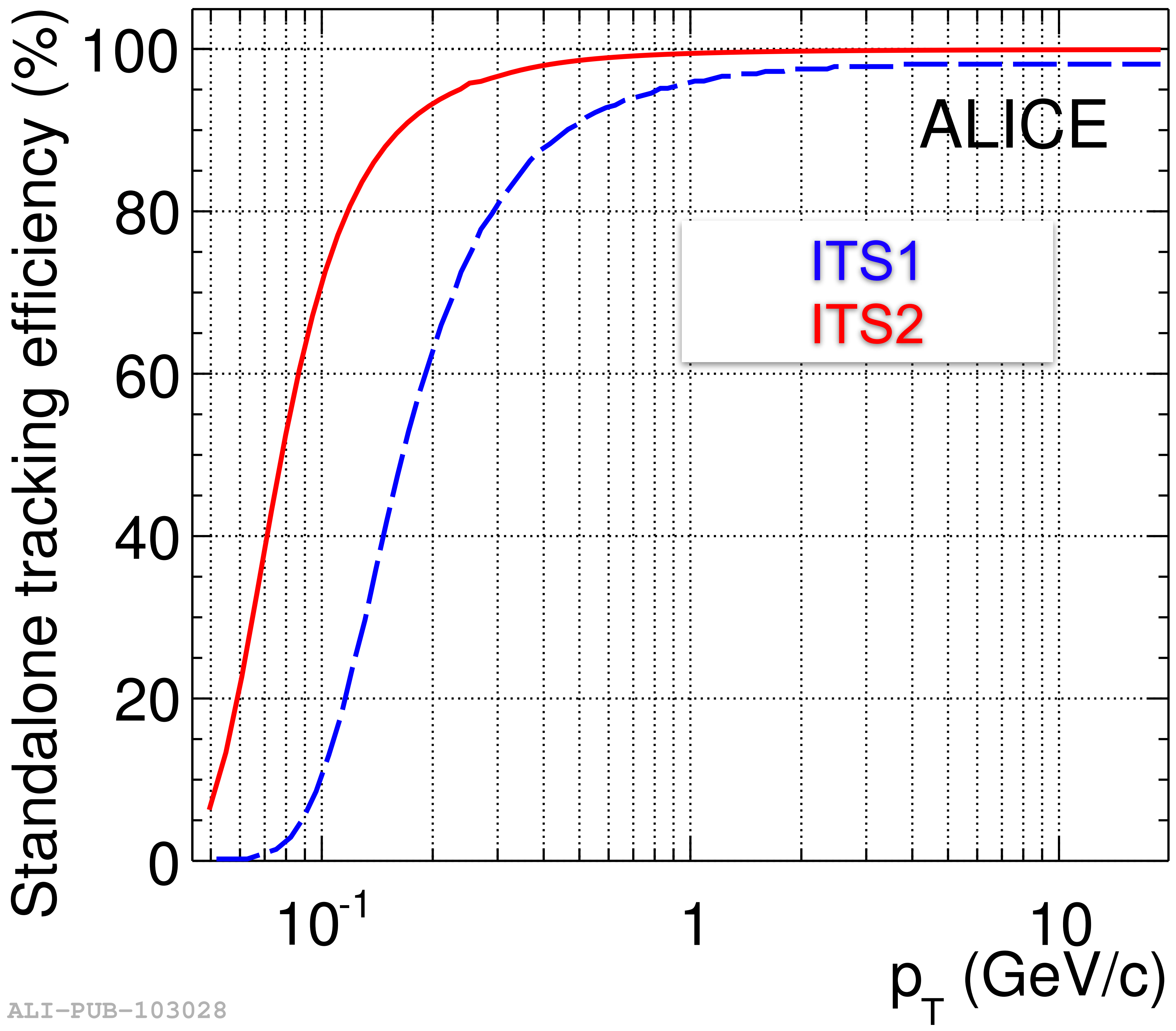


Fast readout

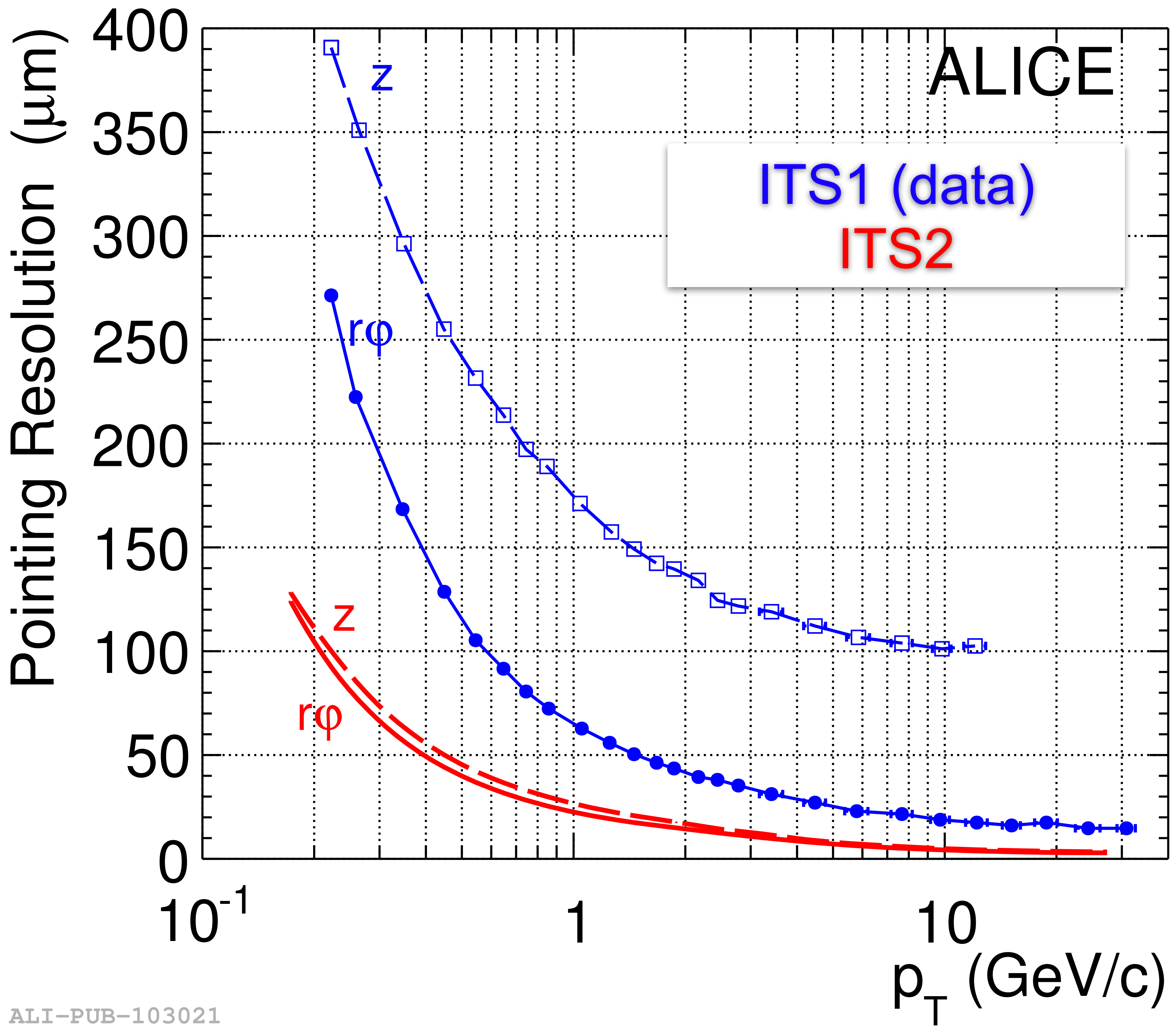
- Readout of Pb-Pb at up to 100 kHz (previously 1 kHz) and 400 kHz for pp



Detector performance in Run 3 — simulations



ALI-PUB-103028



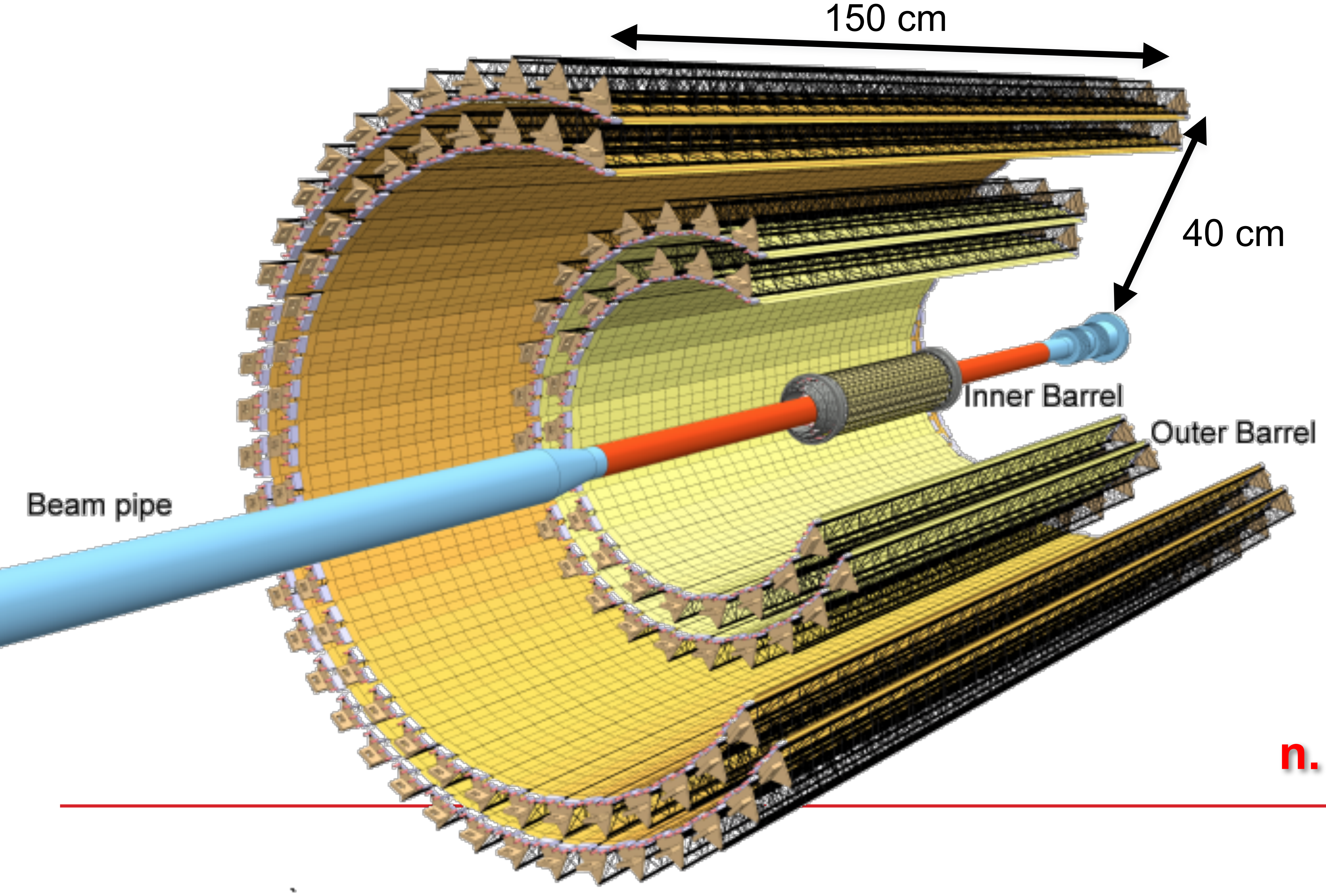
ALI-PUB-103021

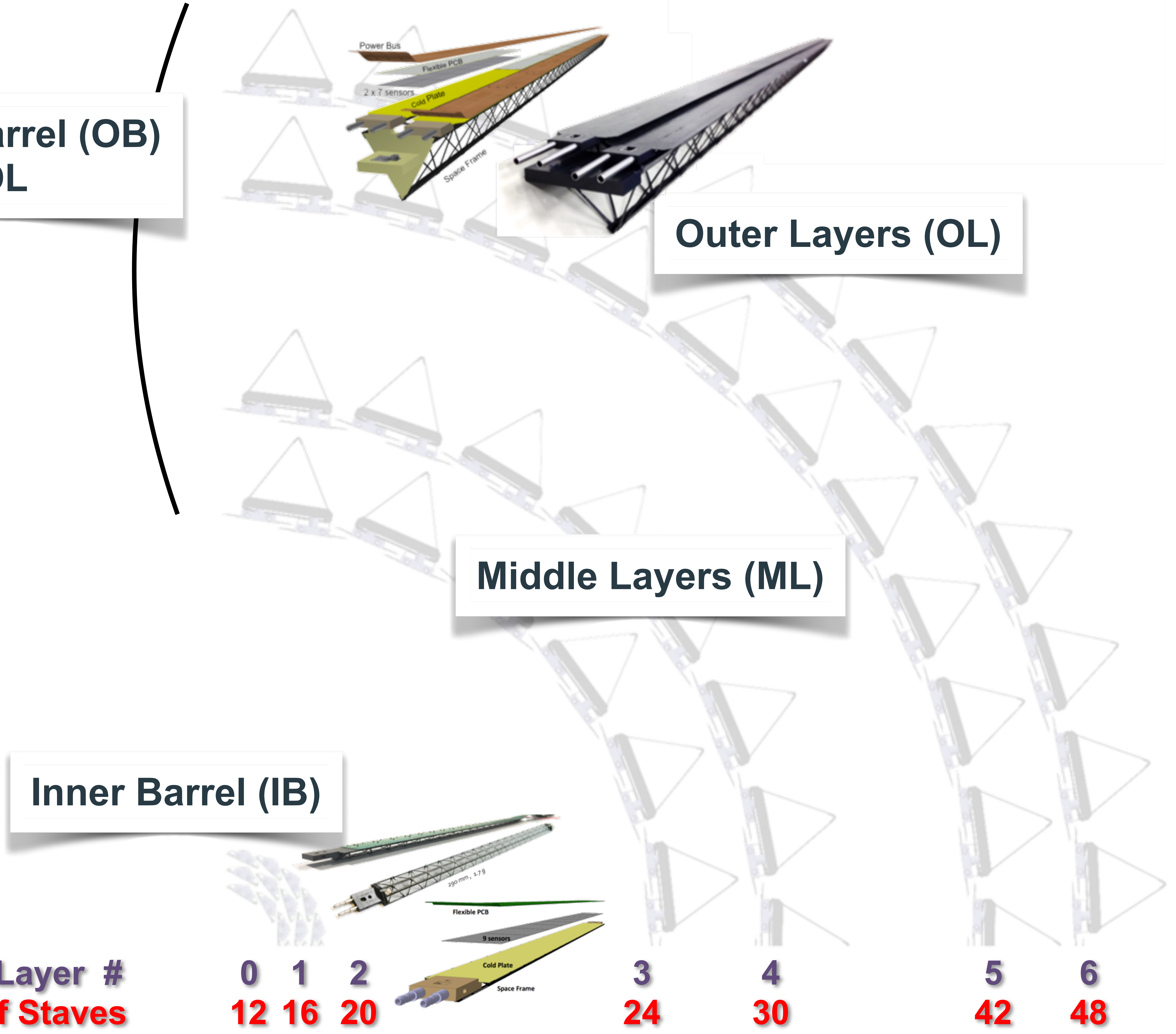
- Improved tracking efficiency (95% instead of 60% at 200 MeV/*c*)
- Pointing resolution 3x better in transverse plane (6x along beam axis) at 200 MeV/*c*

ITS2 layout

- 7 layers (inner/middle/outer): 3/2/2 from R = 23 mm to R = 400 mm
- 192 staves (IL/ML/OL): 48/54/90
- Ultra-lightweight support structure and cooling

10 m² active silicon area, 12.5×10⁹ pixels





Outer Barrel (OB) = ML + OL

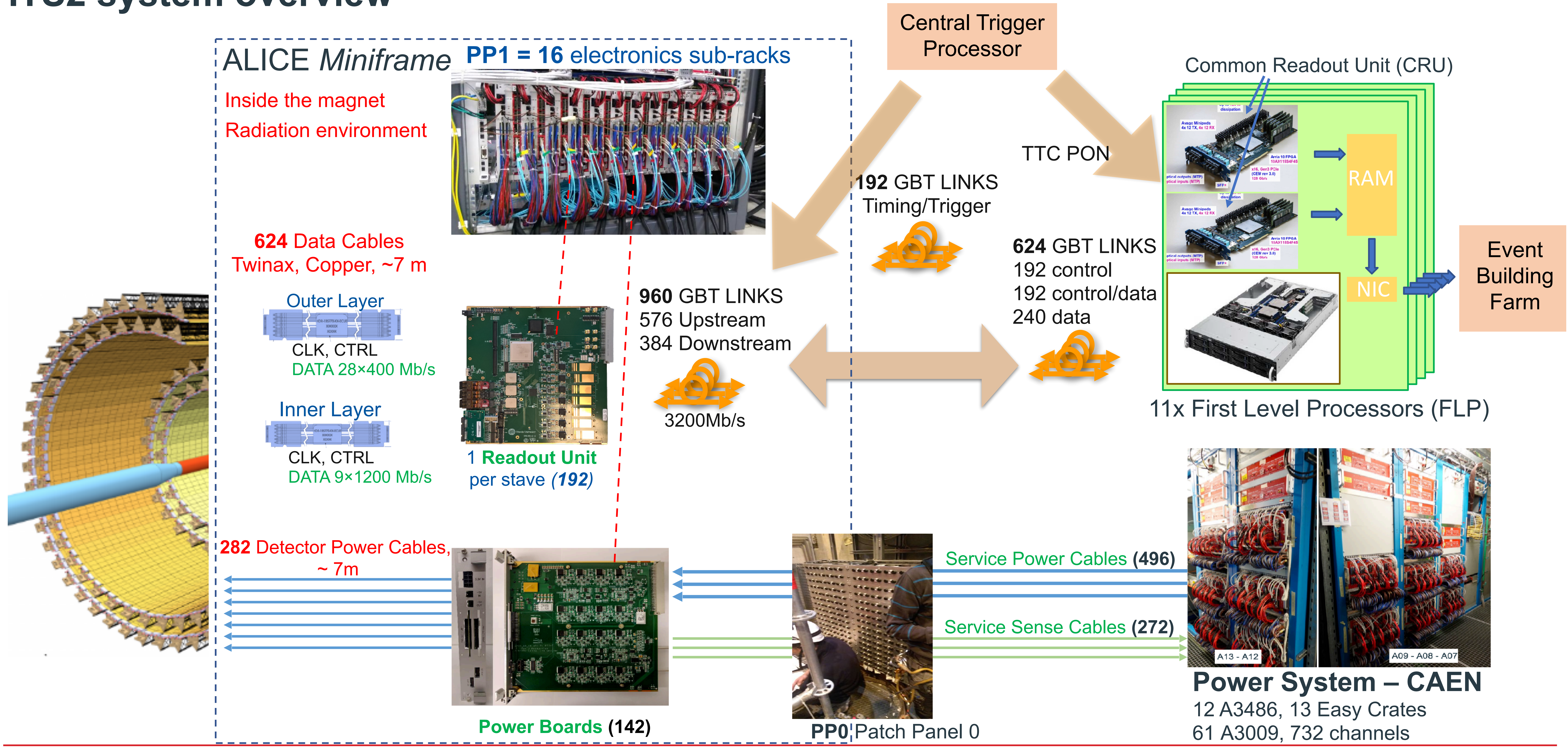
Outer Layers (OL)

Middle Layers (ML)

Inner Barrel (IB)

Layer #	0	1	2	3	4	5	6
n. of Staves	12	16	20	24	30	42	48

ITS2 system overview



ALICE *Miniframe* **PP1 = 16** electronics sub-racks

Inside the magnet

Radiation environment

624 Data Cables
Twinax, Copper, ~7 m

Outer Layer
CLK, CTRL
DATA 28×400 Mb/s

Inner Layer
CLK, CTRL
DATA 9×1200 Mb/s

1 **Readout Unit**
per stave *(**192**)*

960 GBT LINKS
576 Upstream
384 Downstream

3200Mb/s

282 Detector Power Cables,
~ 7m

Power Boards (**142**)

PP0 Patch Panel 0

Central Trigger Processor

TTC PON

192 GBT LINKS
Timing/Trigger

624 GBT LINKS
192 control
192 control/data
240 data

Common Readout Unit (CRU)

RAM

NIC

Event Building Farm

11x First Level Processors (FLP)

Service Power Cables (**496**)

Service Sense Cables (**272**)

Power System – CAEN
12 A3486, 13 Easy Crates
61 A3009, 732 channels

R&D, construction, installation and commissioning timeline

Research & Development
- Conceptual Design Report: Sep ’12
- Technical Design Report: Nov ‘13

Detector construction and assembly
- ~72000 chips —> ~2600 Hybrid Integrated Circuits (HICs) —> ~280 staves
- > 10 production sites worldwide
- ~ 30 institutes involved

On-surface commissioning w/ final services
- 24/7 operation with ~200 shifters from ~30 institutes
- Calibration runs, cosmic muon data taking
- Key to spot potential issues early
- Valuable input for the planning of the installation

Services installation in the cavern

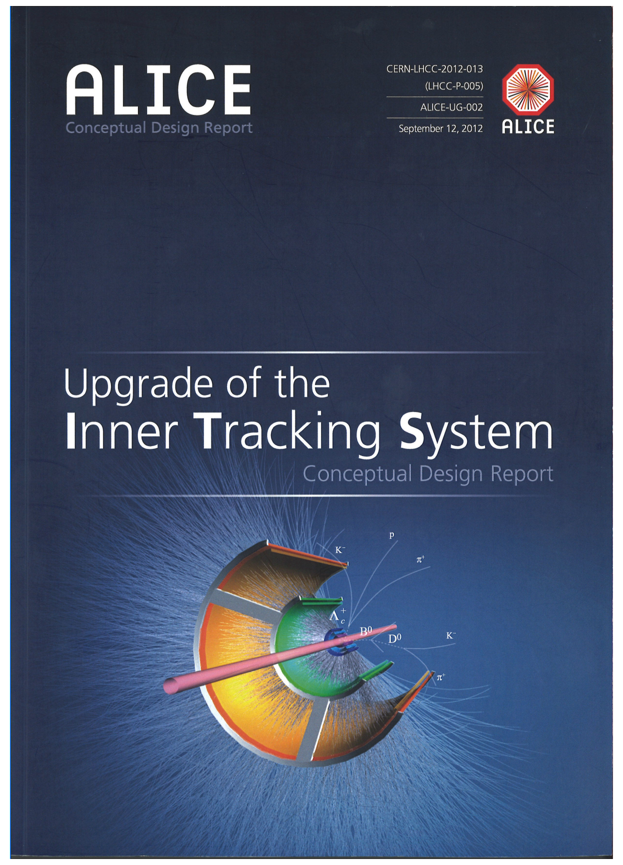
Outer Barrel installation

Inner Barrel installation

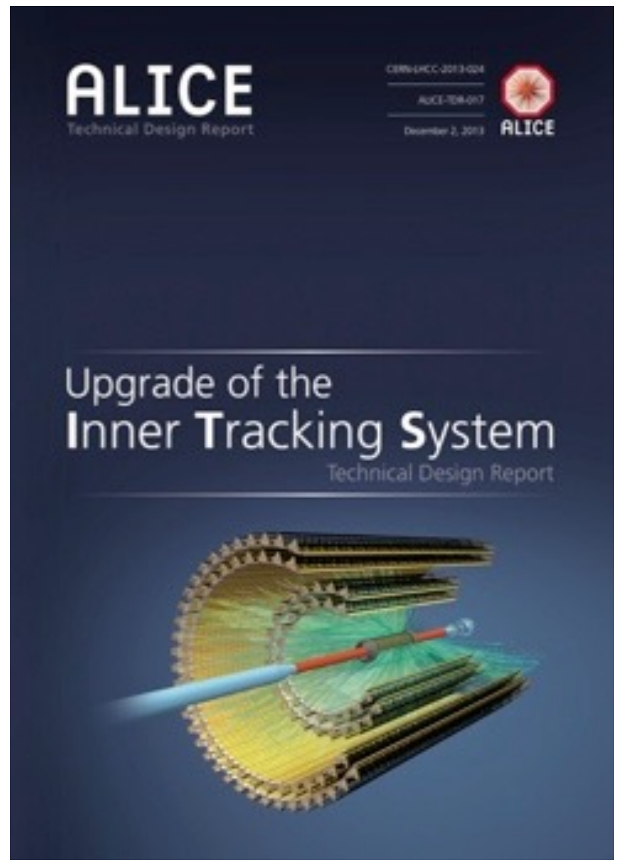
Verification of the detector

Global commissioning

Pilot beam test

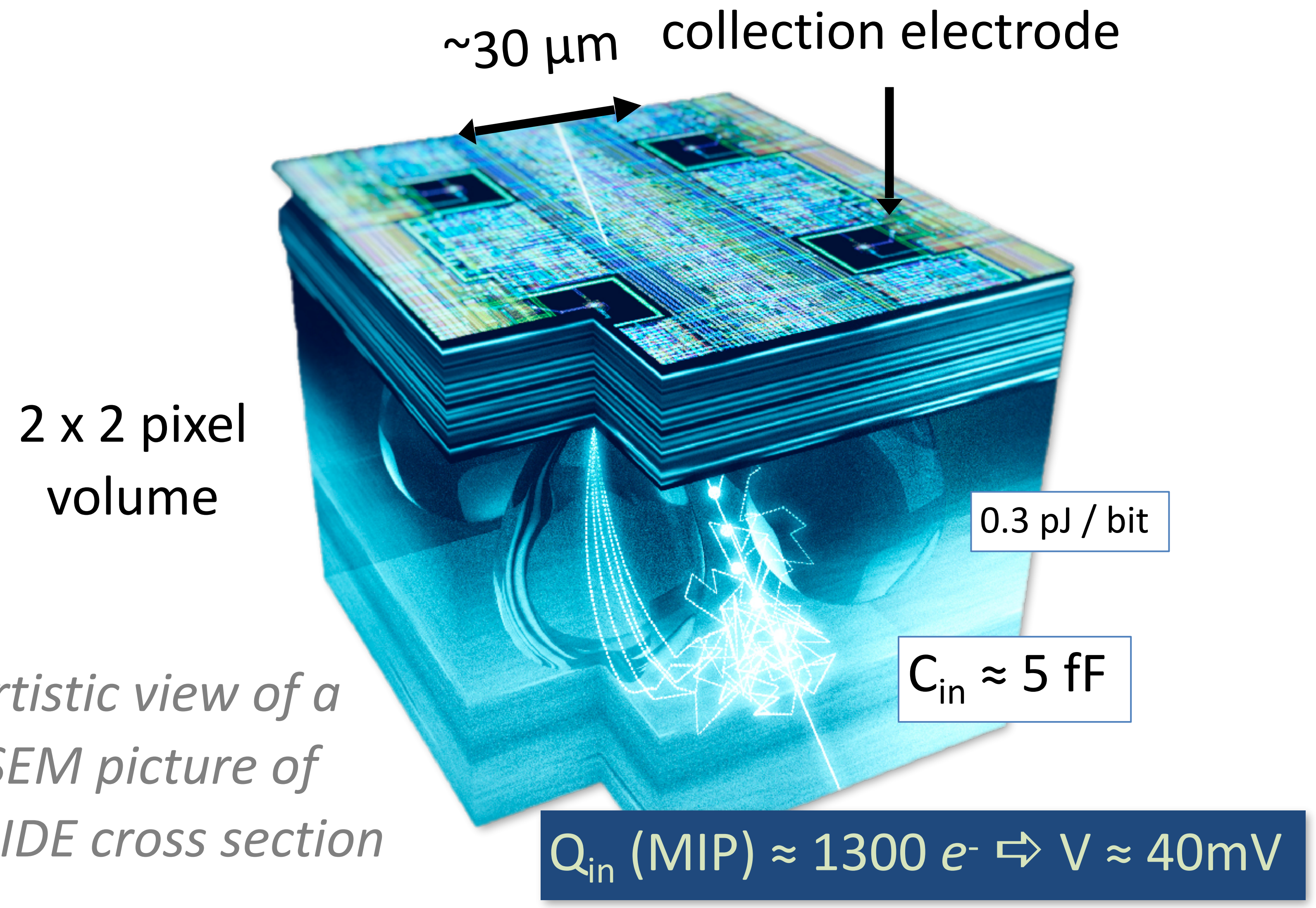


Conceptual Design Report

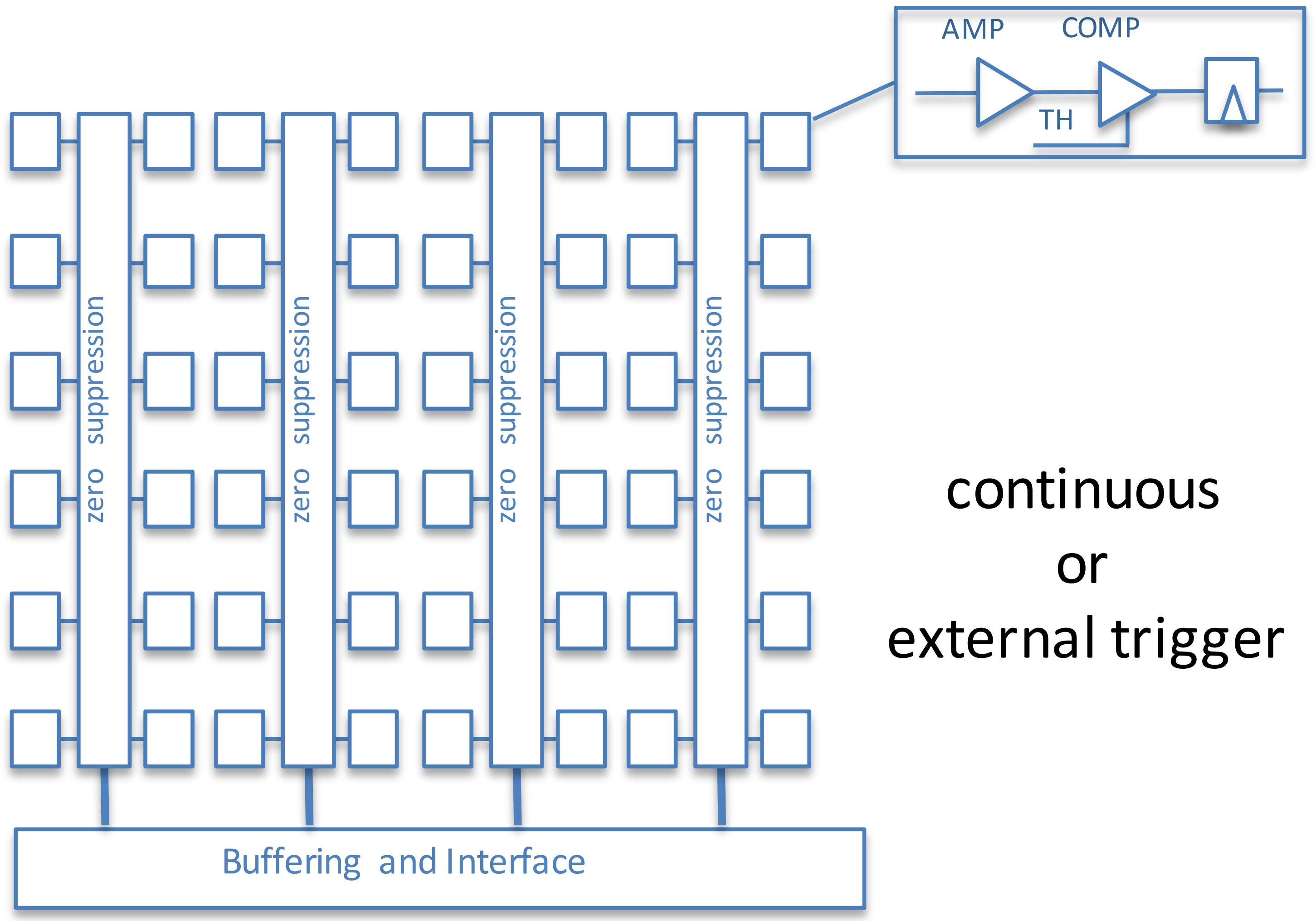


Technical Design Report

ALPIDE — the Monolithic Active Pixel Sensor (MAPS) for ITS2



Artistic view of a SEM picture of ALPIDE cross section



- Developed within the ITS2 project

Technology

Technology now used in other applications

- TowerJazz 180 nm CMOS Imaging Process
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25 µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel (~30 µm)
  ➔ low capacitance (~fF)
- Reverse bias voltage ($-6\text{ V} < V_{BB} < 0\text{ V}$) to substrate to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors
  ➔ full CMOS circuitry within active area

Key features

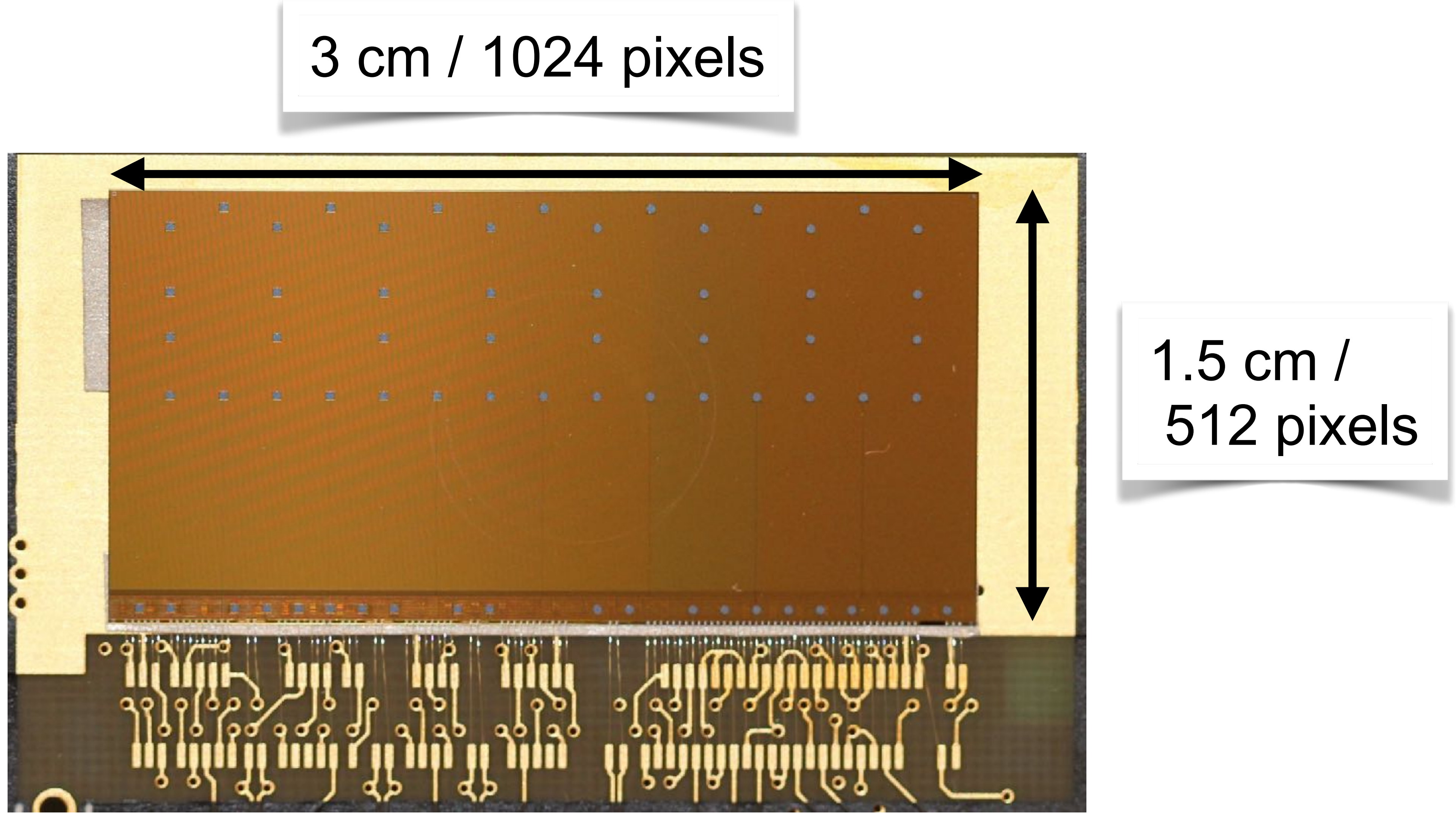
- In-pixel amplification and shaping, discrimination and Multiple-Event Buffers (MEB)
- In-matrix data sparsification
- On-chip high-speed link (1.2 Gbps)
- Low total power consumption < 40 mW/cm^2

ESE Electronics seminar by T. Kugathasan

ALPIDE requirements and performance

Parameter	Requirement	ALPIDE
Spatial resolution (µm)	≈ 5	≈ 5
Integration time (µs)	< 30	< 10
Fake-hit rate (/ pixel / event)	$< 10^{-6}$	$<< 10^{-6}$
Detection efficiency	> 99%	>>99%
Power consumption (mW / cm²)	< 100	< 40
Total Ionising Dose (TID) (krad)	> 270 (IB) > 10 (OB)	OK
Non-Ionising Energy Loss (NIEL) (1 MeV n_{eq} / cm²)	$> 1.7\text{x}10^{12}$	OK

These are not technology limits, but mostly design choices!

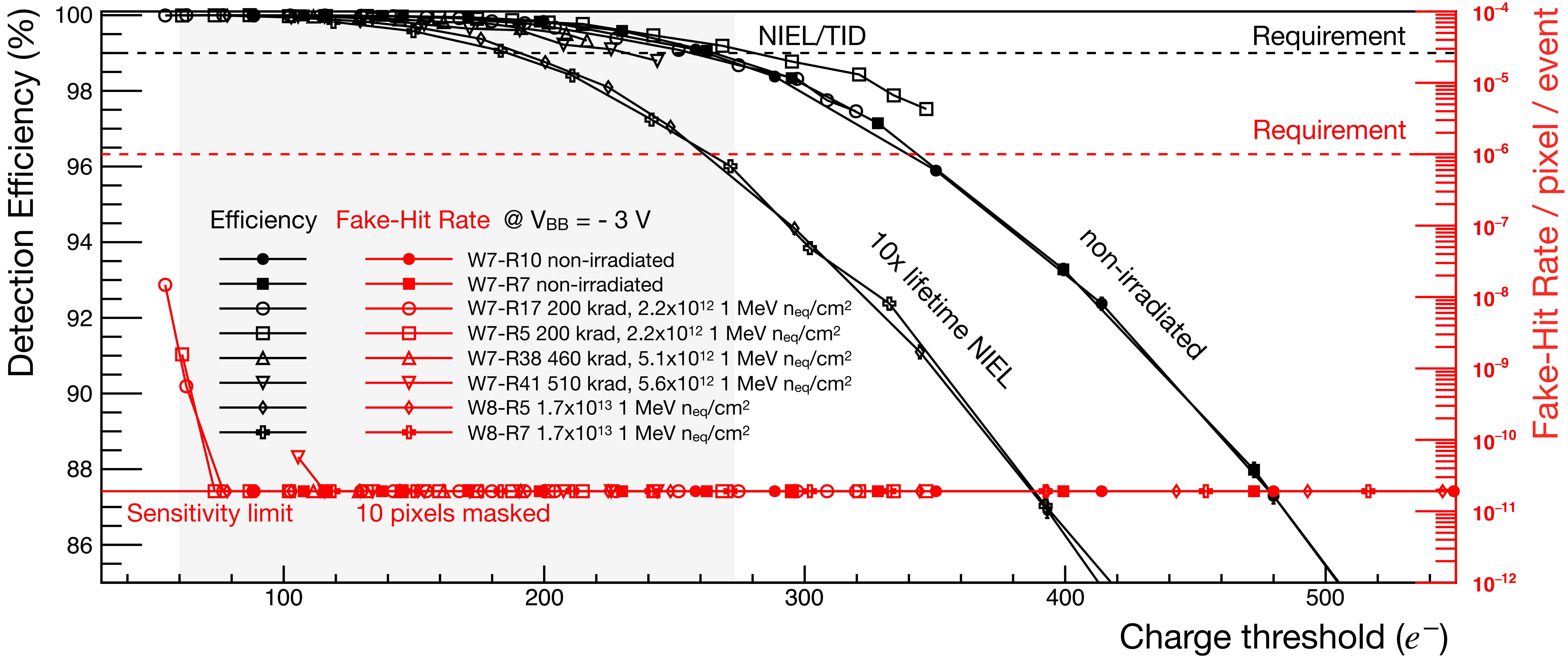


ALPIDE die on carrier card

> 70k chips produced and tested

24k in continuous operation on ITS2
+ several other applications

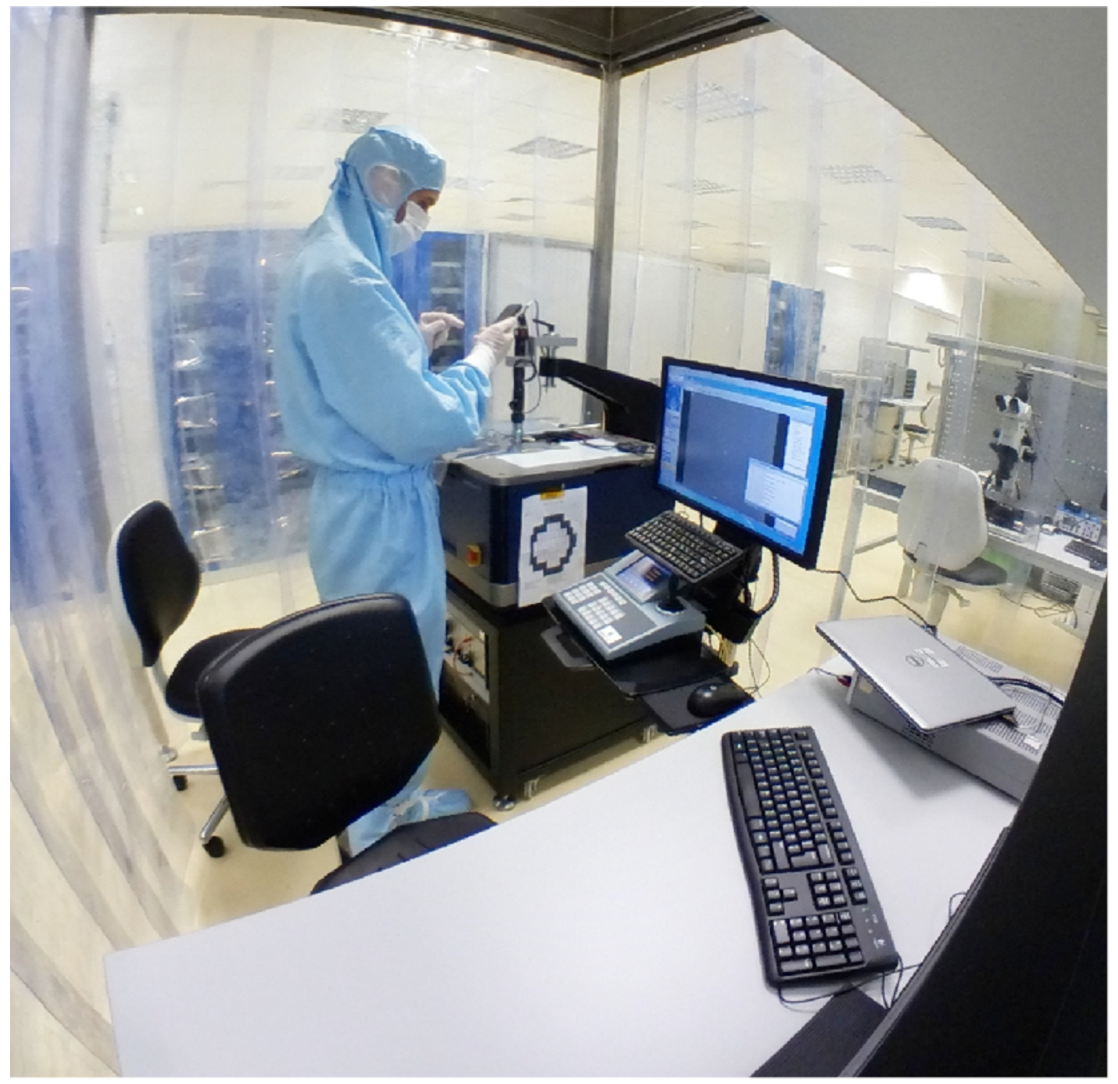
ALPIDE performance — detection efficiency and fake-hit rate



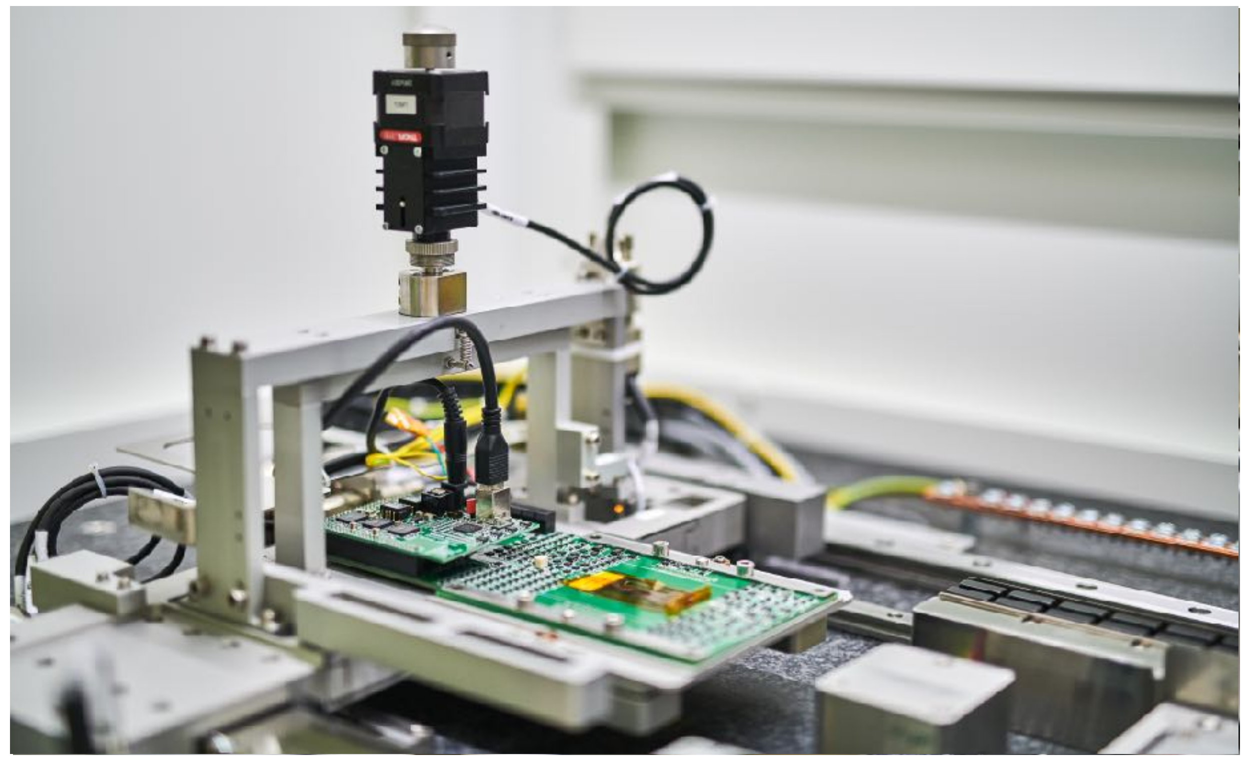
Availability and excellent support from test-beam facilities all over the world have been key for the development of this chip: BTF Frascati, CERN, DESY, LBNL, UC Louvain la Neuve, Pohang (Korea), Rez (Czech Republic), SLRI (Thailand)

ALPIDE series production

- Probe testing on **~10%** of the **wafers** before thinning and dicing
- Tested **all > 70000** thinned and diced **chips** individually
- Two separate, automated machines based on common probe card:
  - ‘ALICIA’ Module Assembly Machine with chip testing extension
  - ‘Corea YS-1’ dedicated chip testing machine
- **Classification** based on
  - Current consumption at nominal powering
  - Performance of the on-chip biasing DACs
  - Functioning of the on-chip digital circuitry
  - Pixel response to analogue injections
  - Charge threshold scan on every pixel
- **Yield**
  - Electrical yield: 65%
  - Gold* chips (used for the IB): 30%



Wafer probe testing



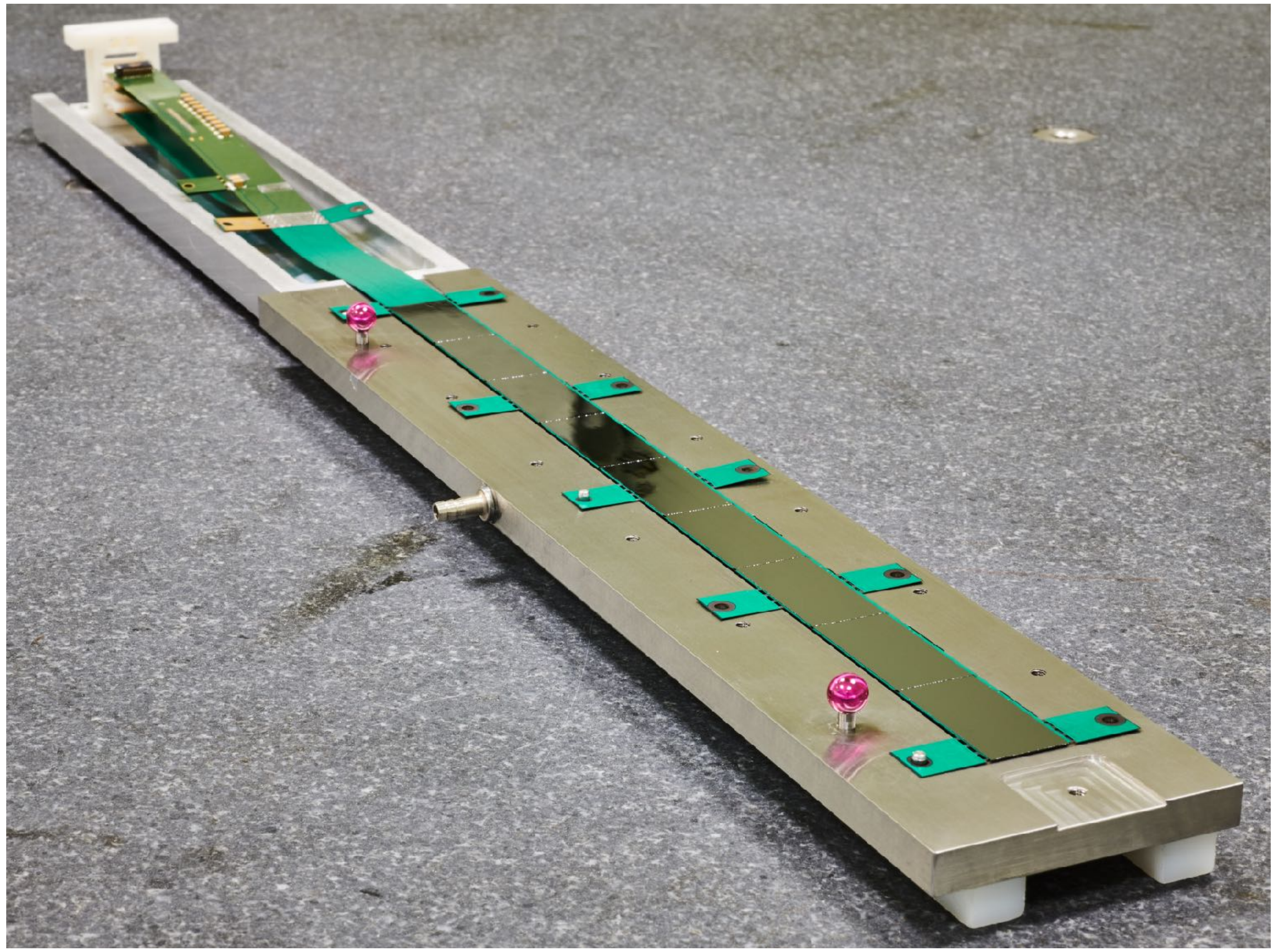
Probe card

ALICIA

Corea YS-01

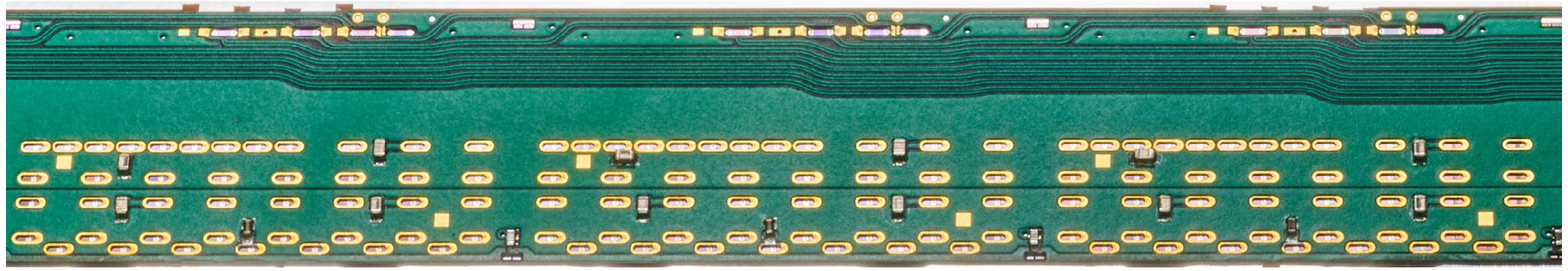
* stricter overall cuts, but in particular no bad double column

Modules — Hybrid Integrated Circuits (HICs) — Inner Barrel (IB)

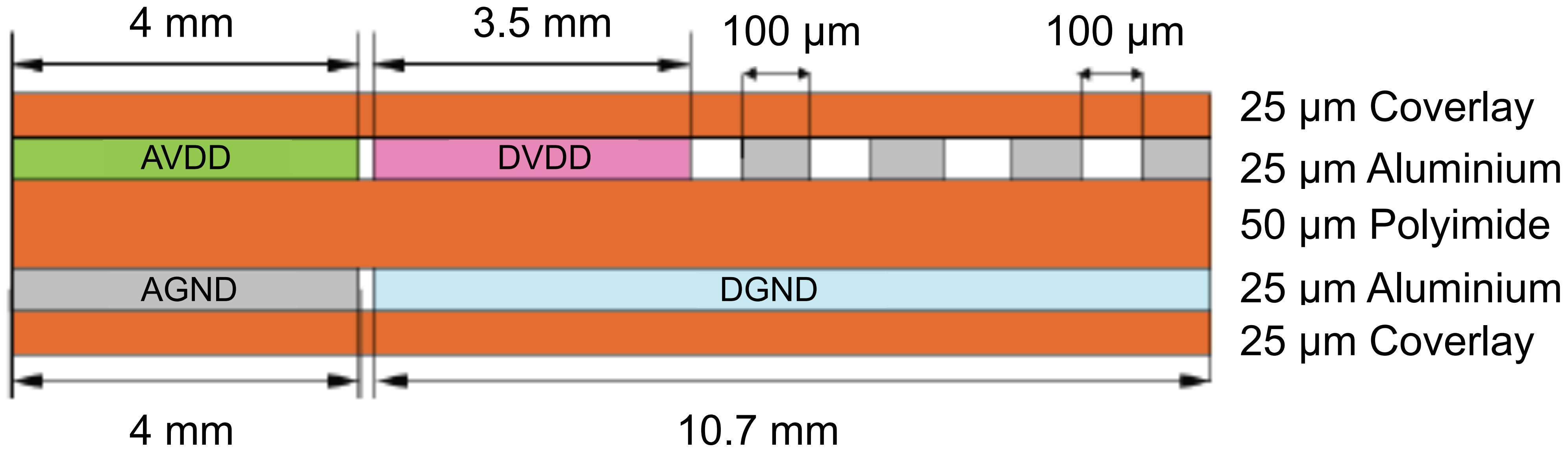


- 9 chips in a row, active area: ~ 1.5 x 27 cm^2
- 1 high-speed link of 1.2 Gbit/s per chip
- Clock, control, data and power supplied via Flexible Printed Circuit (FPC) using aluminium as conductor
- Interconnection by wirebonding through vias in the FPC
- No other active components than the ALPIDE chips on the FPCs
- Production quantity: ~ 100
- Production yield: 73%

Wirebonding through vias

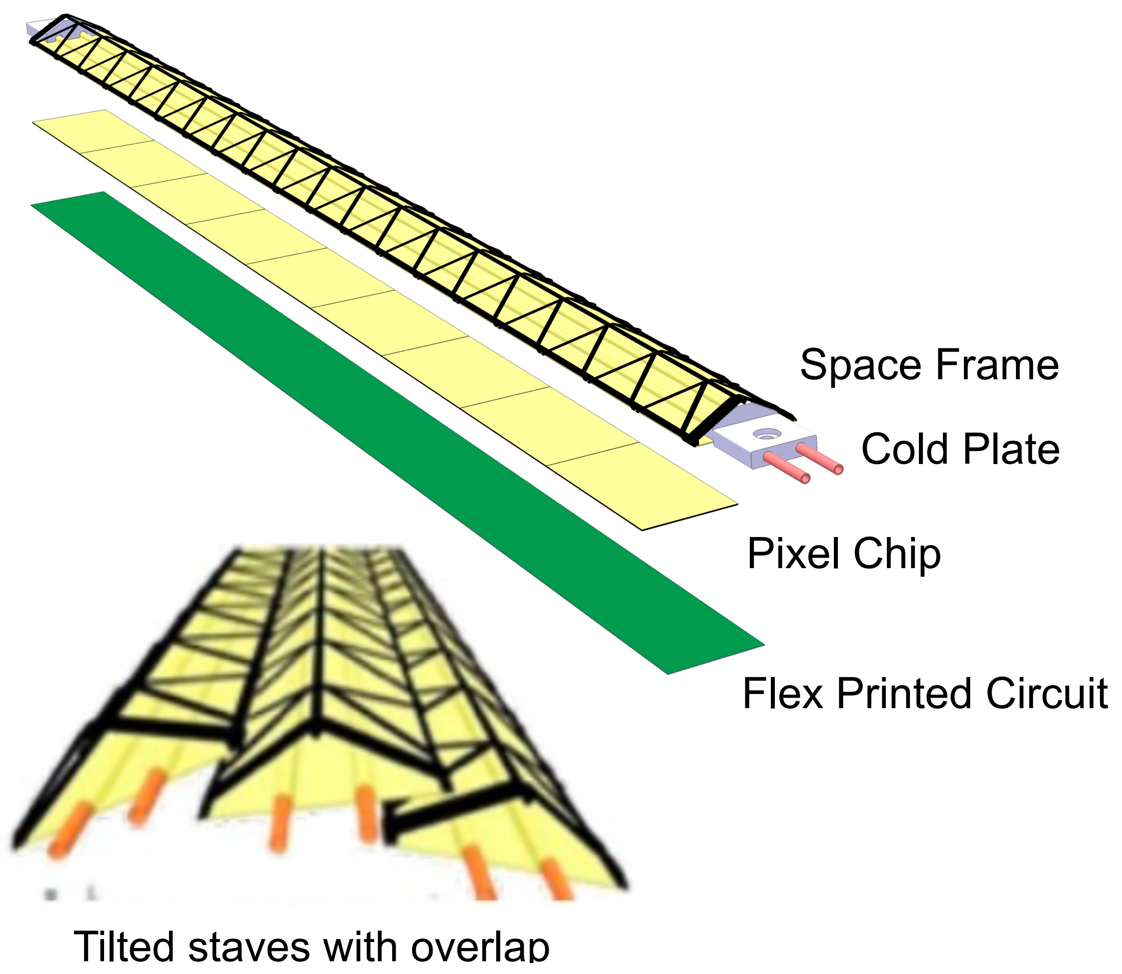


Top: bottom side of an IB HIC, bottom: view on FPC of 3 ALPIDEs



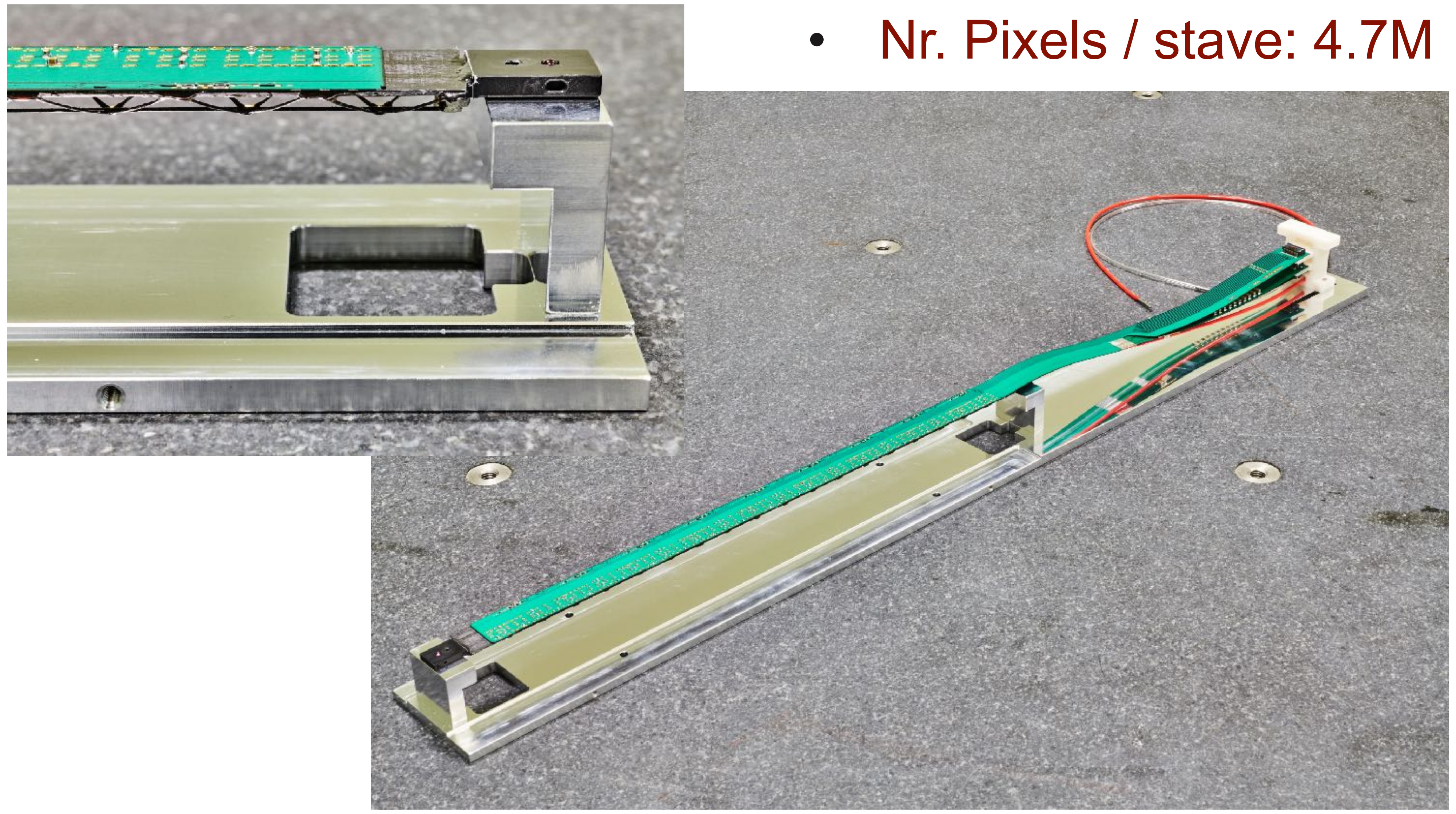
IB FPC stack-up and patterning

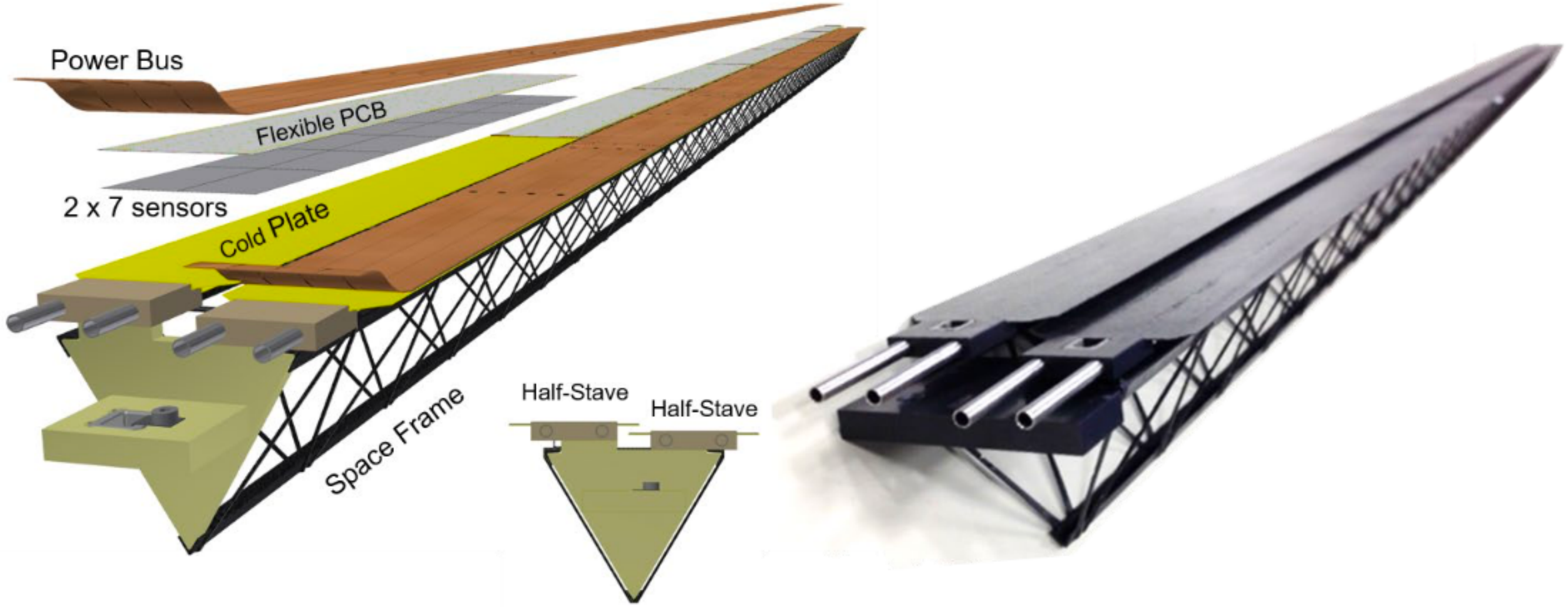
Detector staves



Inner Barrel (IB)

- <radius> (mm): 23, 31, 39
- Length (mm): 270
- Nr. staves: 48 (total)
  12 (L0), 16 (L1), 20 (L2)
- Nr. Chips: 432
- Material budget:
  ~0.36% X_0 per layer
- Single HIC per stave
- Nr. Pixels / stave: 4.7M

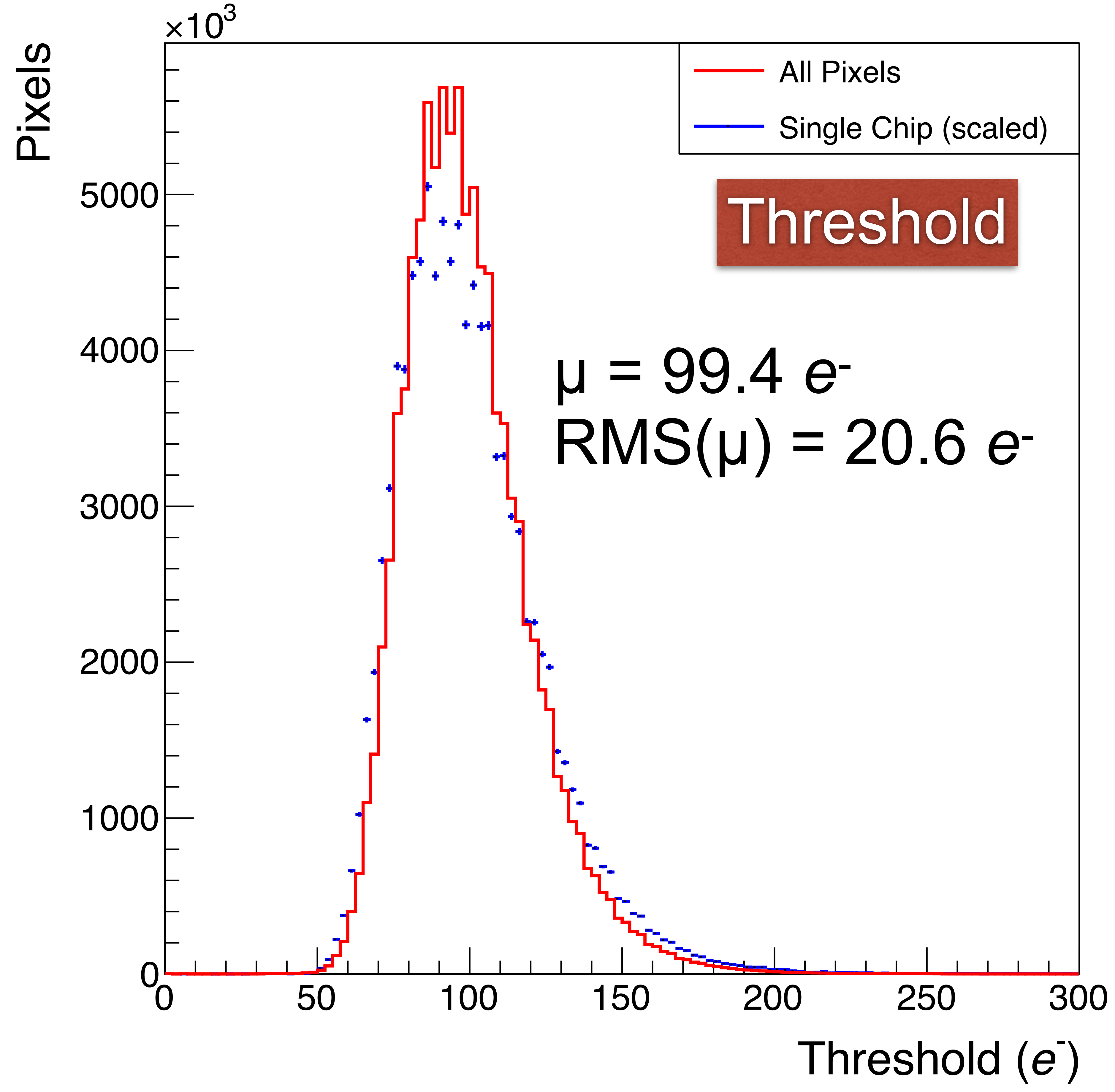


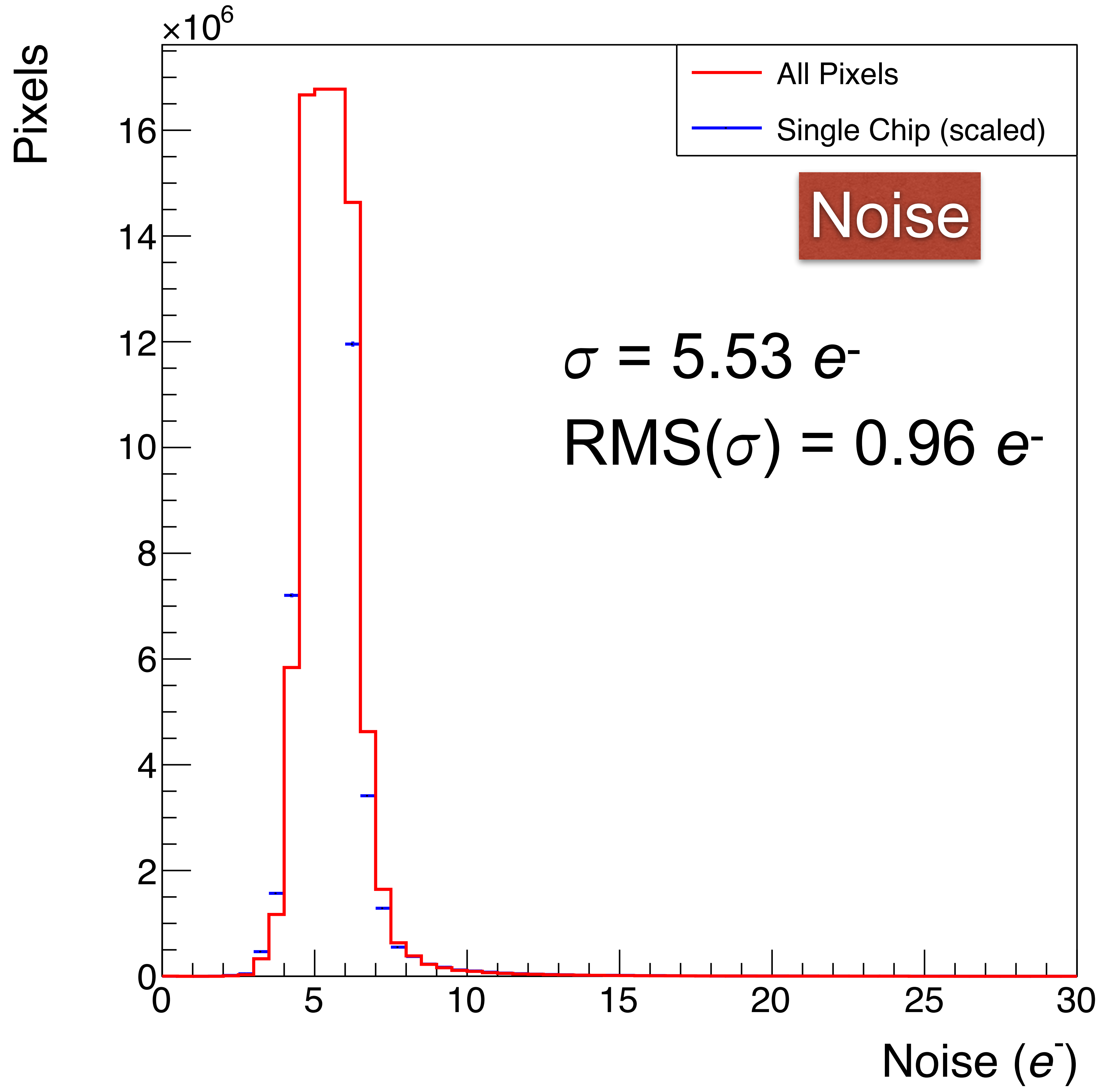


Outer Barrel (OB) — Middle Layers (MLs) and Outer Layers (OLs)

- <radius> (mm): 194, 247, 353, 405
- Nr. staves: 24 (L3), 30 (L4), 42 (L5), 48 (L6); total: 144
- Nr. chips: 6048 (ML), 17740 (OL)
- Length (mm): 844 (ML), 1478 (OL)
- Material budget: ~ 1.14% X_0 per layer
- Two partially overlapping half-staves per staves
- Nr. modules / half-stave: 4 (ML), 7 (OL)
- Nr. pixels / stave: 59M (ML), 102M (OL)

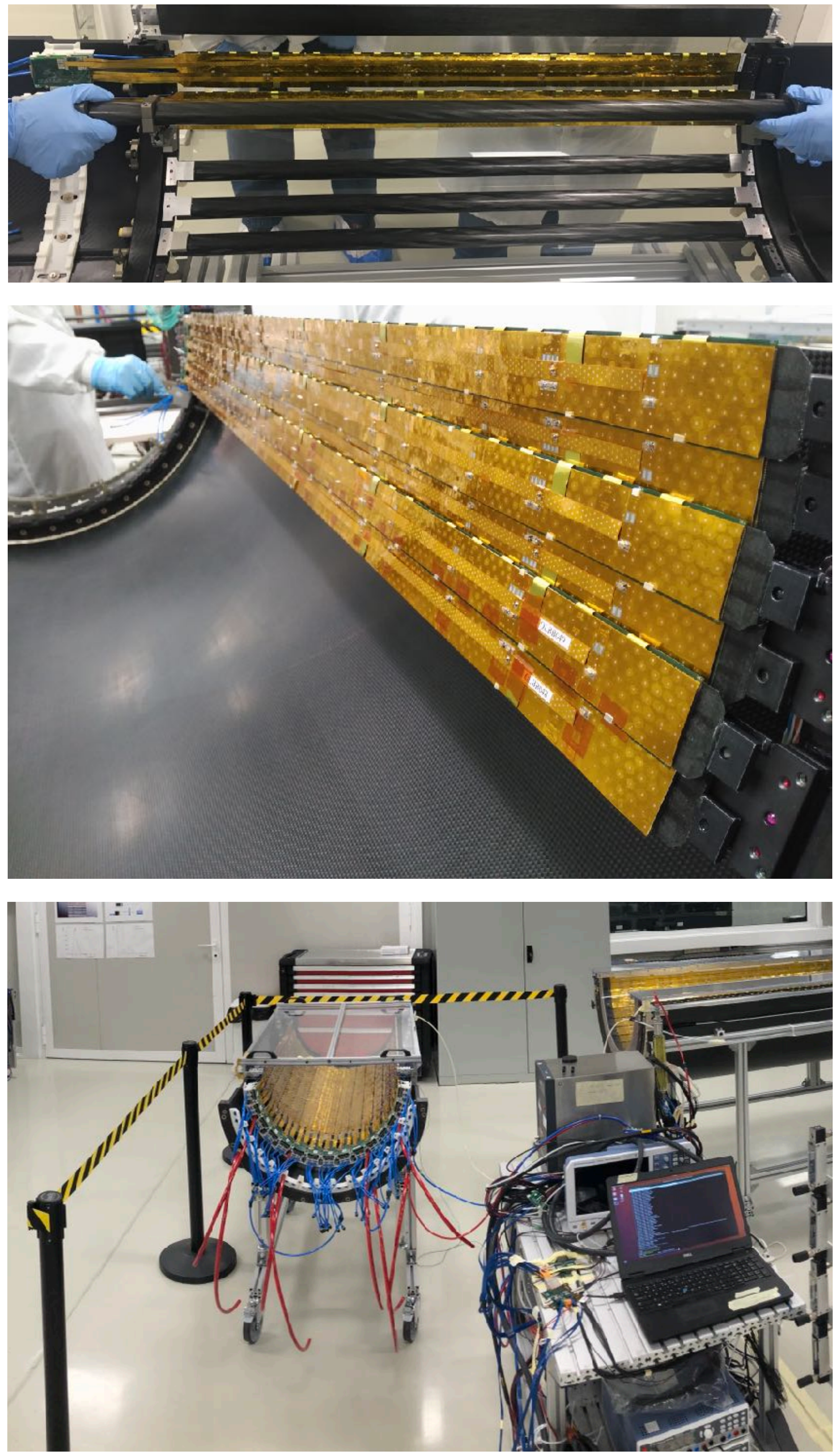
Outer Layer stave — threshold and noise uniformity



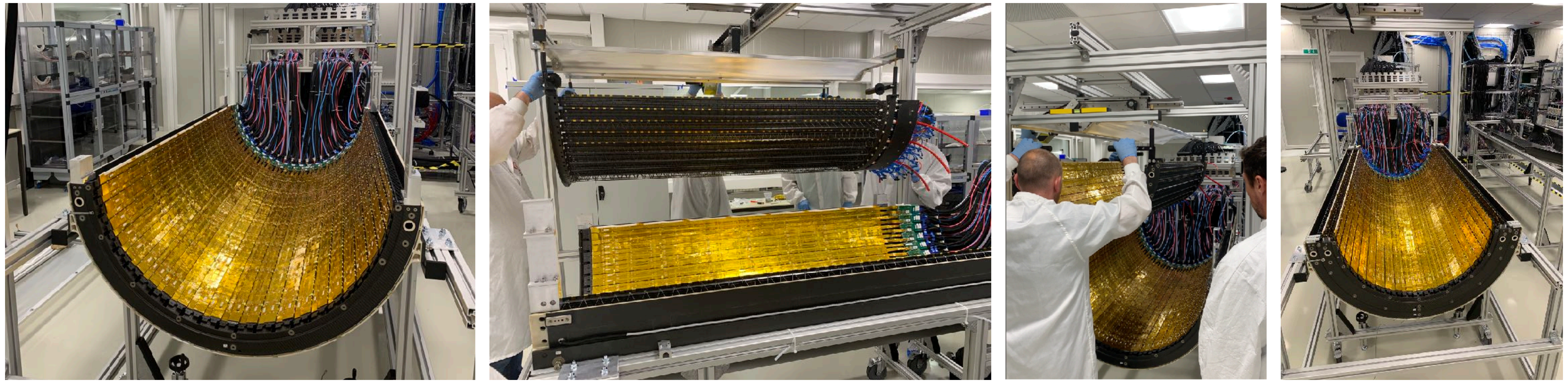


- Chip-by-chip tuning of the settings of the 196 chips (103M pixels)
- Excellent noise and threshold uniformity maintained across the full stave

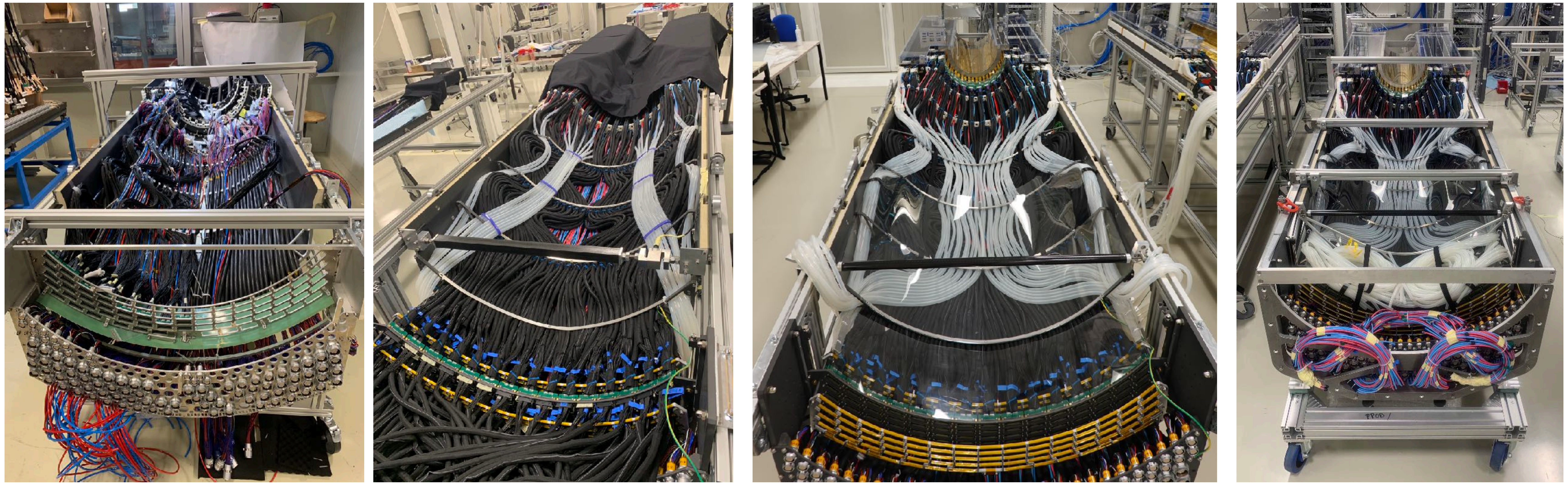
Layer and Half-Barrel assembly



Layer assembly and testing

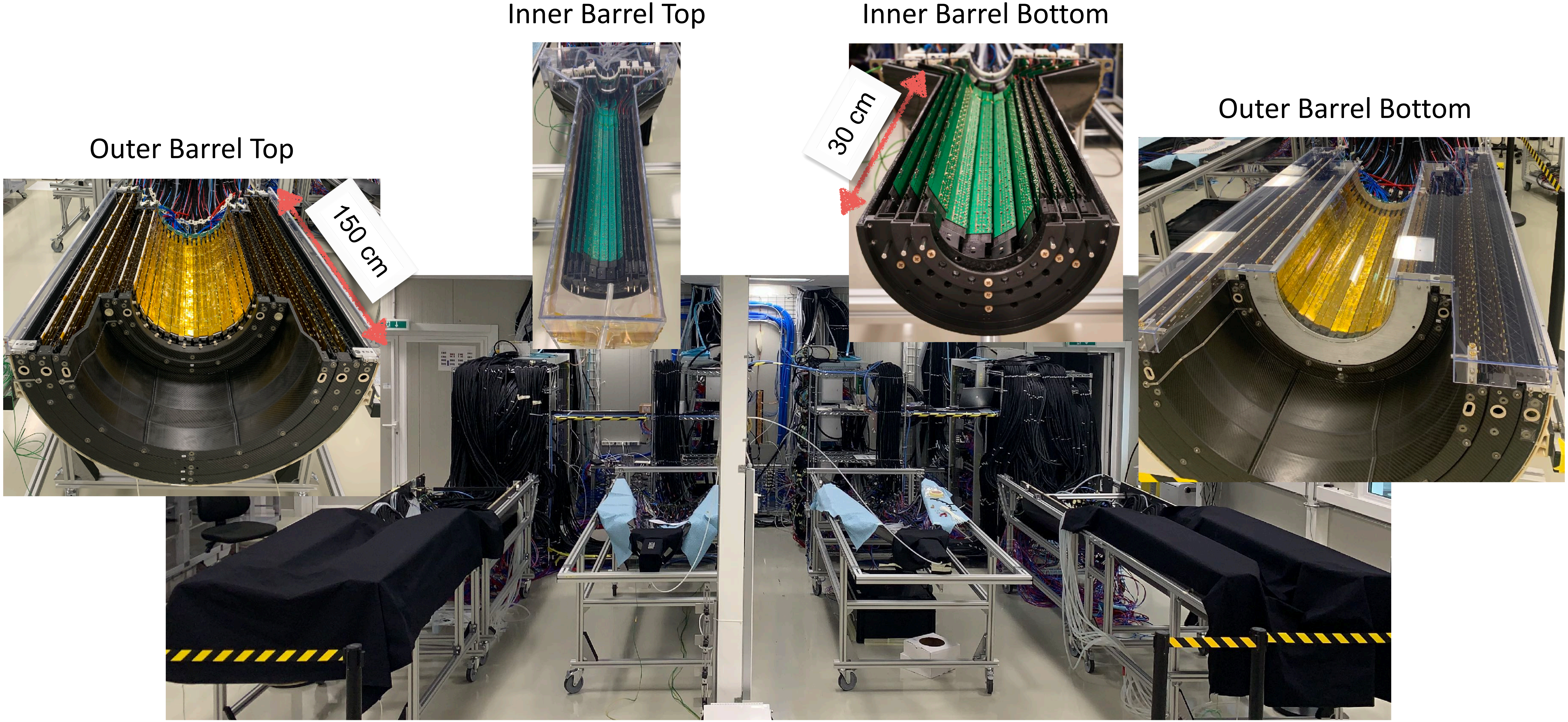


Half Barrel assembly



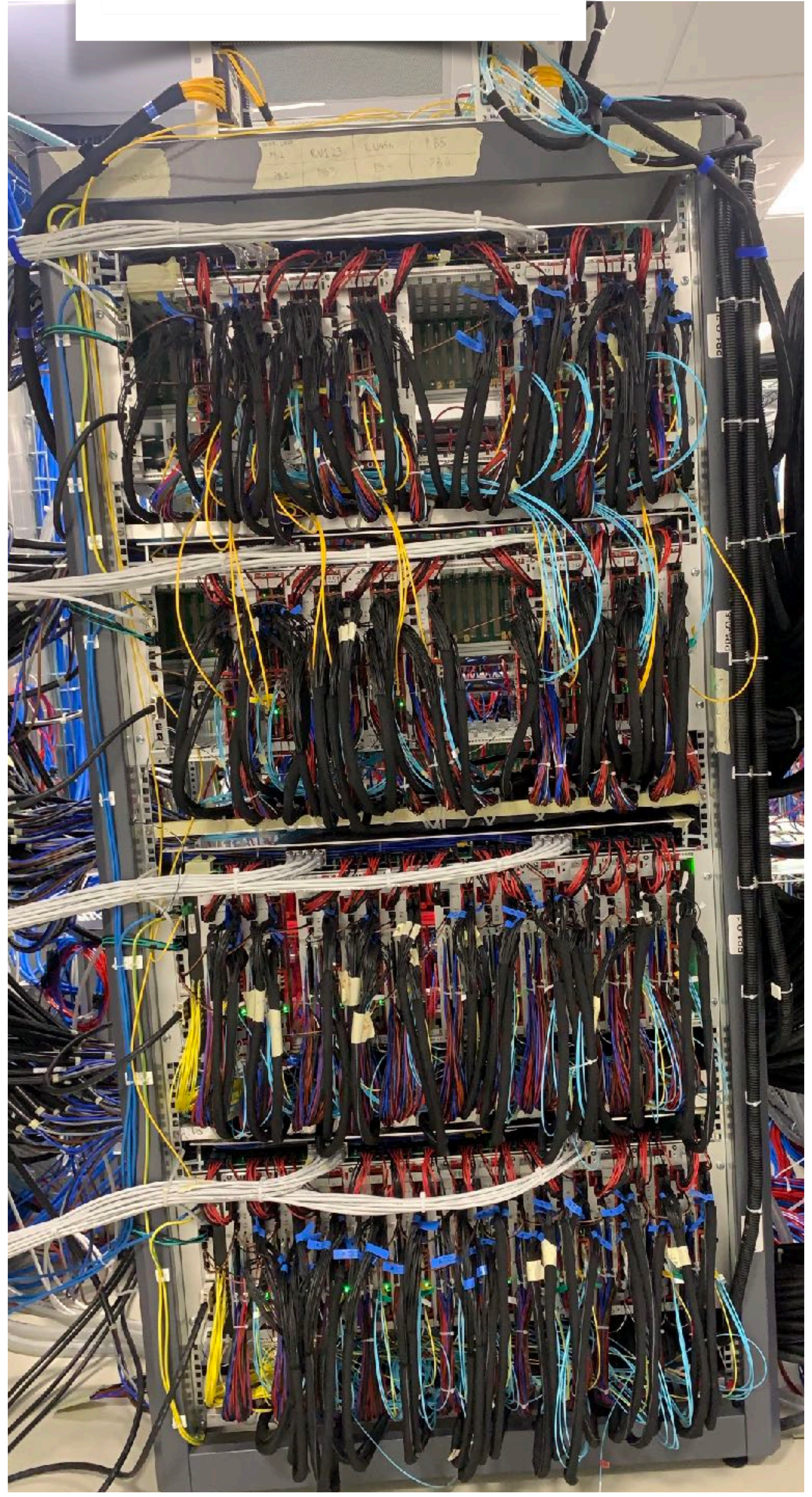
Service routing: several iterations, stripped power cable jackets, added flexible sleeves for power and data cables

On-surface commissioning

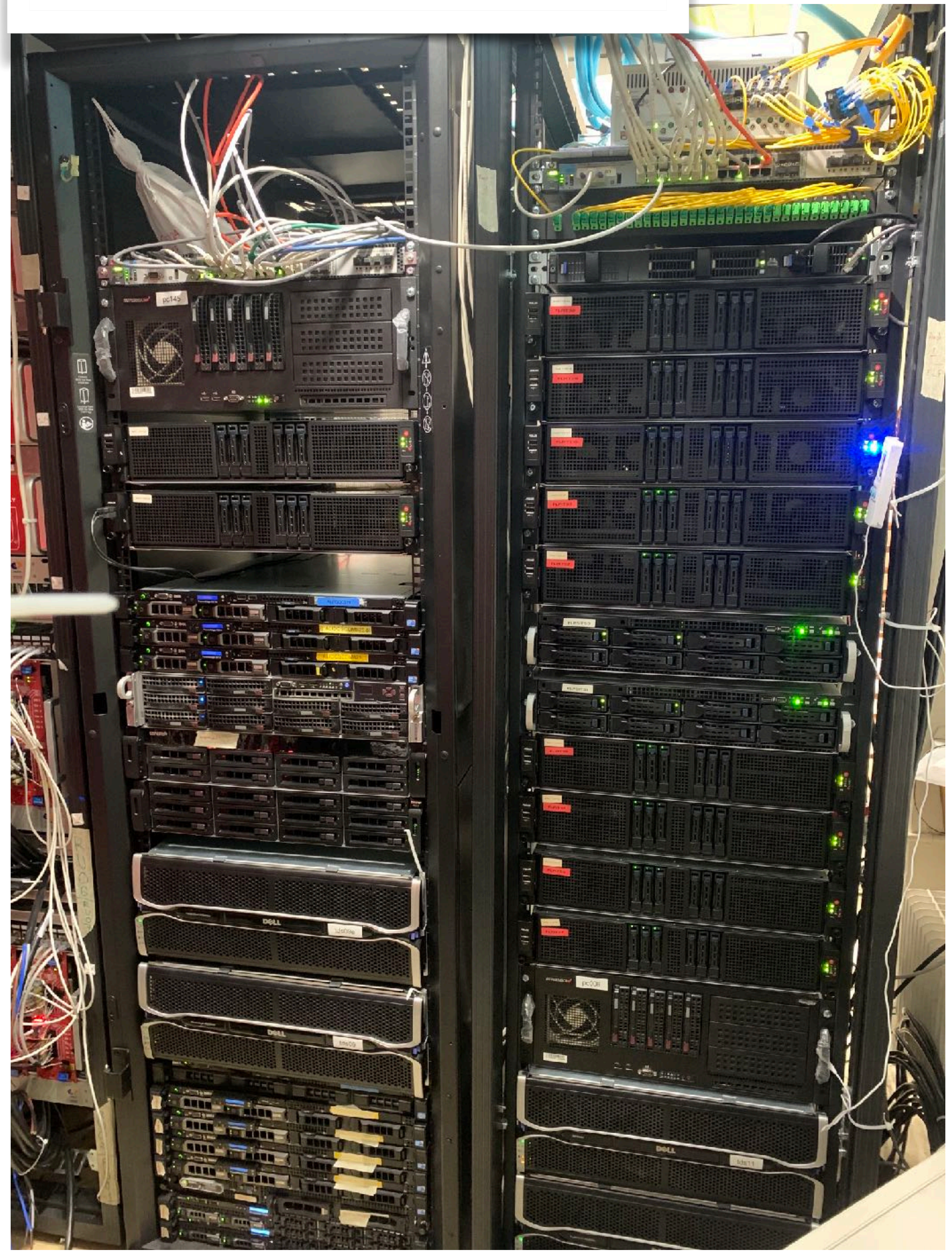


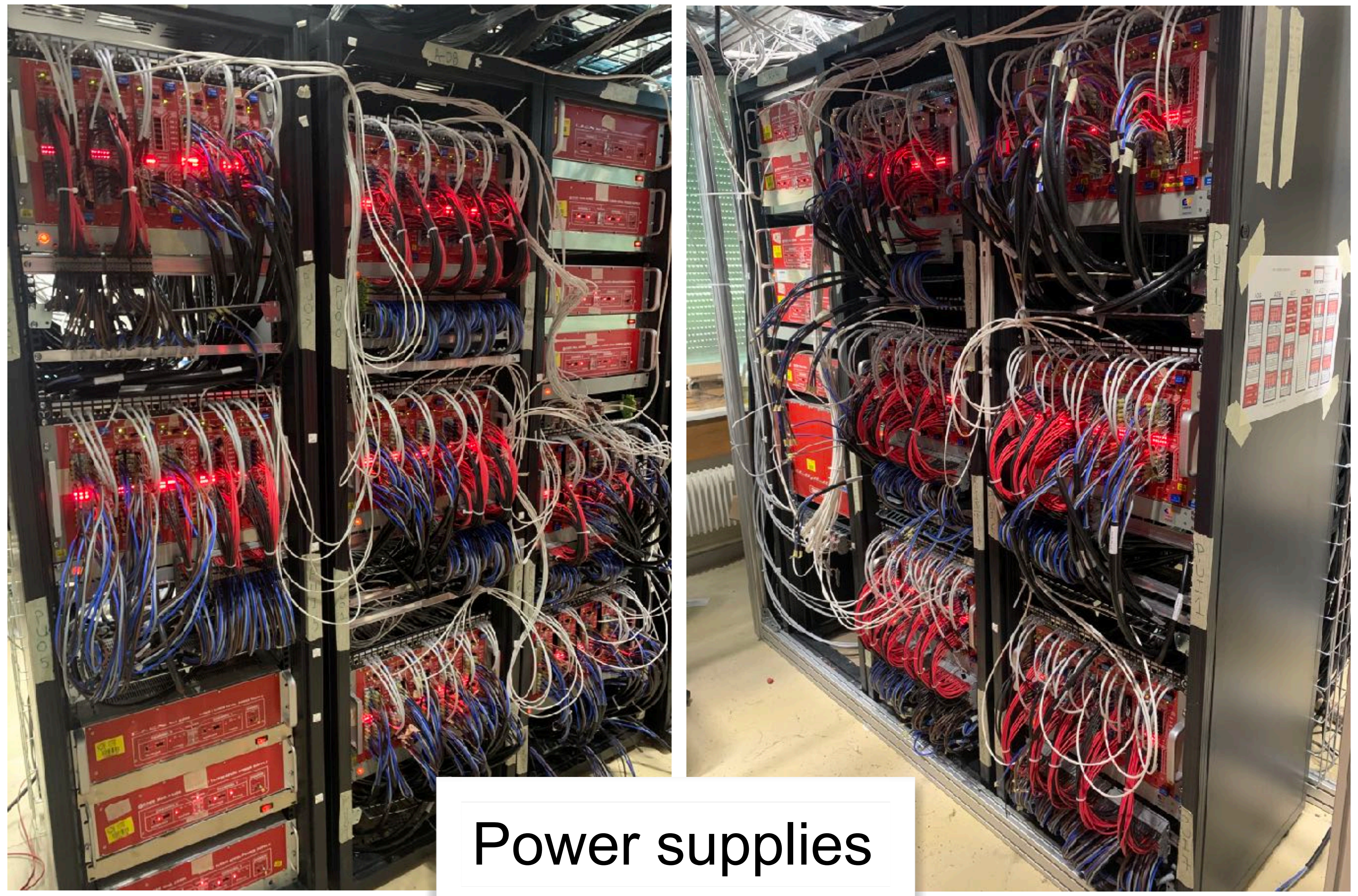
On-surface commissioning — services

Readout Units /
Power Boards



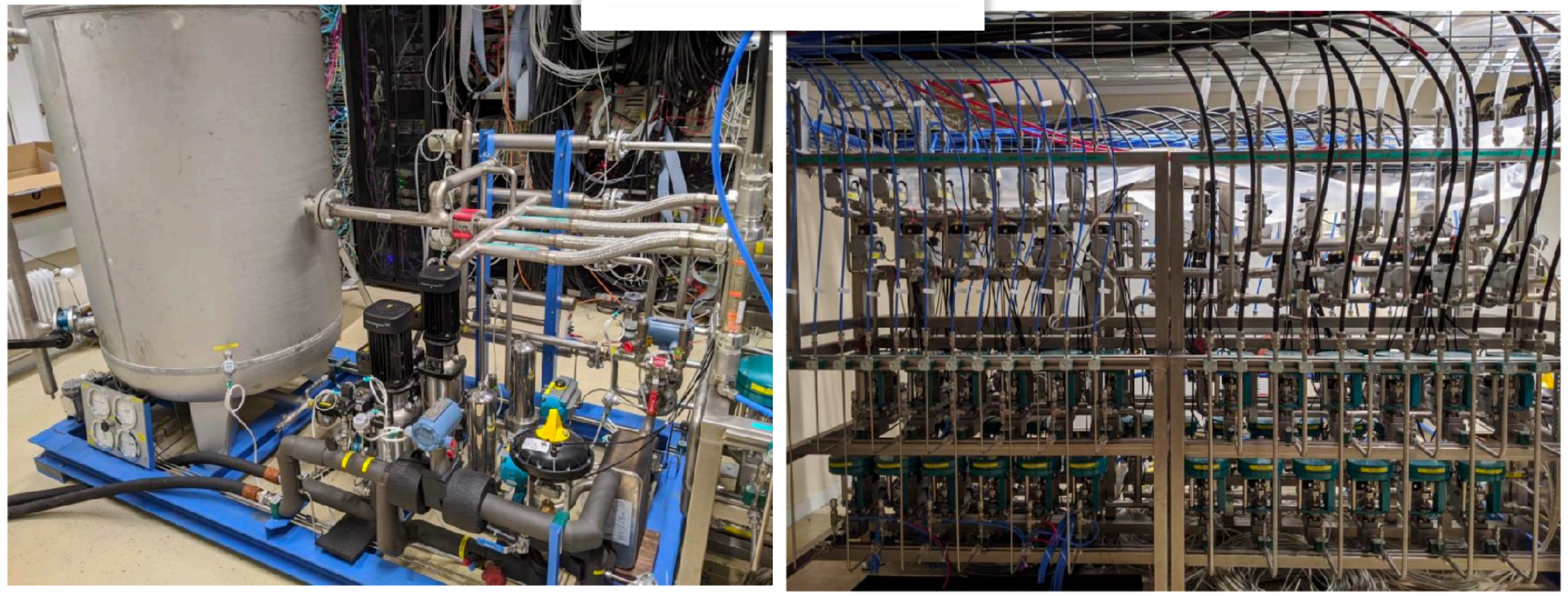
Readout / Control Servers





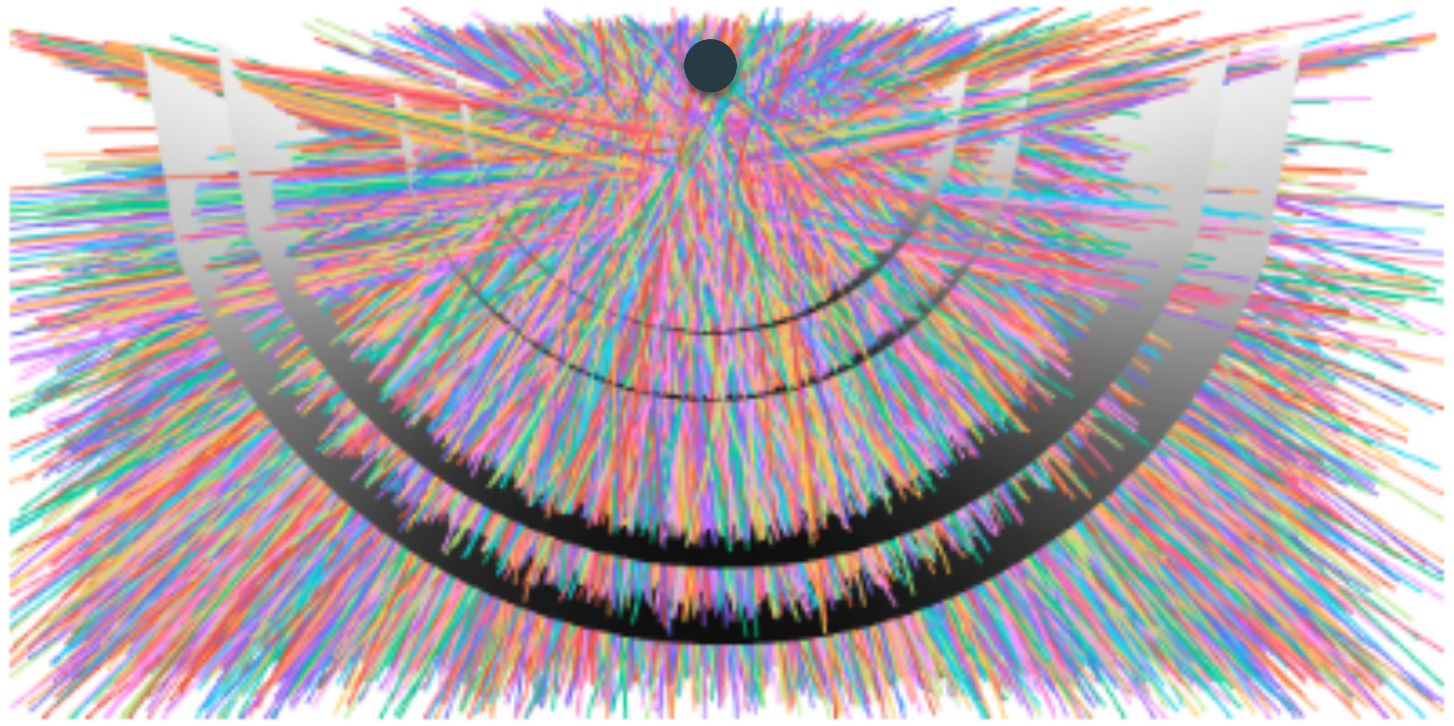
Power supplies

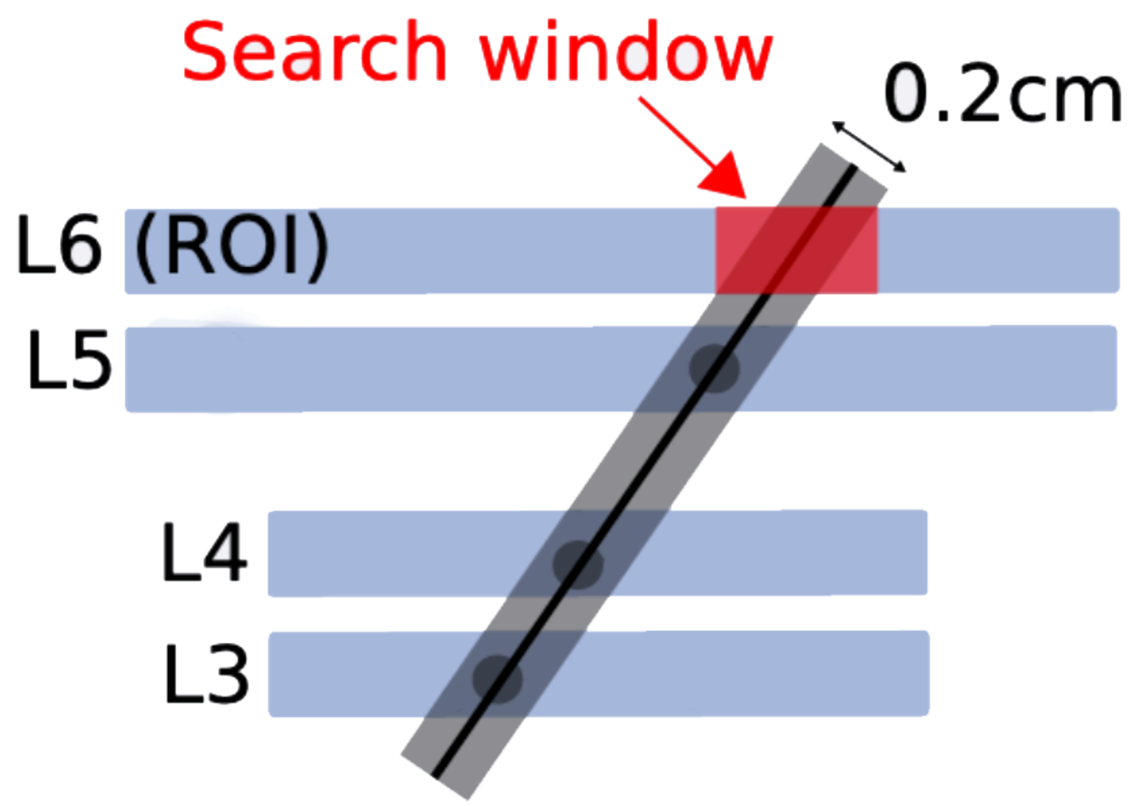
Cooling Plant



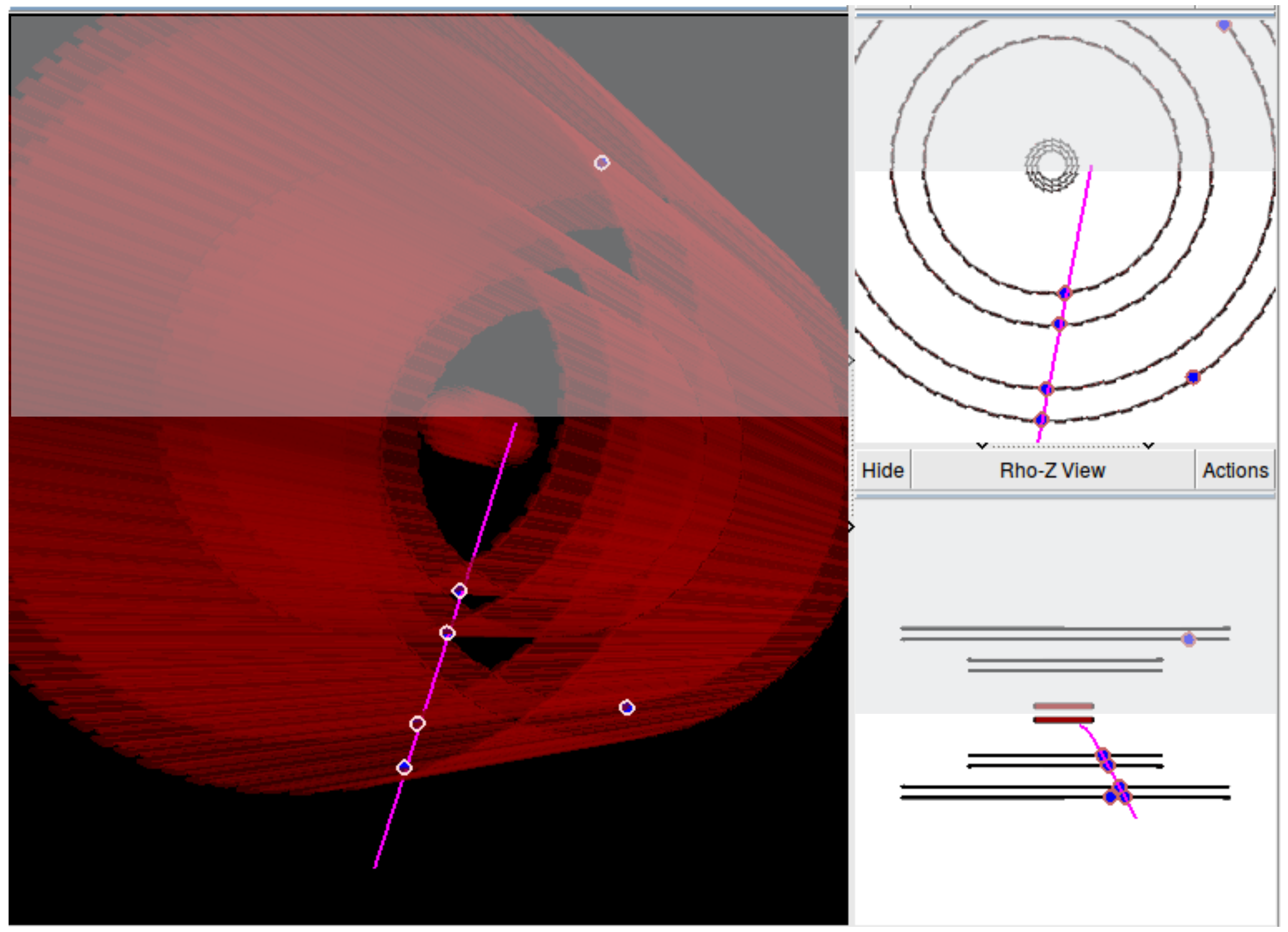
On-surface commissioning — Outer Barrel — detection efficiency

Layer	TOP	BOT
3	99.74 + 0.02 - 0.02	99.67+ 0.02 - 0.02
4	99.75 + 0.02 - 0.02	99.68 + 0.02 - 0.02
5	99.44 + 0.03 - 0.03	99.62 + 0.02 - 0.02
6	99.67 + 0.02 - 0.02	99.60 + 0.02 - 0.03



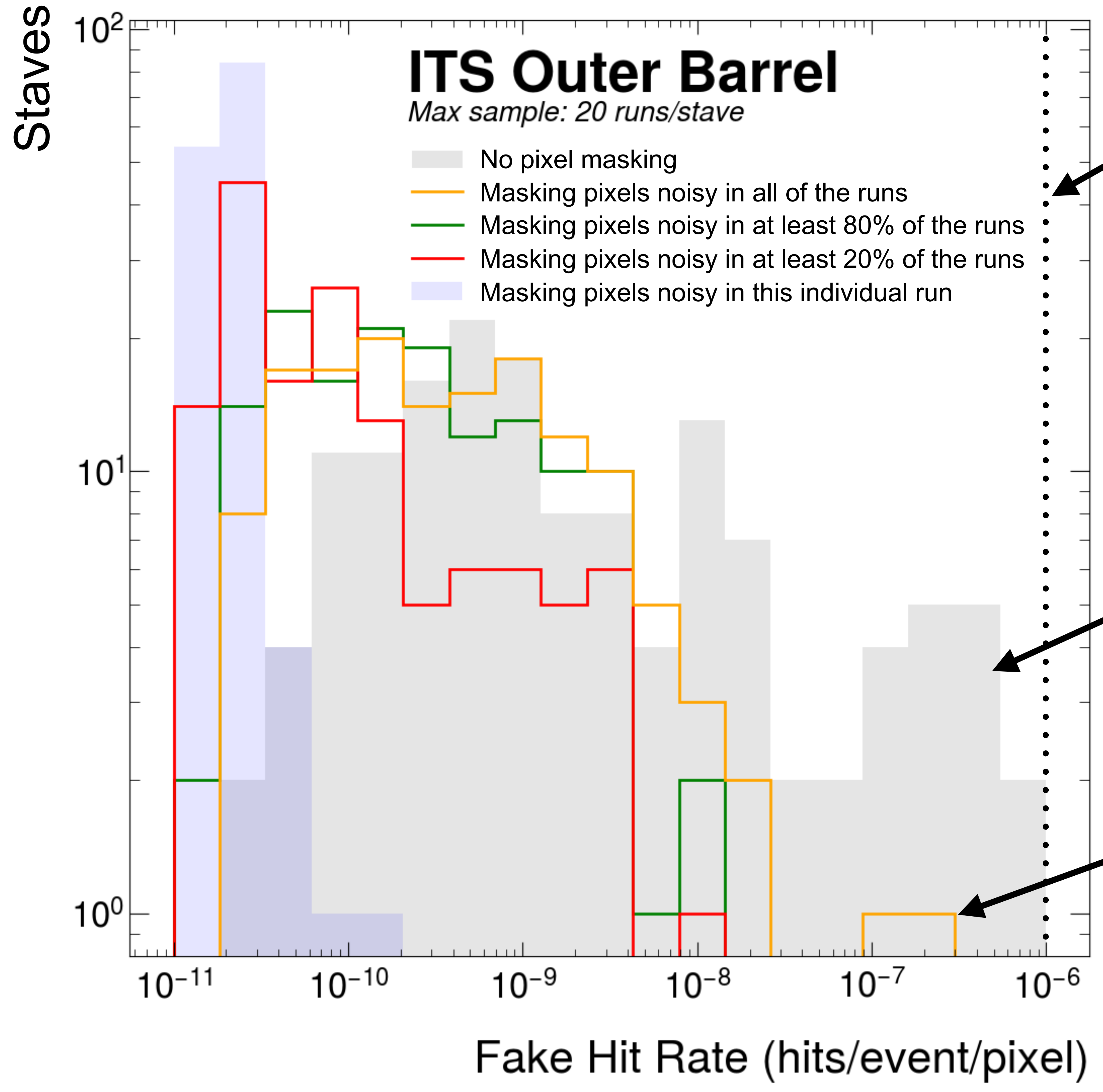


- Analysis prior to software alignment
- Hardware alignment sufficient for first studies
- Based on straight line fits through 3 out of 4 layers
- Excluding tracks in corner cases
  - – Traversing inactive chips
  - – Inter-chip gaps (enhanced due to tracks not originating from the nominal interaction point)
- **Active area shows efficiency > 99%**



Track candidate in OB Bottom Half-Barrel

On-surface commissioning — Outer Barrel — fake-hit rate

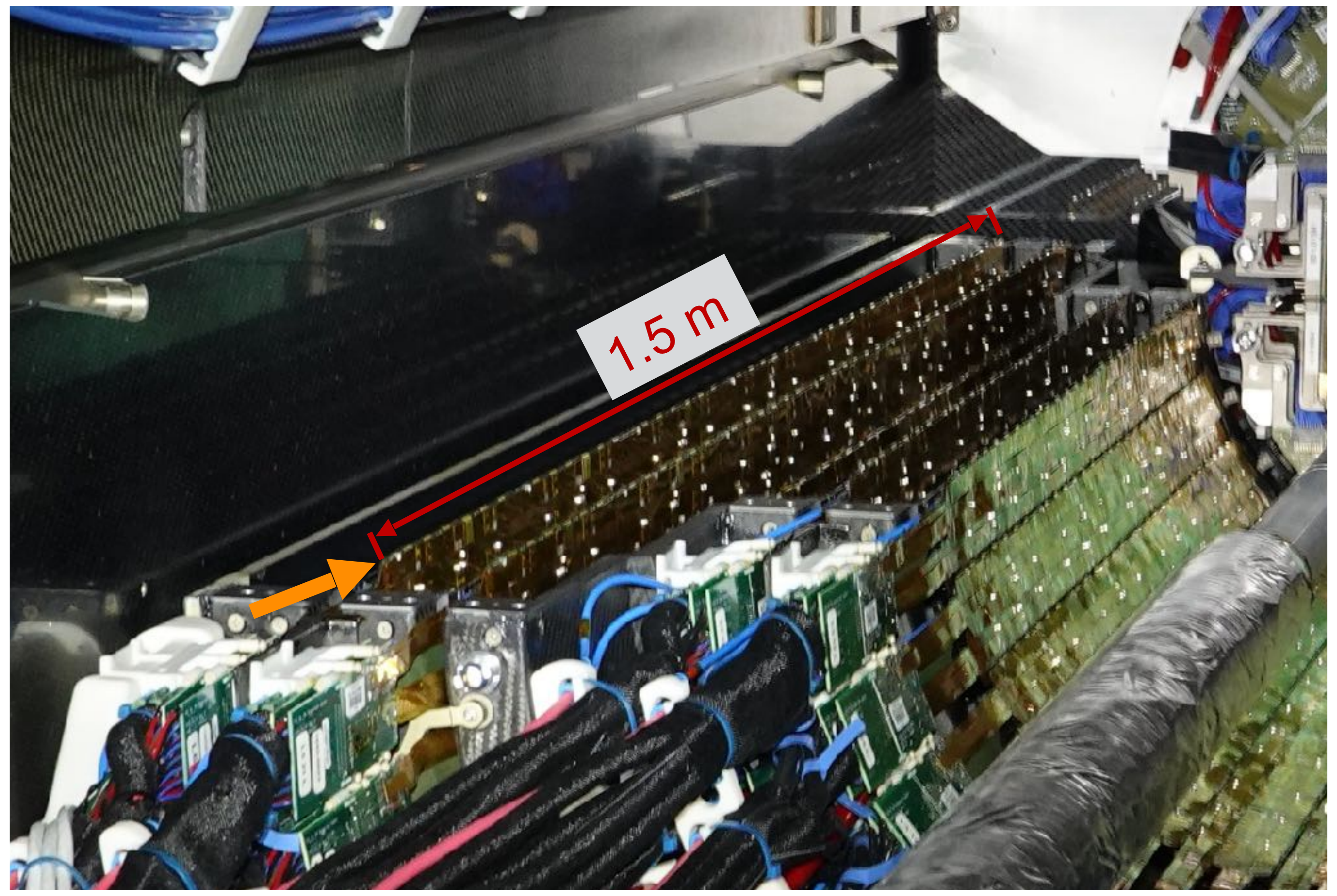


Requirement:
10^{-6} / pixel /event

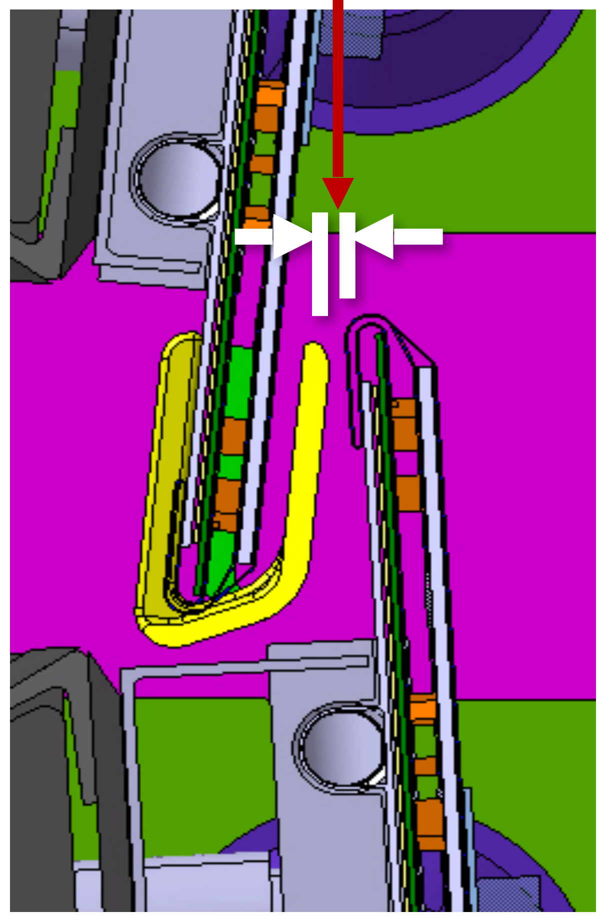
- Measured fake-hit in multiple runs per stave
- Calculation of fake-hit rate applying different masking schemes offline:
  - No pixel masking (■), excluding only faulty double columns)
    ⇒ Meeting requirement
  - Masking pixels found noisy in all runs (—):
    - Fraction of permanently noisy pixels
    - Estimate for the performance achievable with online / hardware in-pixel masking:
      vast majority of staves < 10^{-7} / pixel /event
      ⇒ possible to run the detector w/ a static mask
  - Masking pixels present in 80% (—) and 20% (—) further improves the fake-hit rate
  - Masking based on an individual run leads to a fake-hit rate of 10^{-10} / pixel / event

Installation — challenges

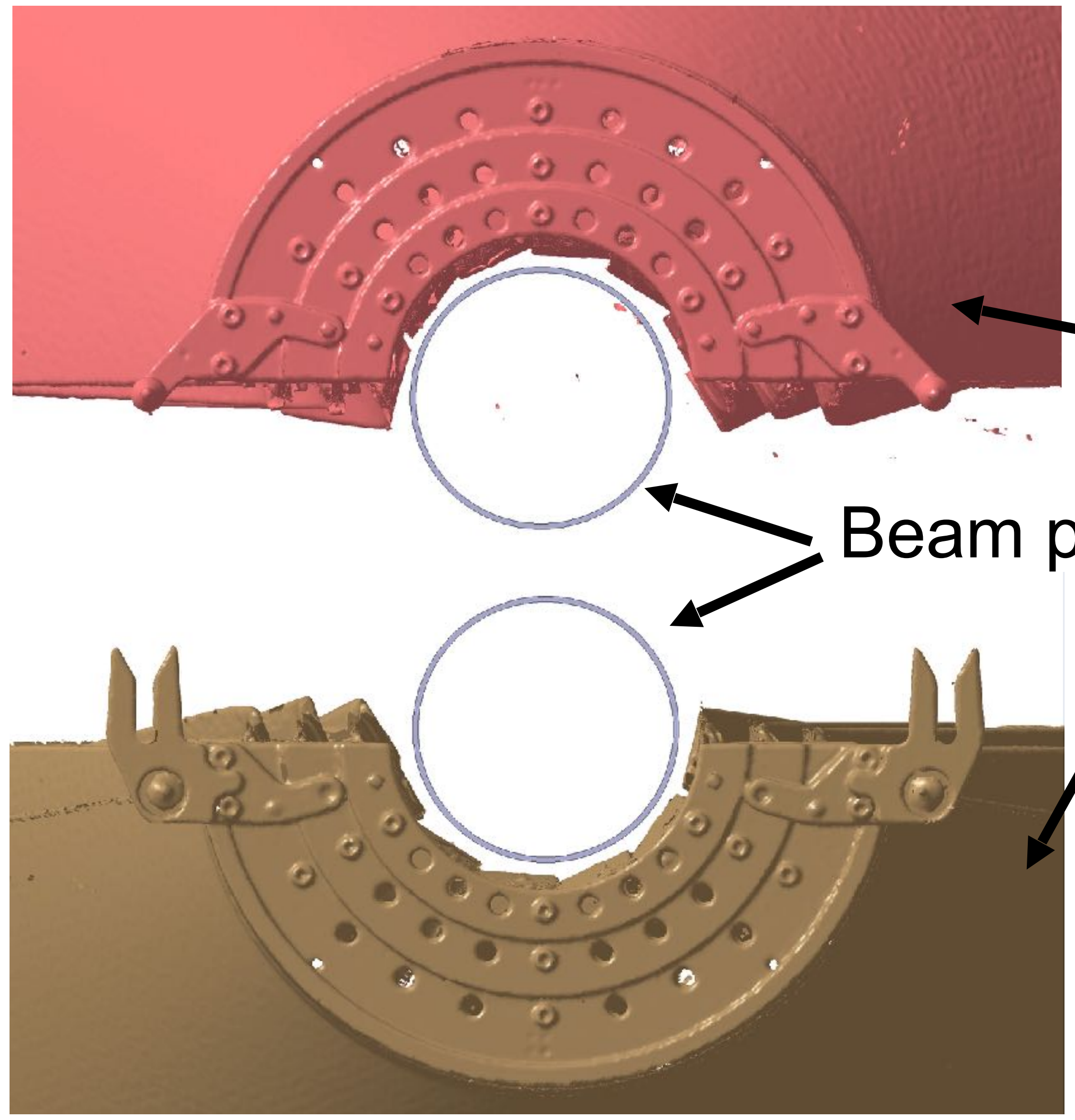
- Precise positioning of fragile objects inside the TPC bore
  → manipulating from a few meters distances
  → difficult to actually see the position by eye
- Use of 3d scans, surveys and cameras



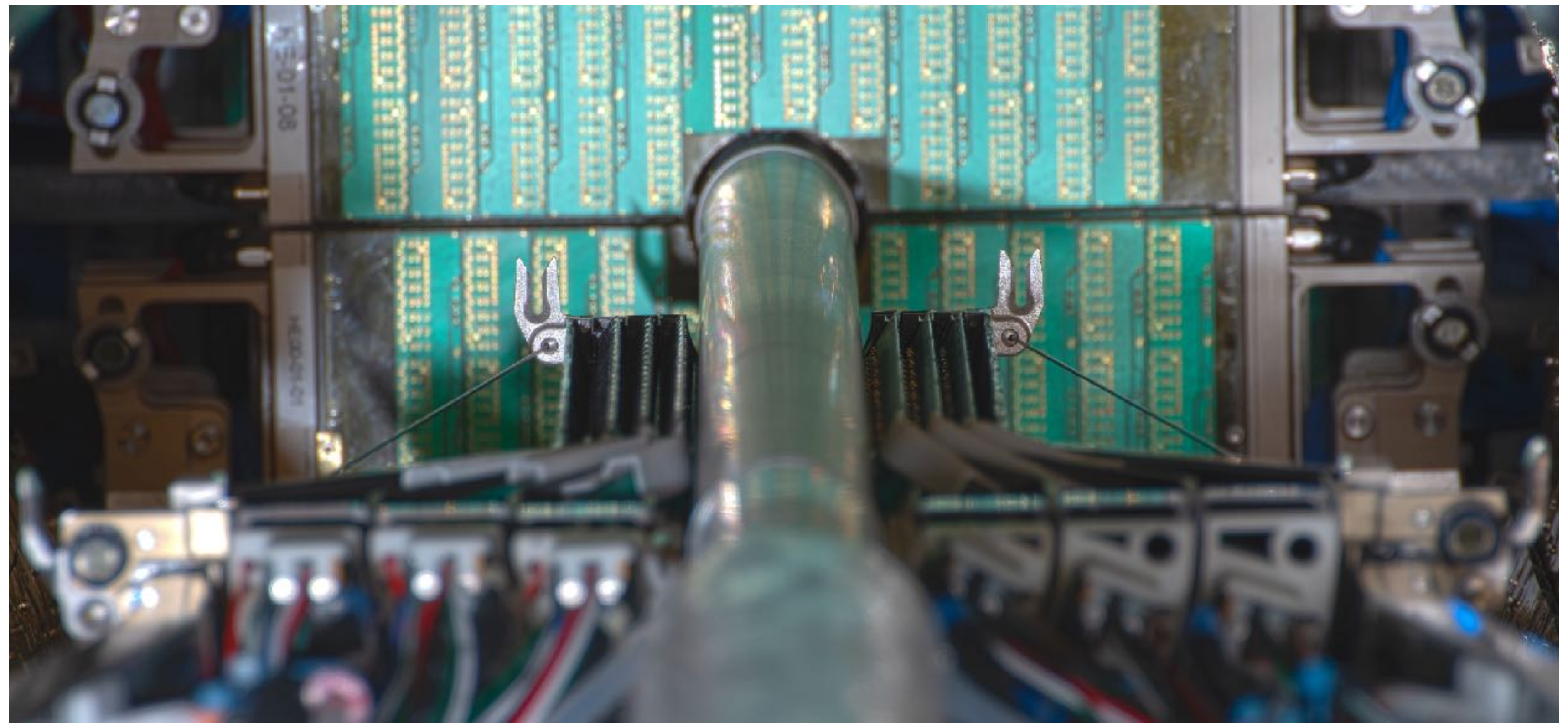
OB stave edge


1.2 mm nominal clearance

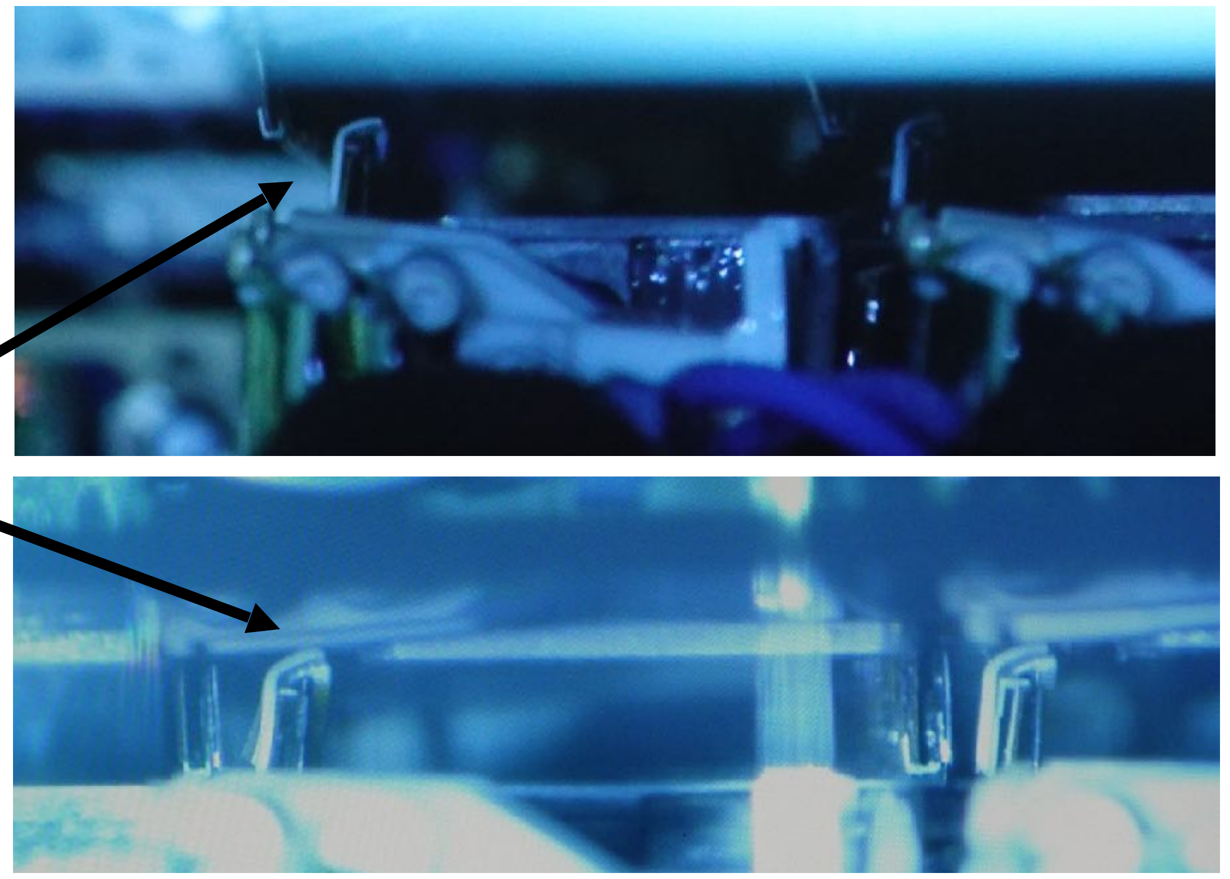
OB stave edge clearance when fully mated



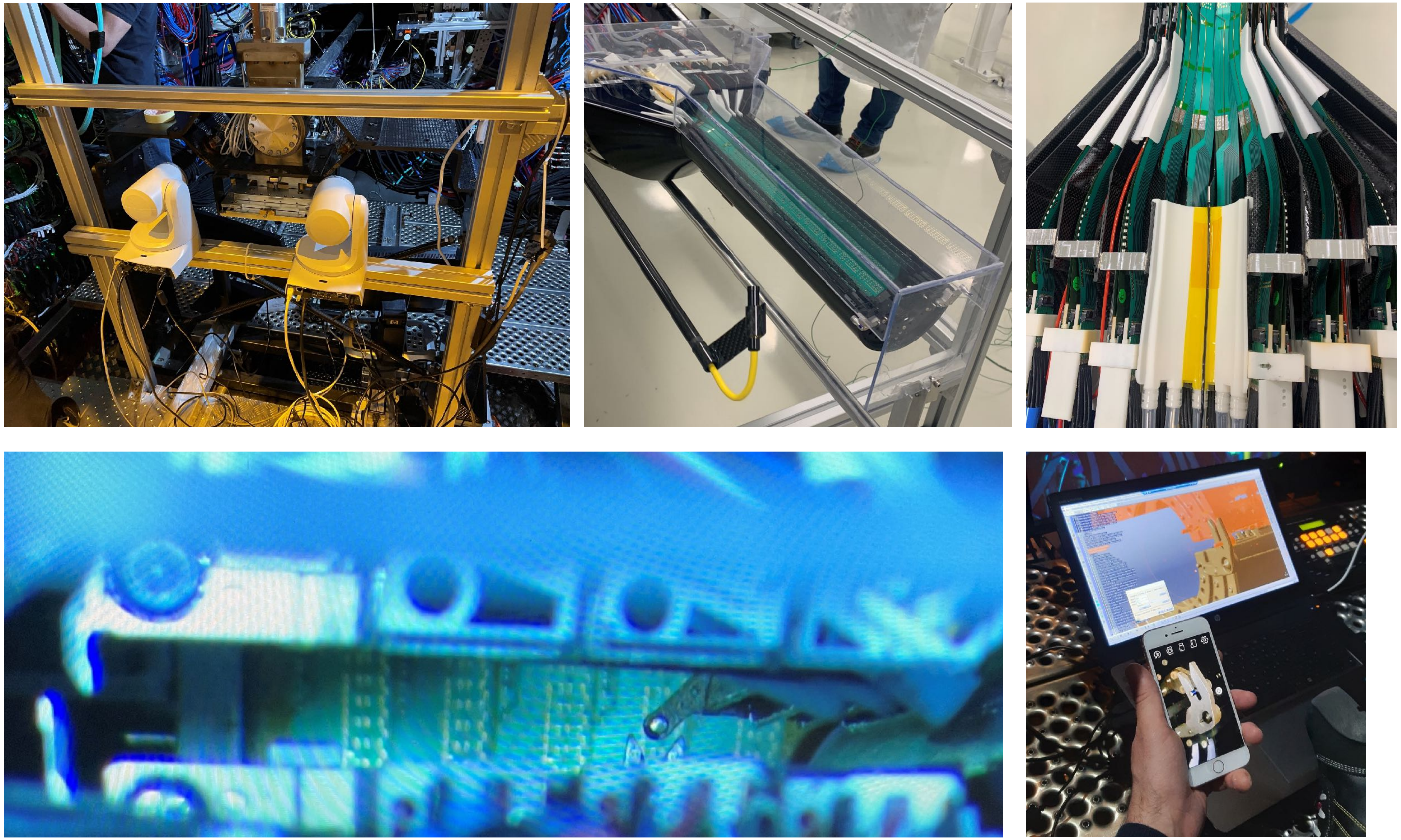
3d scans of IB Half-Barrels next to beam pipe, based on survey



IB Bottom in the final position

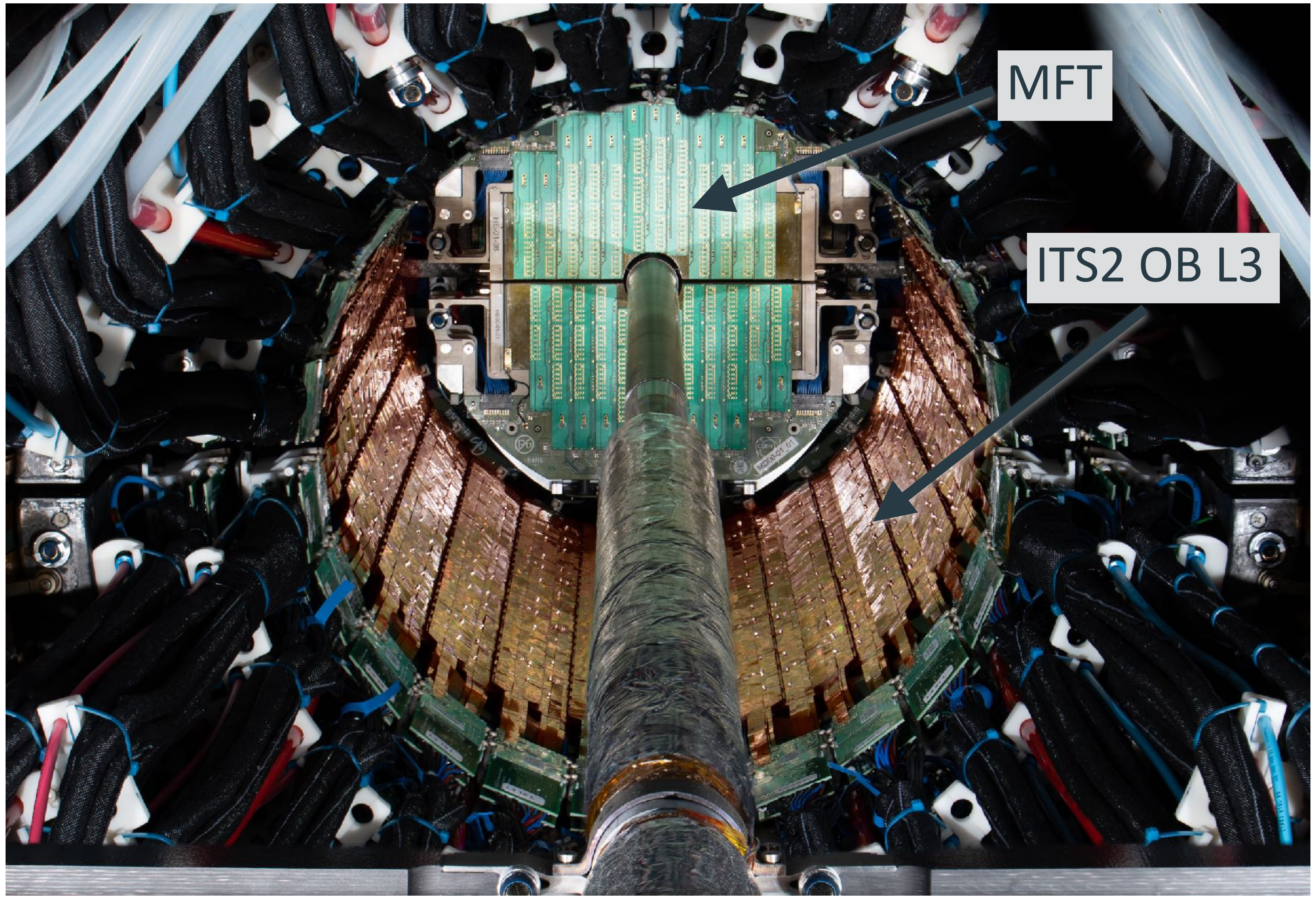


Inner Barrel final positioning

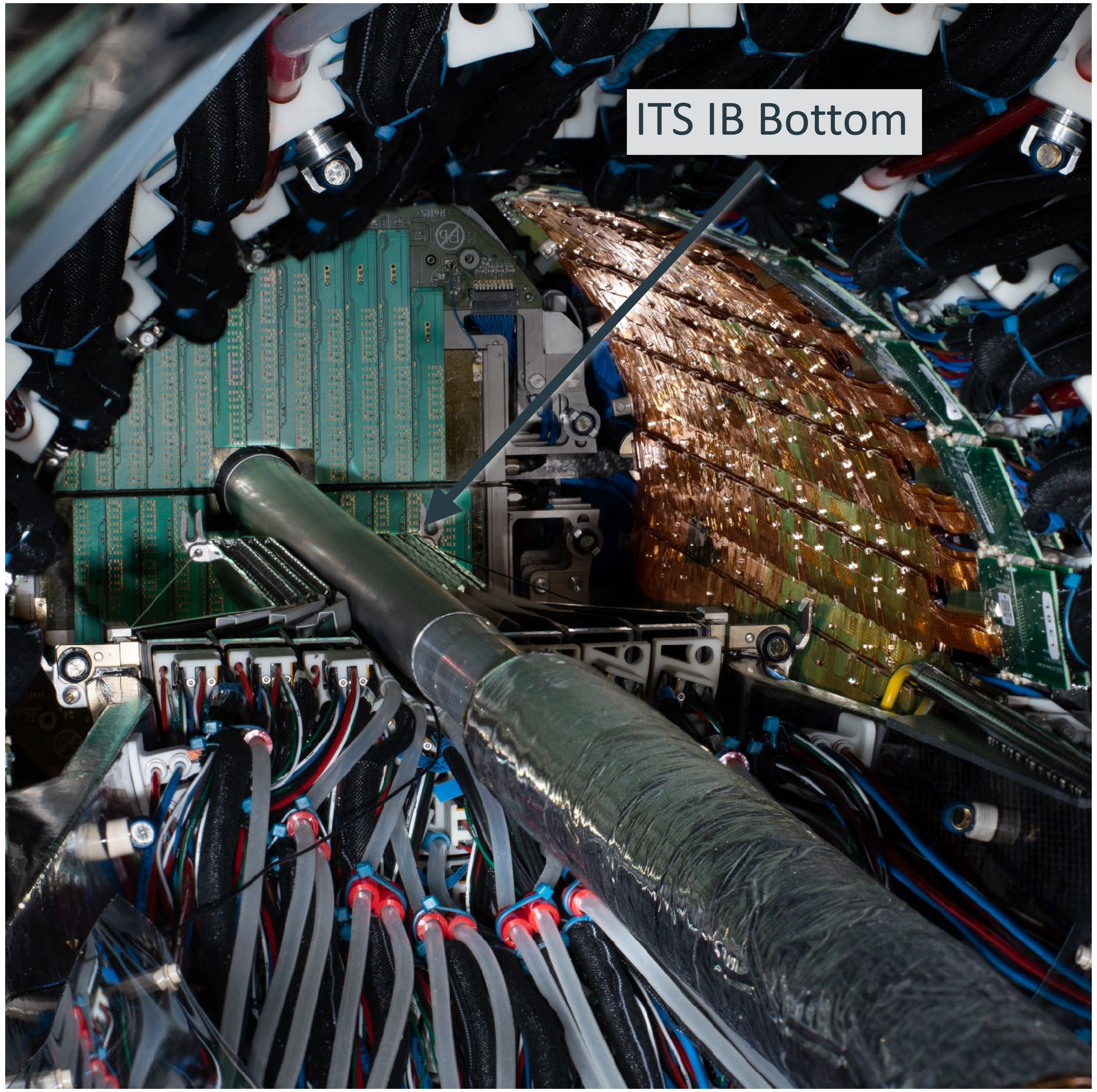


Real time verification using 6 cameras
+ comparison to 3D CAD scans

ITS2 in the ALICE experimental apparatus



ITS Outer Barrel surrounding the beam pipe, MFT in the back



ITS Inner Barrel Bottom and Outer Barrel

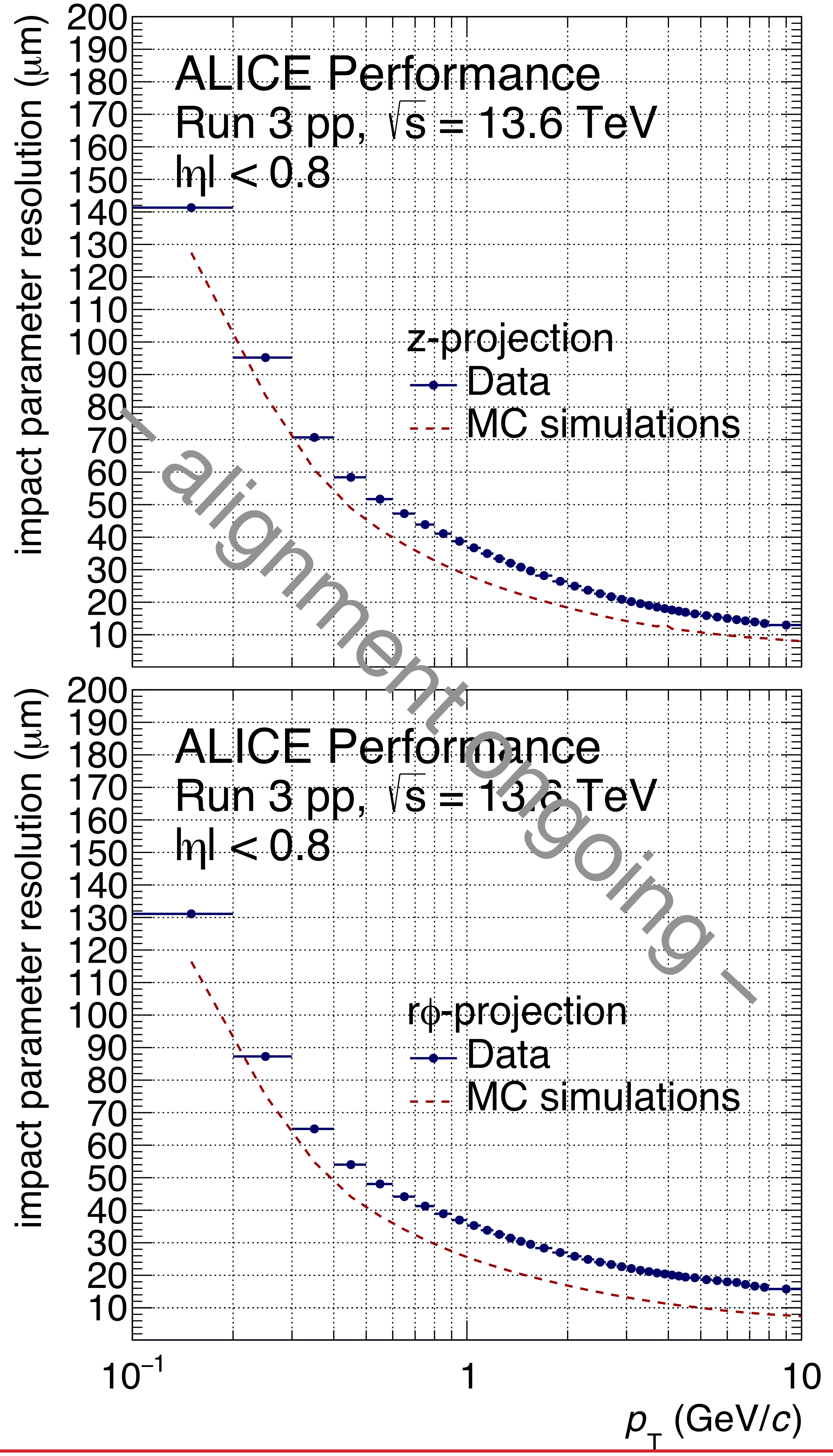
ITS Outer Barrel installation website

ITS2 offspring — example sPhenix

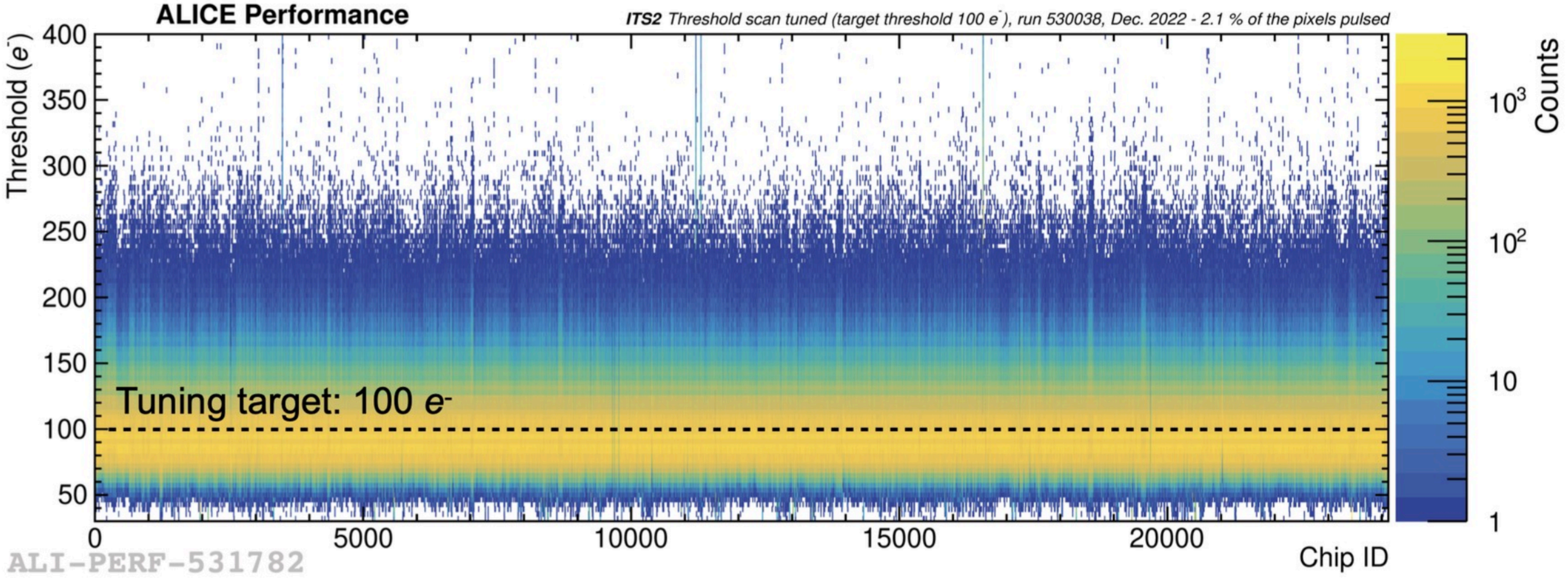
replica of ITS2 Inner Barrel (3 layers) – installed in Mar’23

ALICE ITS2 — Performance

- Stable operation of 24k chips
- >99% functional pixels
- Very low fake hit rate: < 10^{-8}/pixel/event
- Tuned and stable thresholds



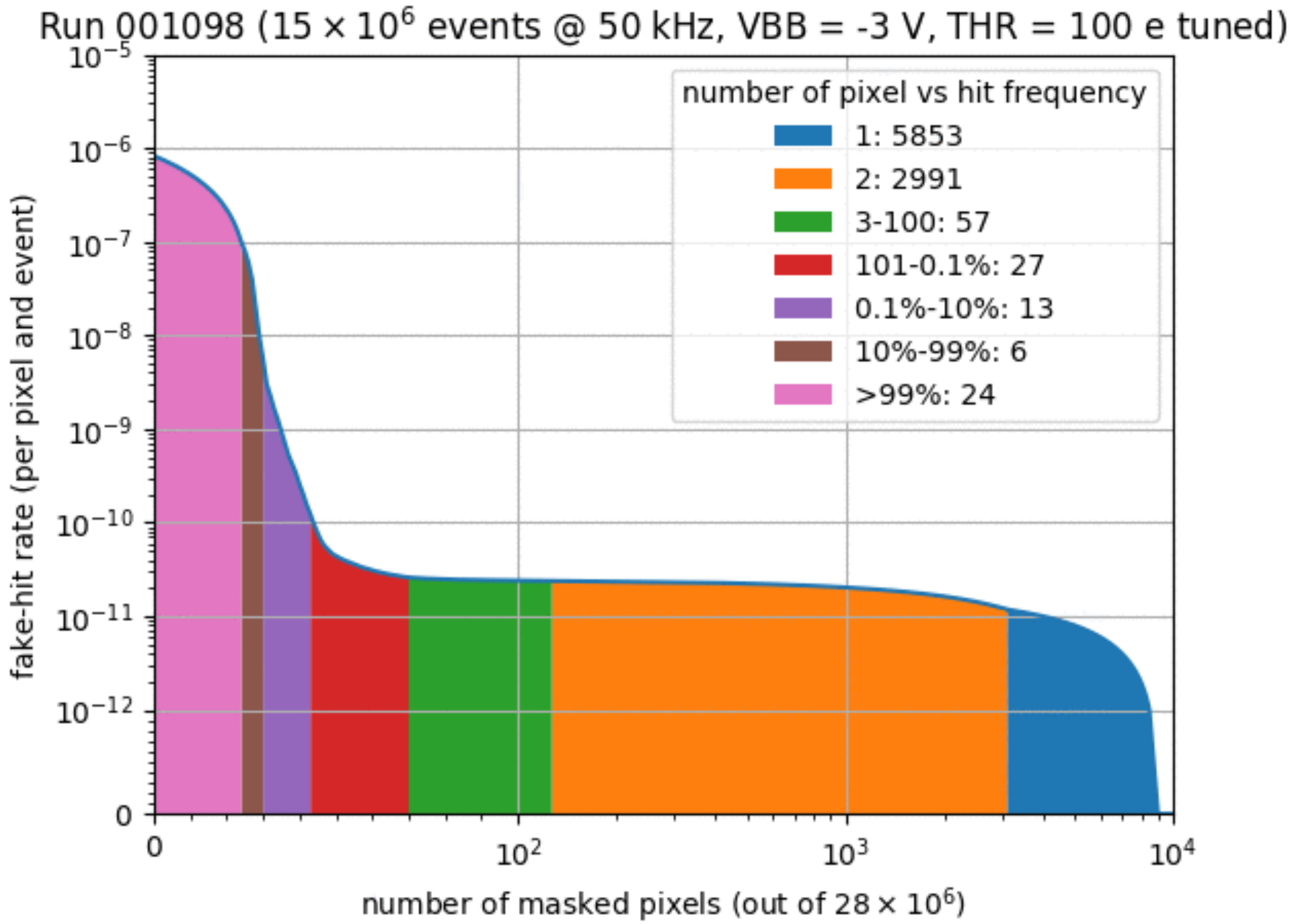
– alignment ongoing –



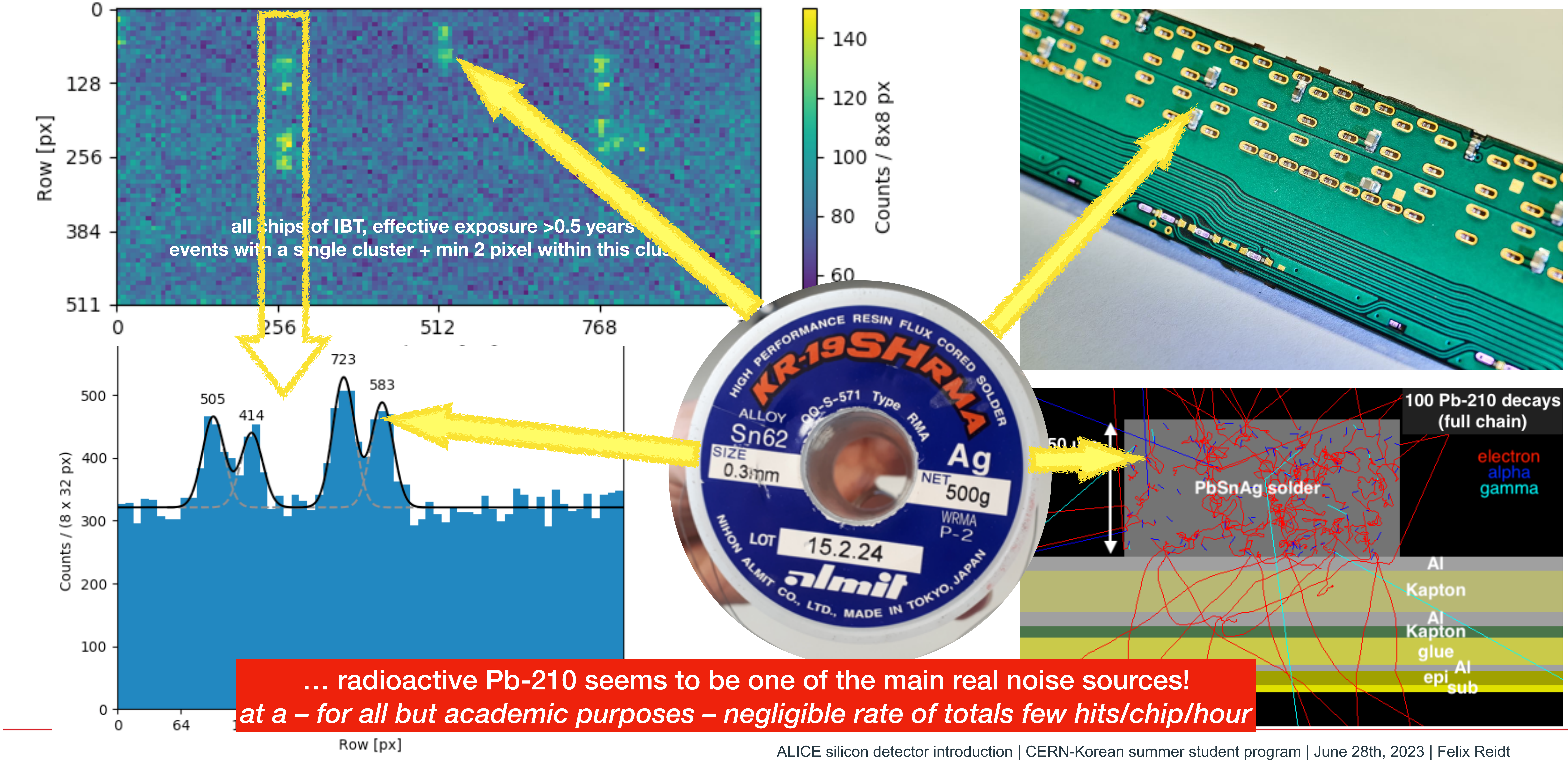
ALI-PERF-531782

ALICE ITS2 — Performance (2)

- This is the real rate measured on-detector, including final services
- Essentially, apart from a hand-full pixels per chip, the detector is **noise-free**
- Biggest contributor is natural radiation (which is *not* excluded here)



ITS2 performance — the noise floor is really that low



… radioactive Pb-210 seems to be one of the main real noise sources!

at a – for all but academic purposes – negligible rate of totals few hits/chip/hour

ALICE

Pb-Pb 5.36 TeV

LHC22s period

18th November 2022

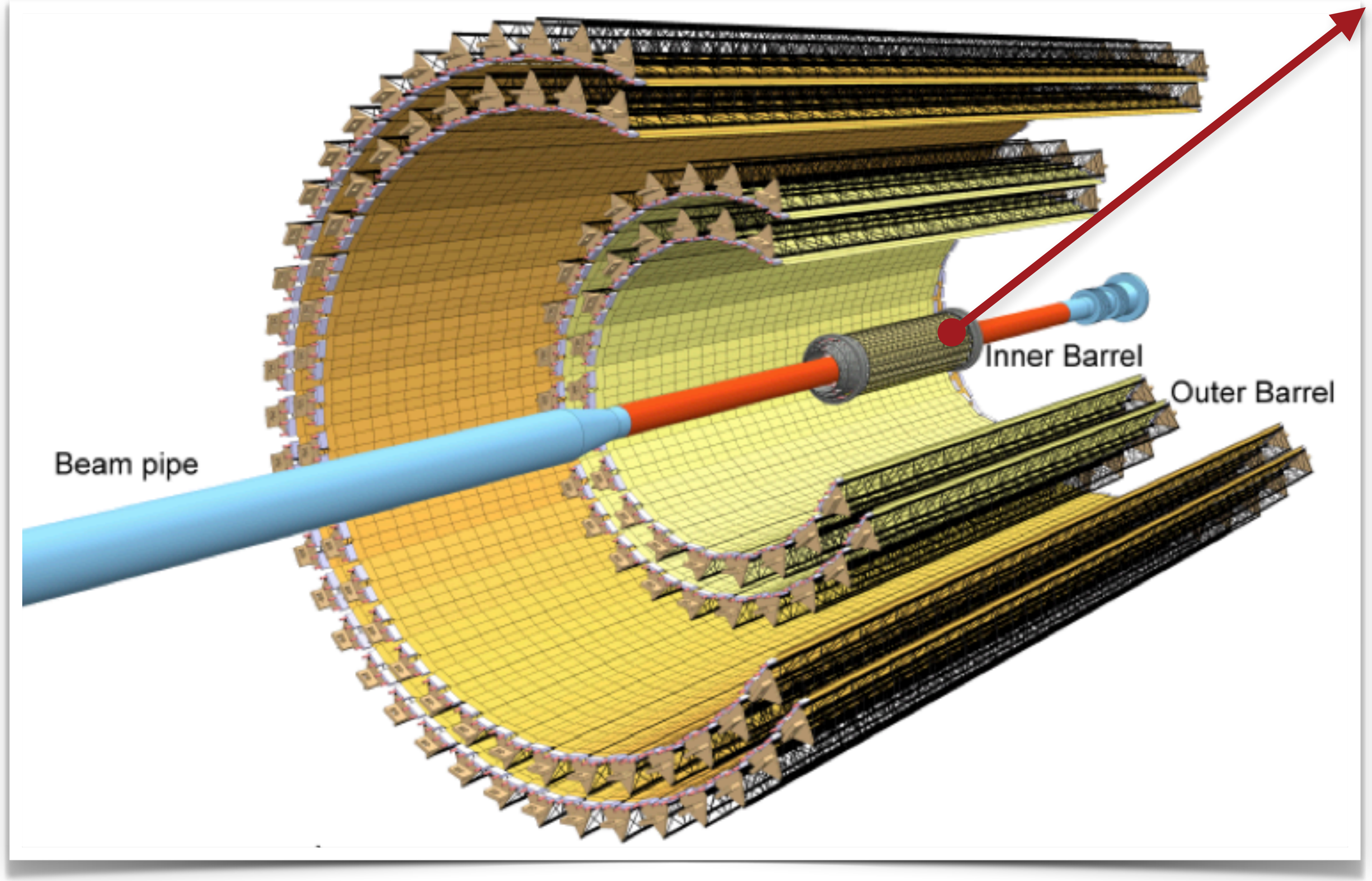
16:52:47.893

ITS3

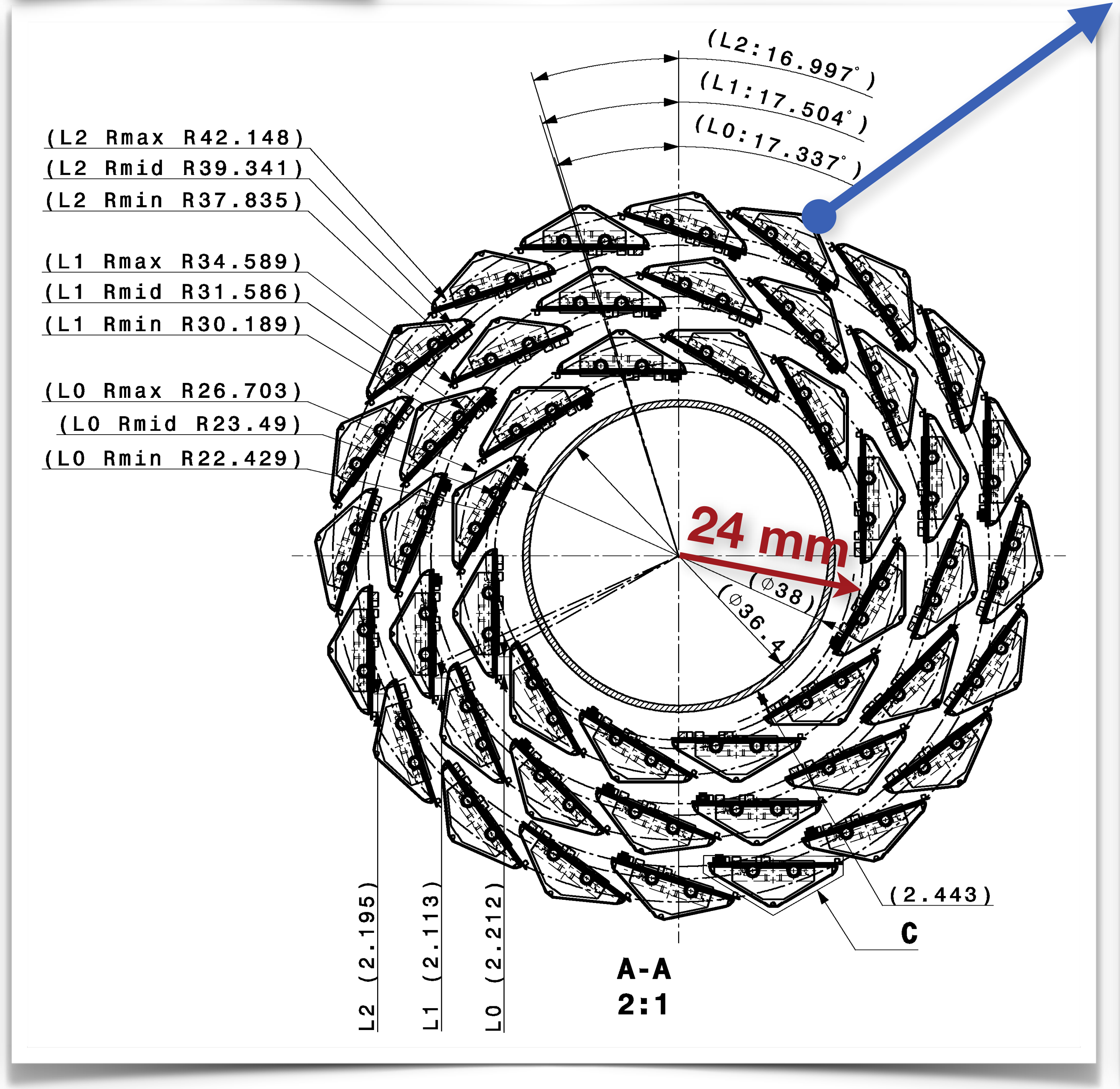
ITS3 Detector Seminar: https://indico.cern.ch/event/1071914/

How to improve on ITS2?

ITS2 layout



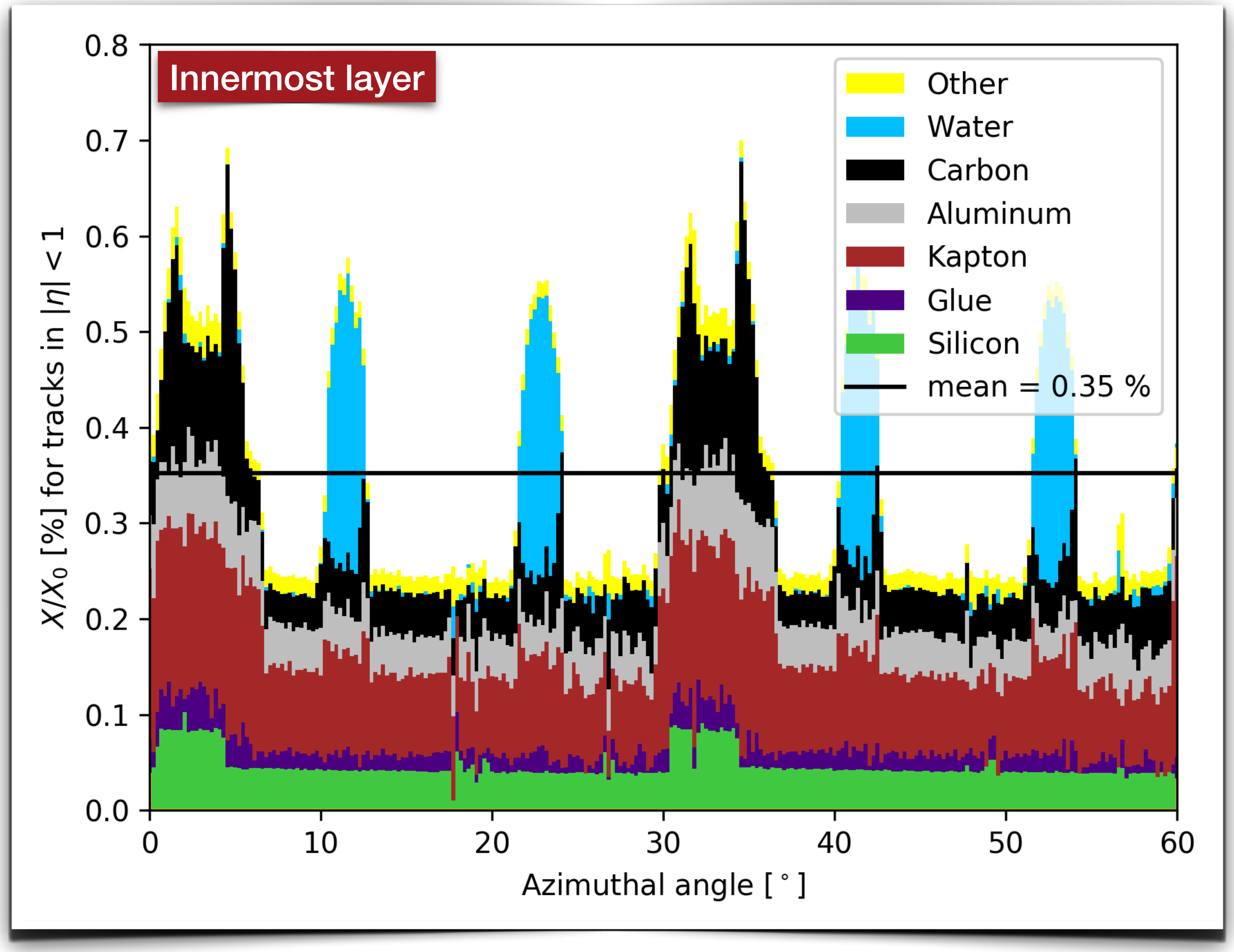
Inner barrel



Layer 2 (20 staves)

- ITS2 is ultralight but densely packed
  → **Can the material be further reduced?**
- **Can we get closer to the interaction point?**

Material budget

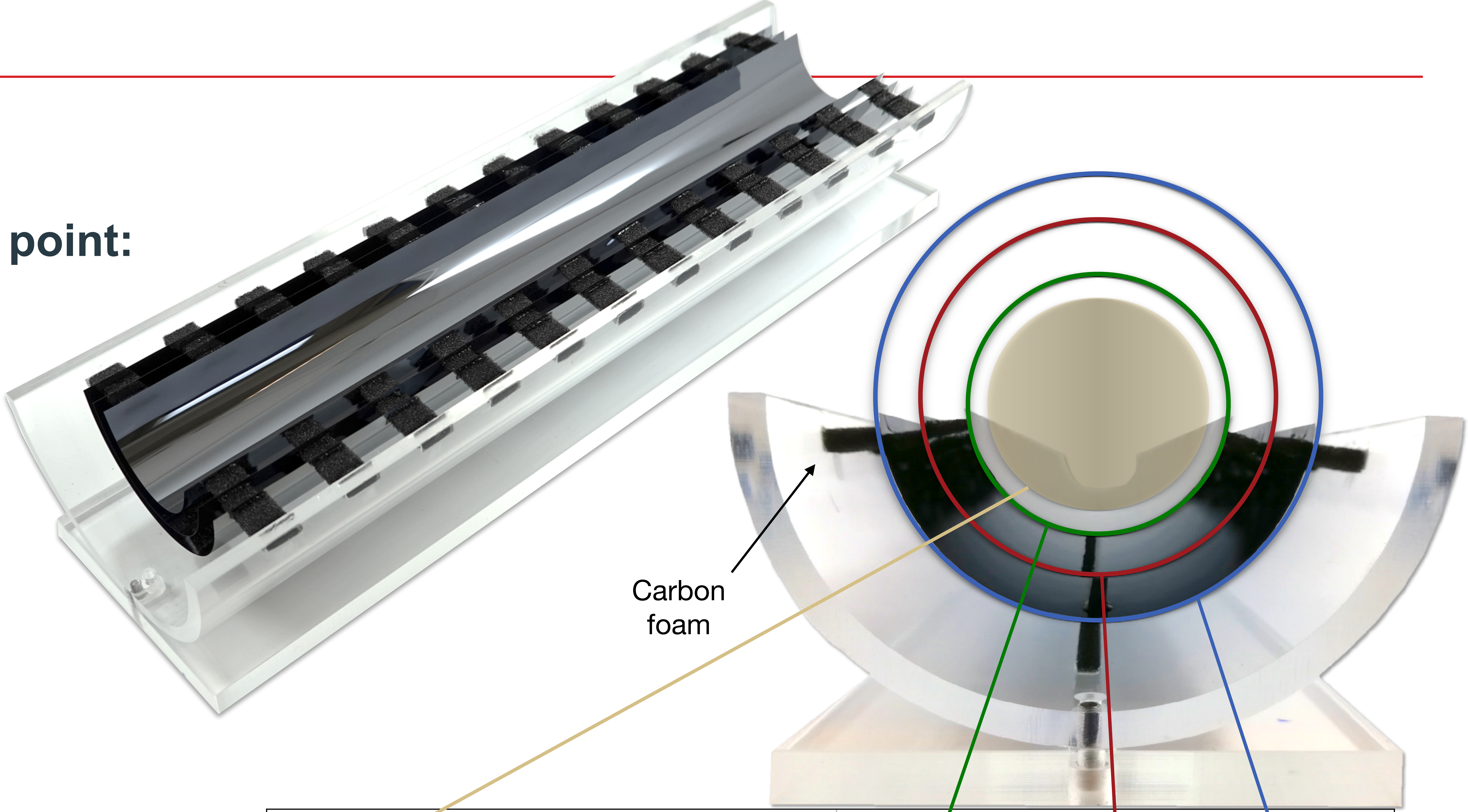


- Observations:
  - Si makes only $^1/_7$-th of total material budget
  - Non-uniformity due to support, cooling & overlaps
- Removal of water cooling:
  - If **power consumption < 20 mW/cm^2**
- Removal of the circuit board for power & data:
  - If **integrated on chip**
- Removal of mechanical support:
  - **Self-supporting arched structure**

ITS3 layout

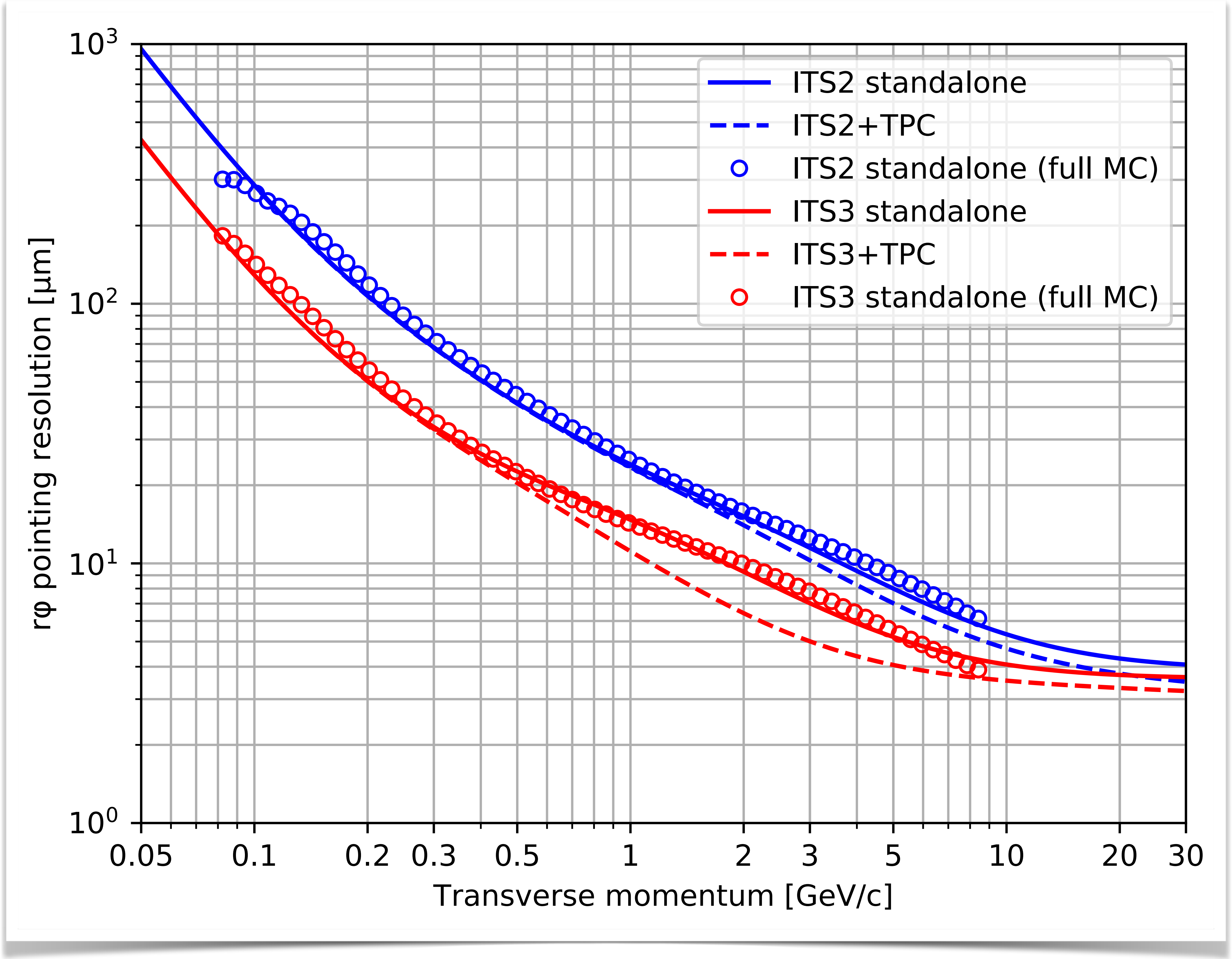
- **Getting closer to interaction point:**
  - Beam pipe radius
    18.2 → 16.0 mm
  - Layer 0 position
    24 mm (mean) → 18.0 mm

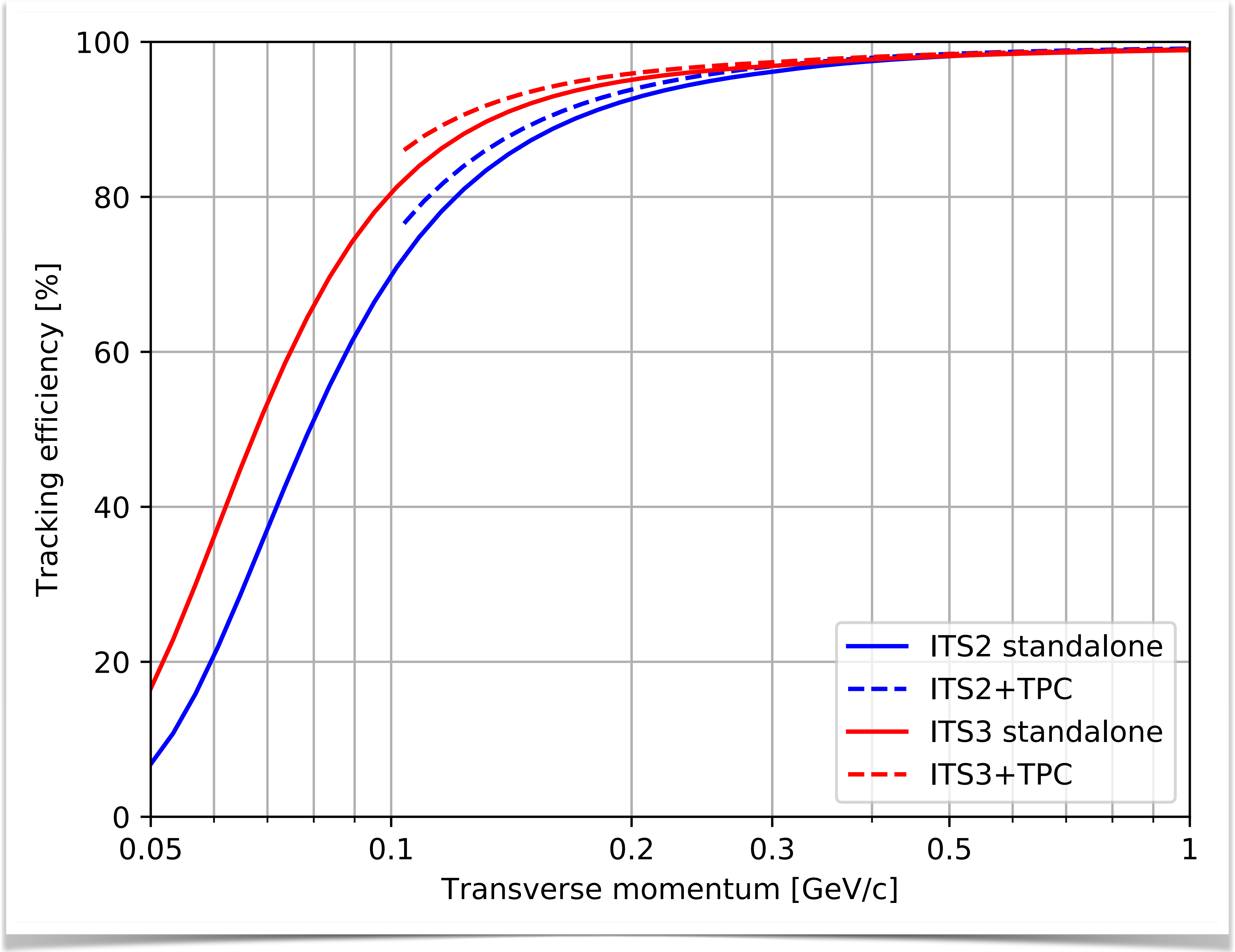
- **Reducing material budget:**
  - Beam pipe thickness
    800 → 500 µm (0.14% X_0)
  - Layer thickness
    0.36 → < 0.05% X_0



Beam pipe inner/outer radius (mm)	16.0/16.5		
Layer parameters	**Layer 0**	**Layer 1**	**Layer 2**
Radial position (mm)	18	24	30
Pixel sensor dimensions (mm^2)	270 x 56	270 x 74	270 x 93
Number of pixel sensors	2		
Pixel size (µm^2)	O(20 x 20)		

Performance gain of ITS3 over ITS2





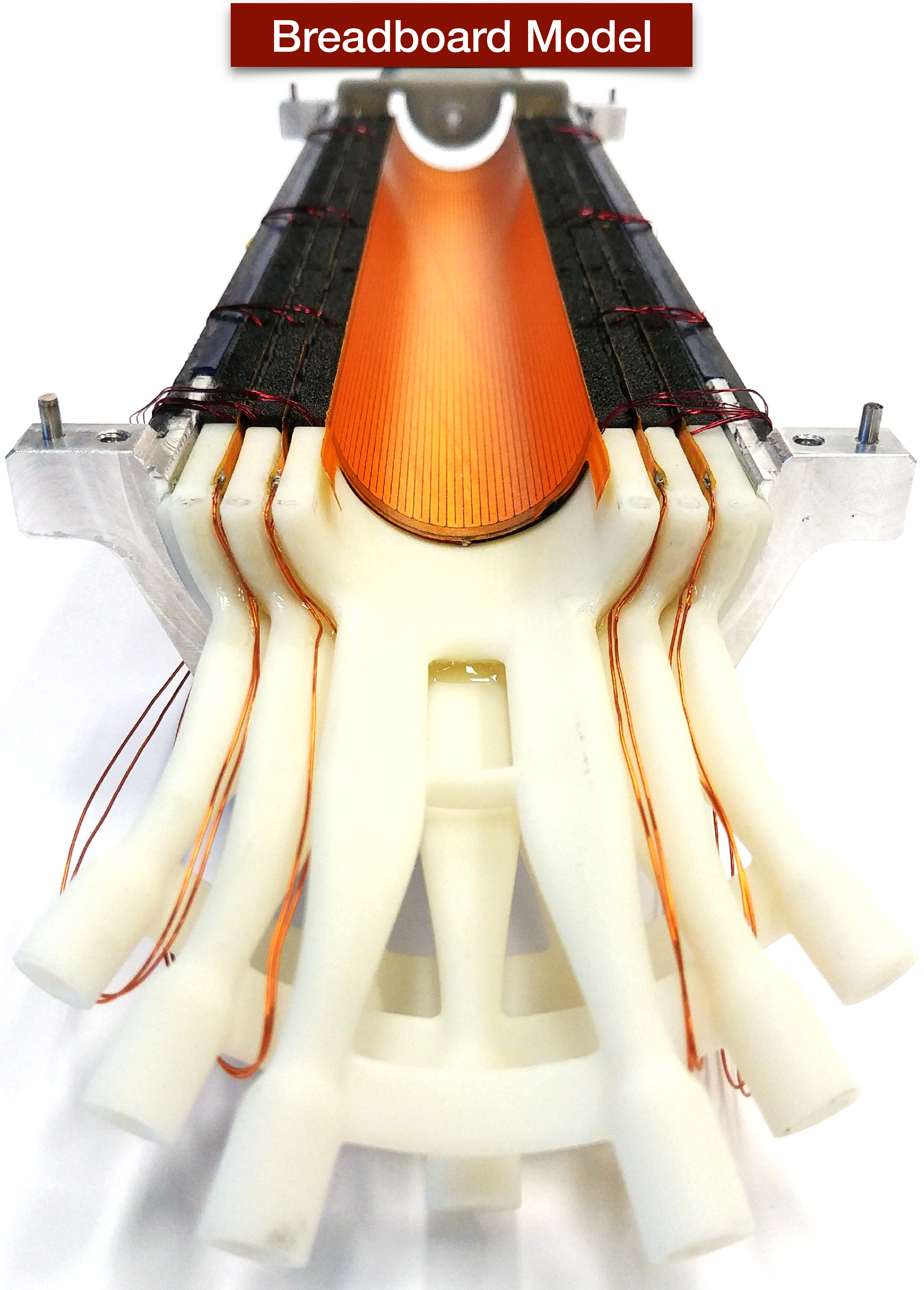
[ALICE-PUBLIC-2018-013]

- Pointing resolution 2x better
- Improved tracking efficiency for low momenta

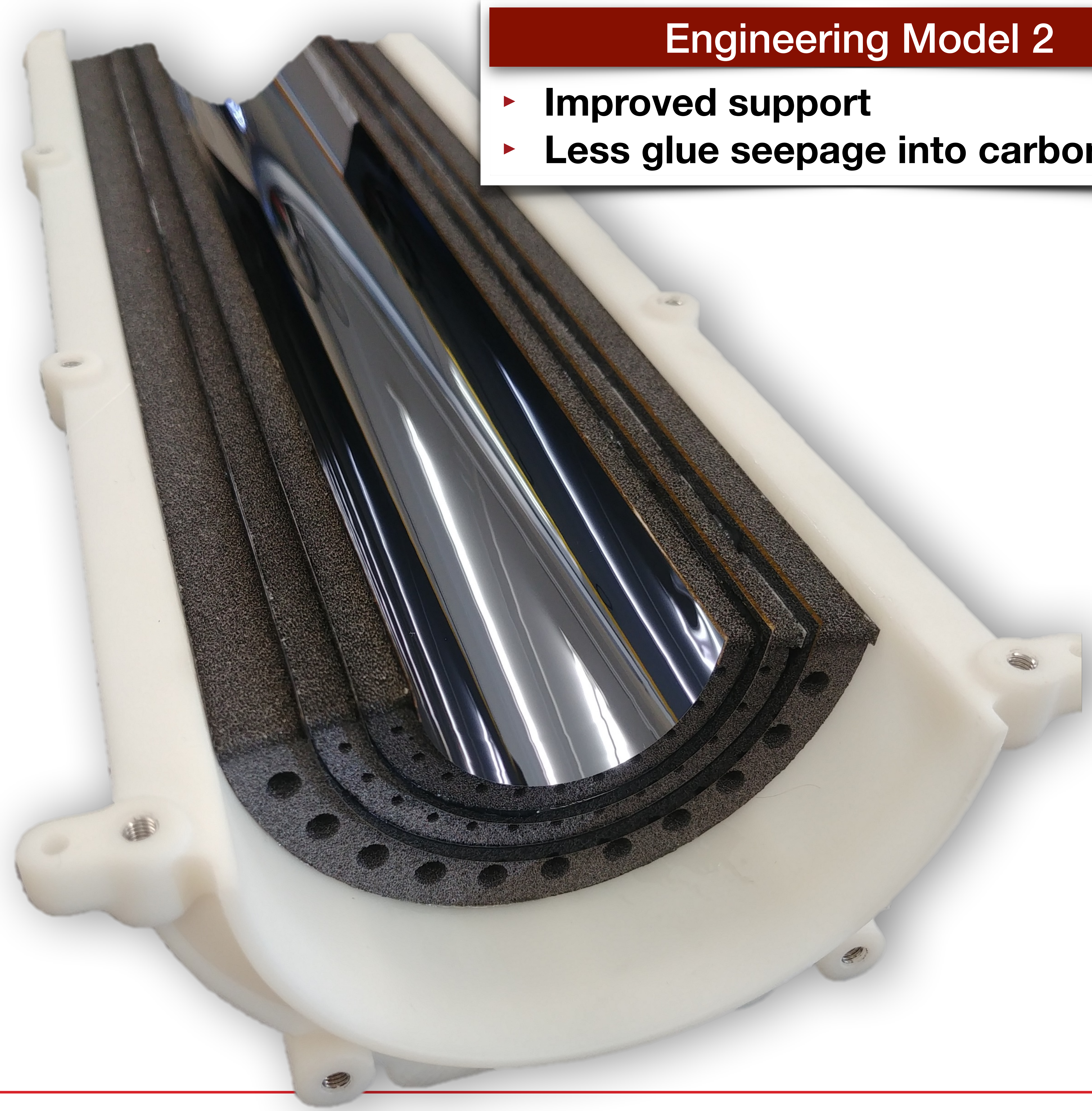
- Improved physics performance for heavy-flavour baryons and low-mass dielectrons

(EOI: ALICE ITS Upgrade in LS3,ALICE-PUBLIC-2018-013)

Mechanical models



Breadboard Model



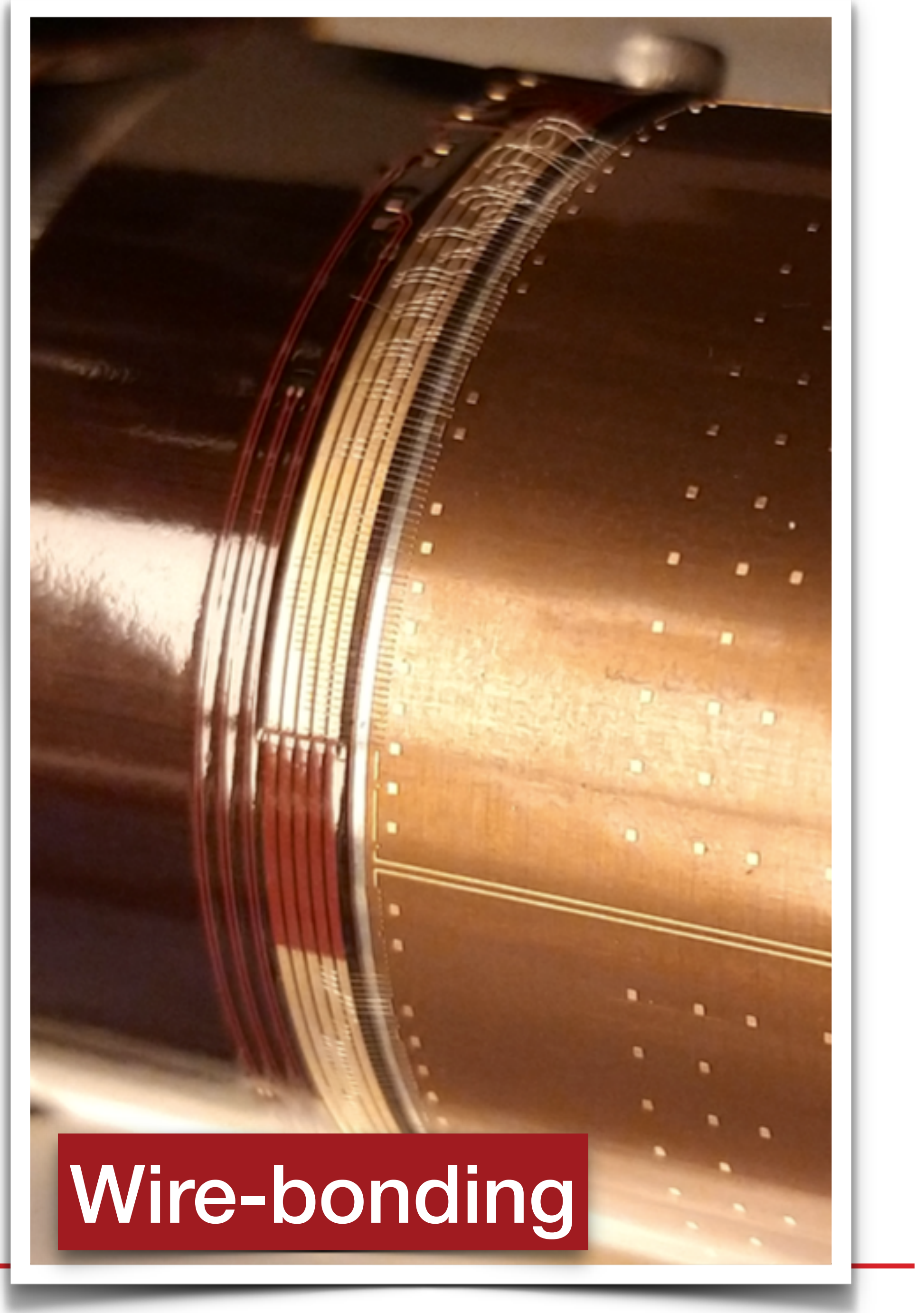
Engineering Model 2

- Improved support
- Less glue seepage into carbon foam

Air cooling

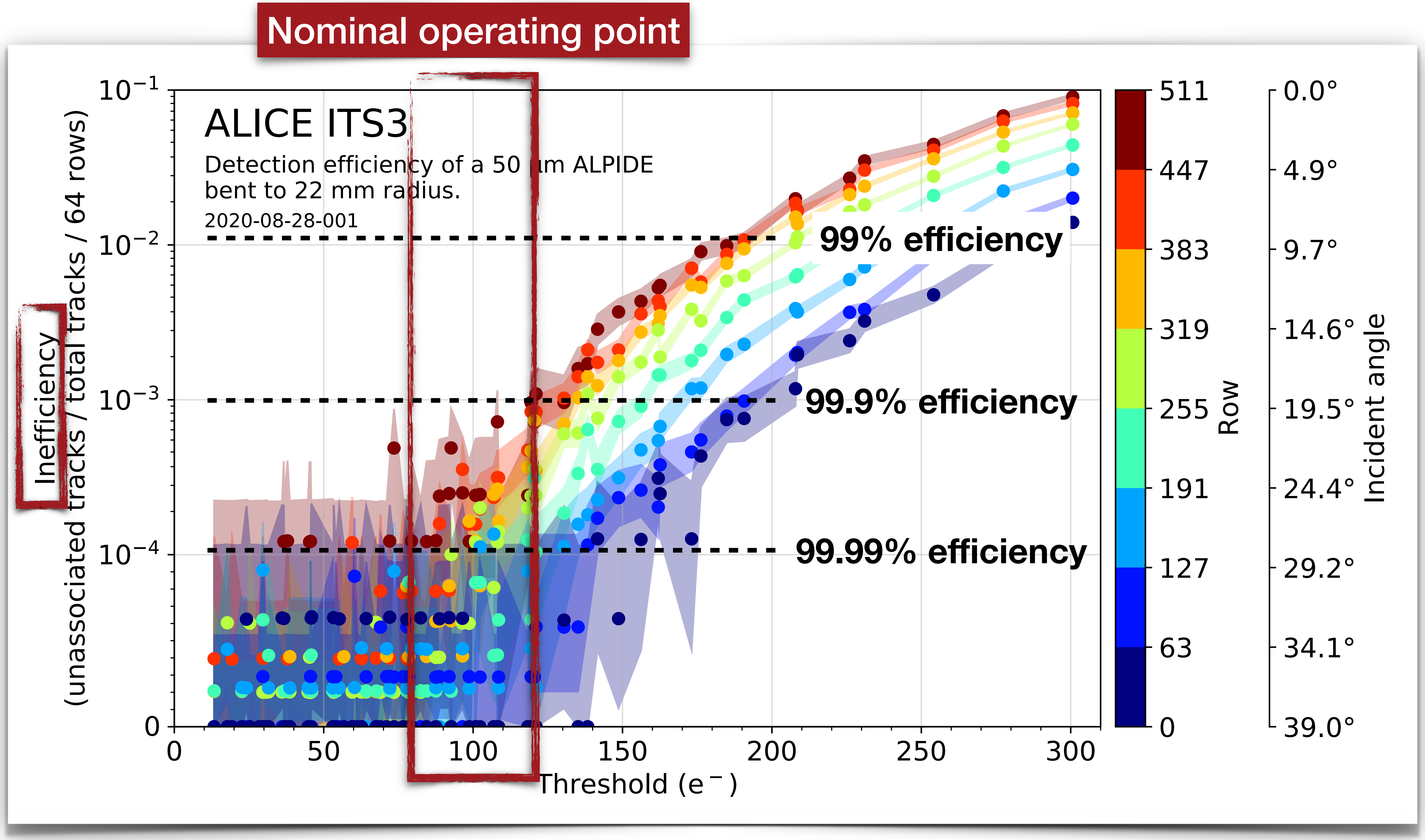
- 3 layers of silicon chips, embedded in Kapton PCB with heating traces
- Exemplary power consumption:
  - matrix: 25 mW/cm²
  - end-cap: 1000 mW/cm²

Integration and services



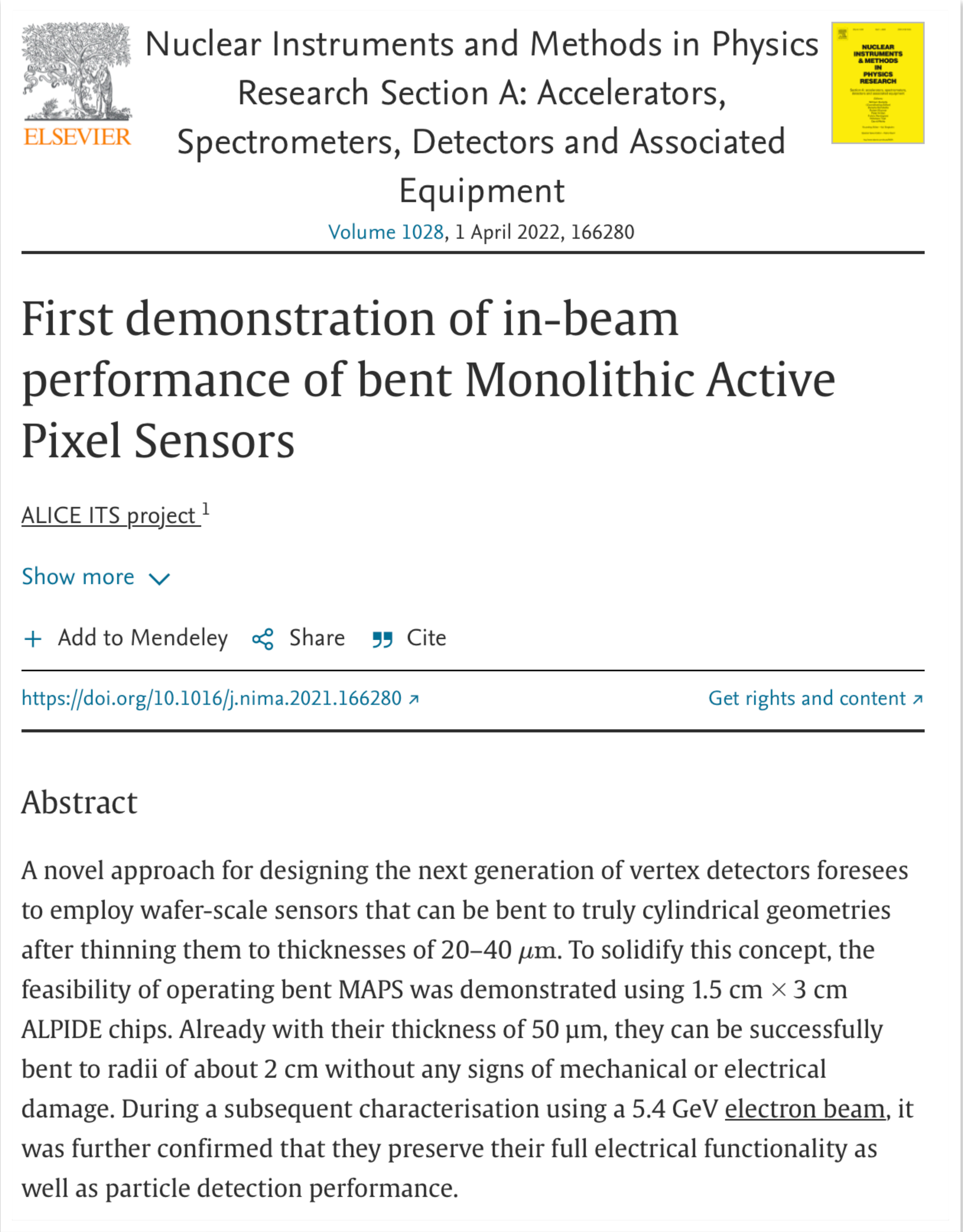
- Data transmission up to 10 Gb/s
- Detector service board close to the detector
  - Electrical to optical conversion
  - Power regulation

Bent MAPS in beam tests



Nominal operating point

Clearly proving that bent MAPS are working!


ELSEVIER

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

Volume 1028, 1 April 2022, 166280

First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS project [1]

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https://doi.org/10.1016/j.nima.2021.166280 ↗

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Abstract

A novel approach for designing the next generation of vertex detectors foresees to employ wafer-scale sensors that can be bent to truly cylindrical geometries after thinning them to thicknesses of 20–40 μm. To solidify this concept, the feasibility of operating bent MAPS was demonstrated using 1.5 cm × 3 cm ALPIDE chips. Already with their thickness of 50 µm, they can be successfully bent to radii of about 2 cm without any signs of mechanical or electrical damage. During a subsequent characterisation using a 5.4 GeV electron beam, it was further confirmed that they preserve their full electrical functionality as well as particle detection performance.

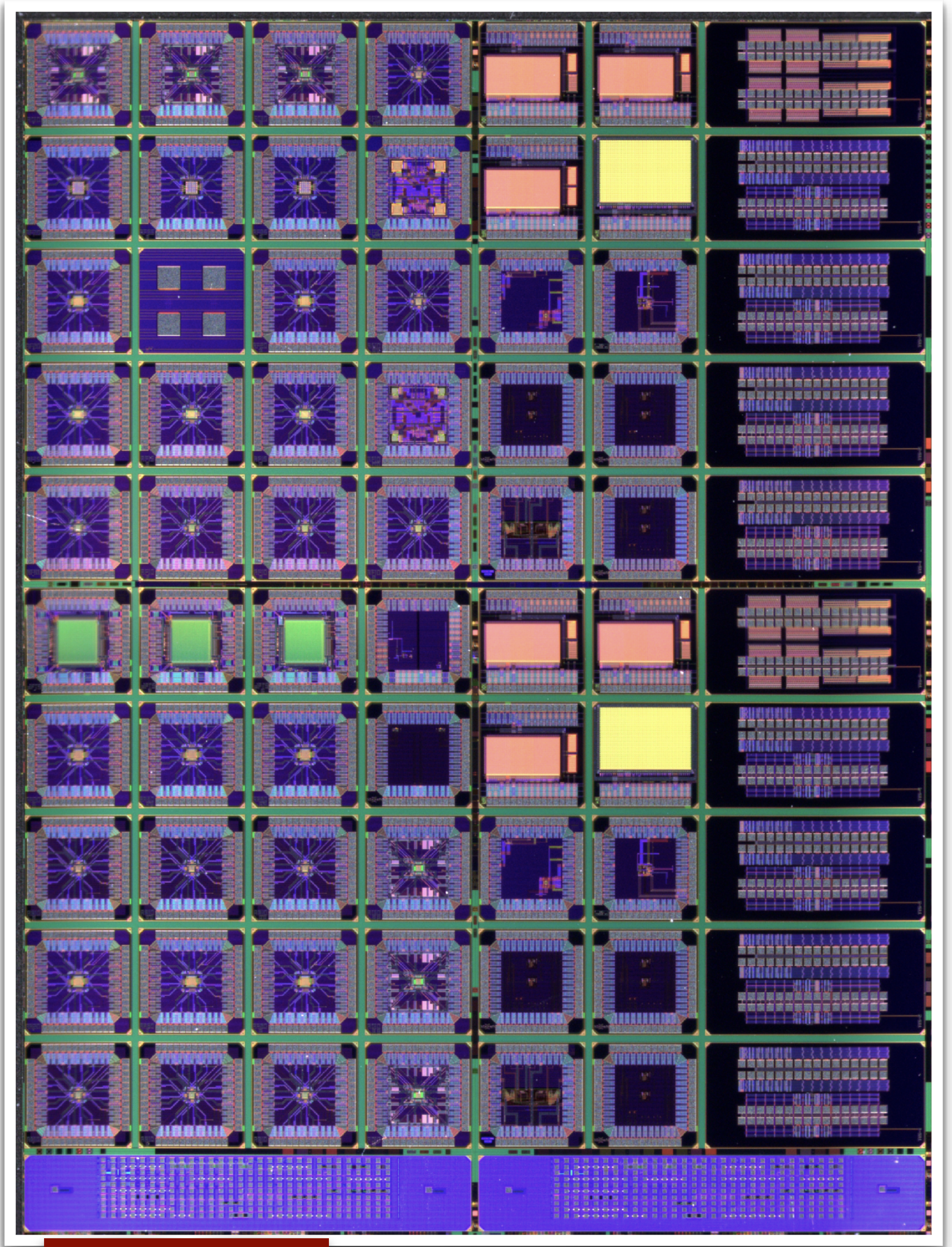
doi.org/10.1016/j.nima.2021.166280

Bent fully processed 65 nm wafer

Technology qualification

- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- TPSCo 65 nm CMOS Imaging Sensor process
- **Key benefits** (over 180 nm technology in ITS2):
  - Smaller features/transistors: higher integration density
  - Smaller pitches
  - Lower power consumption
  - **Larger wafers** (200 → 300 mm)
- **MLR1**
  - Comprehensive *first* submission: **55** prototype chips
  - Goal: qualify the technology (achieved)
- **ER1**
  - Goal: first test of stitching
  - First sensors tested beginning of June!

See: doi.org/10.48550/arXiv.2212.08621



MLR1 reticle

MLR1 testing condensed summary

Requirement

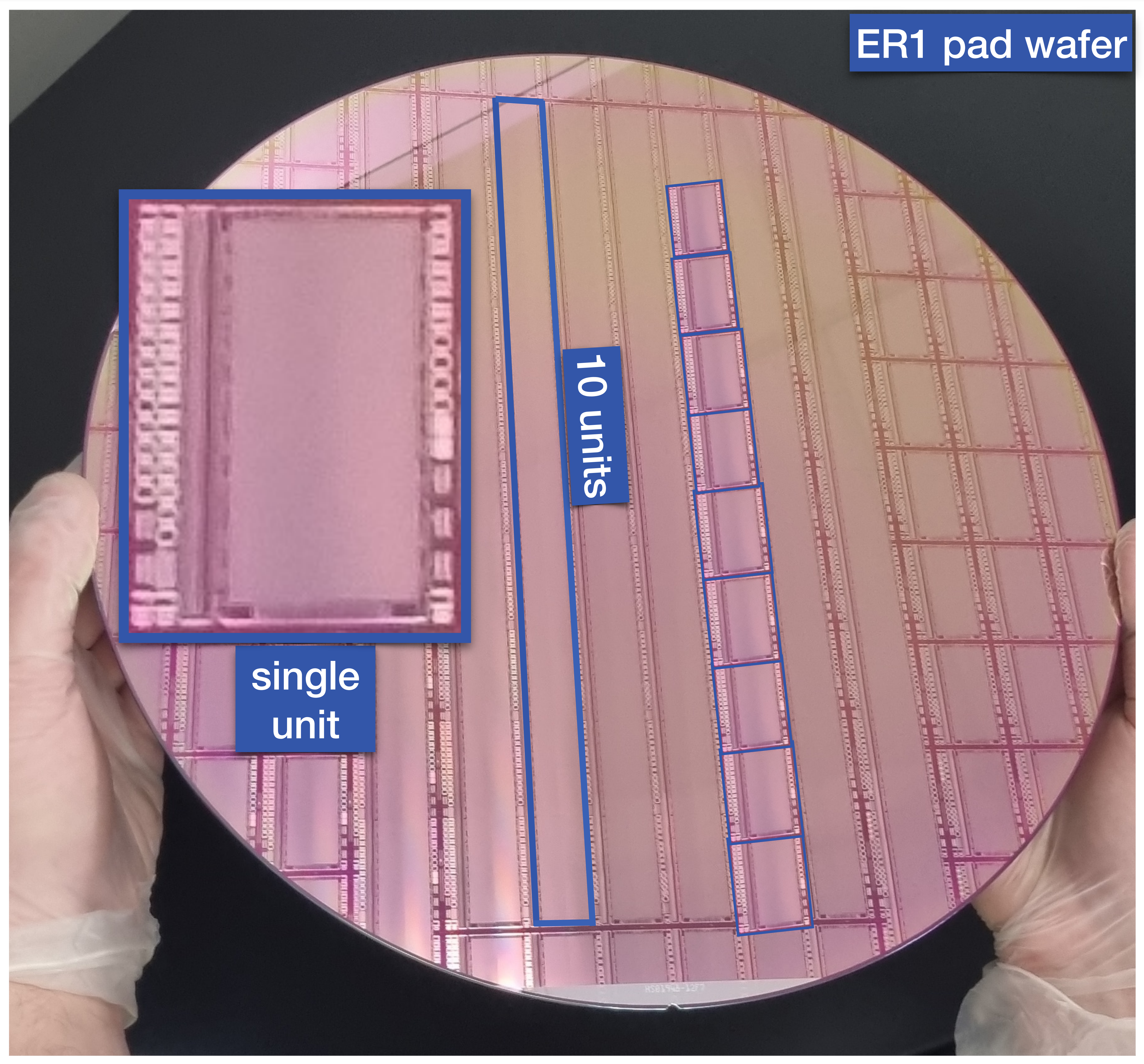
Maximum FHR

@ 20°C

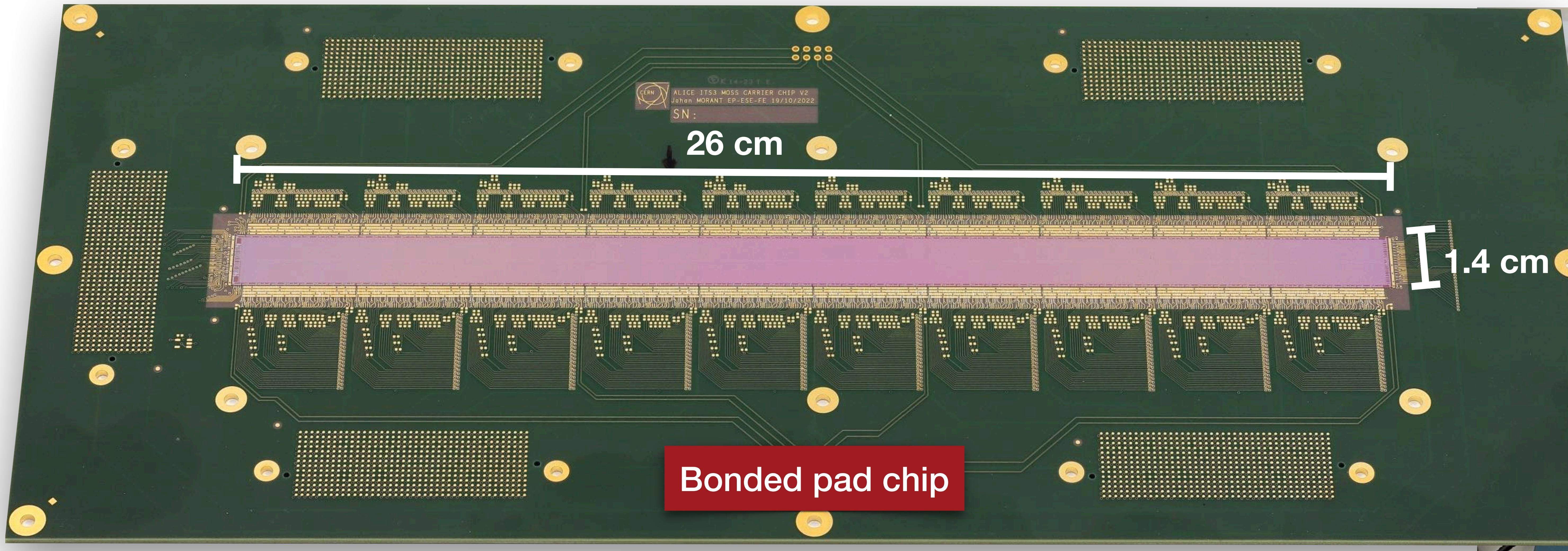
3×ITS3

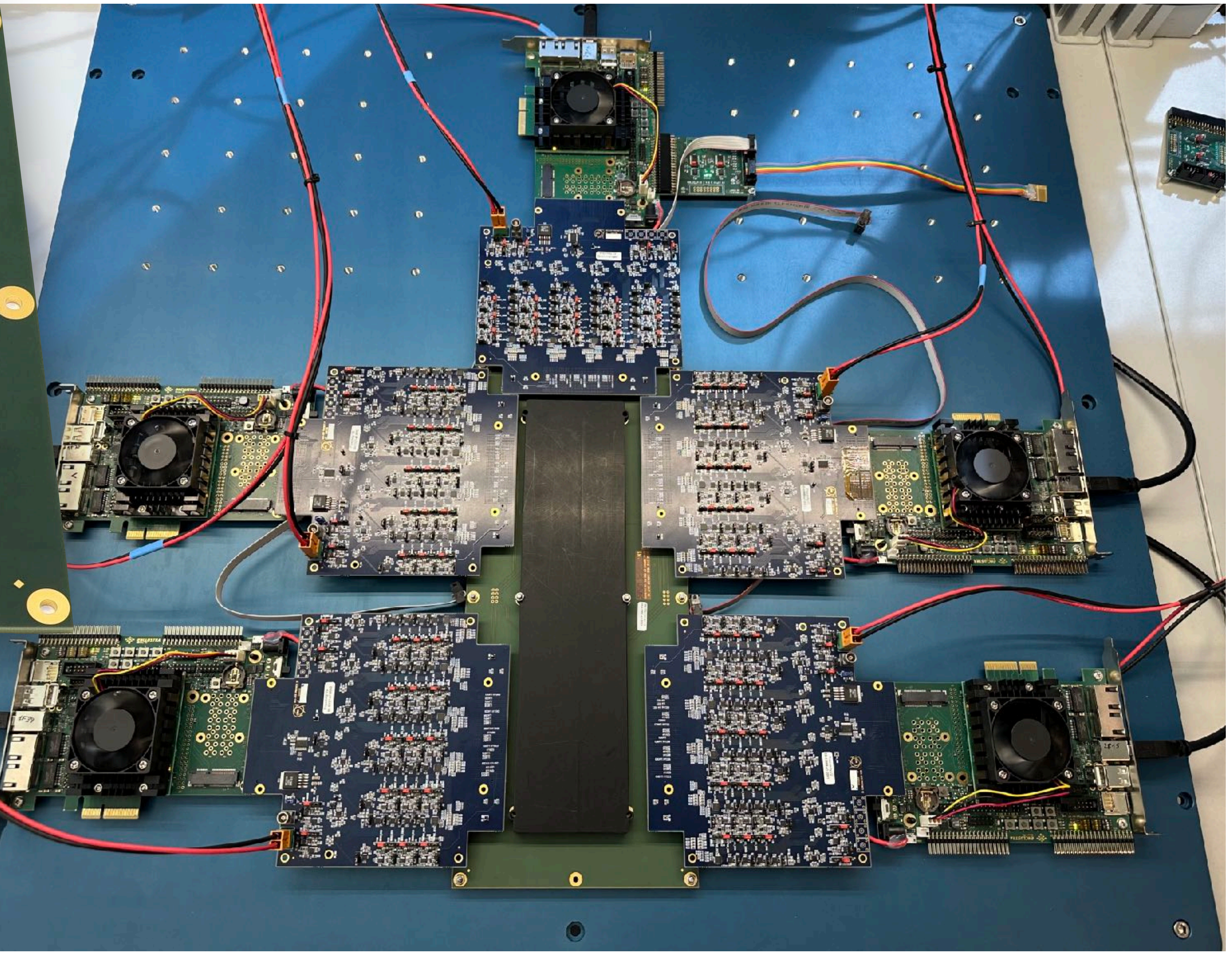
ER1: wafer-scale sensors

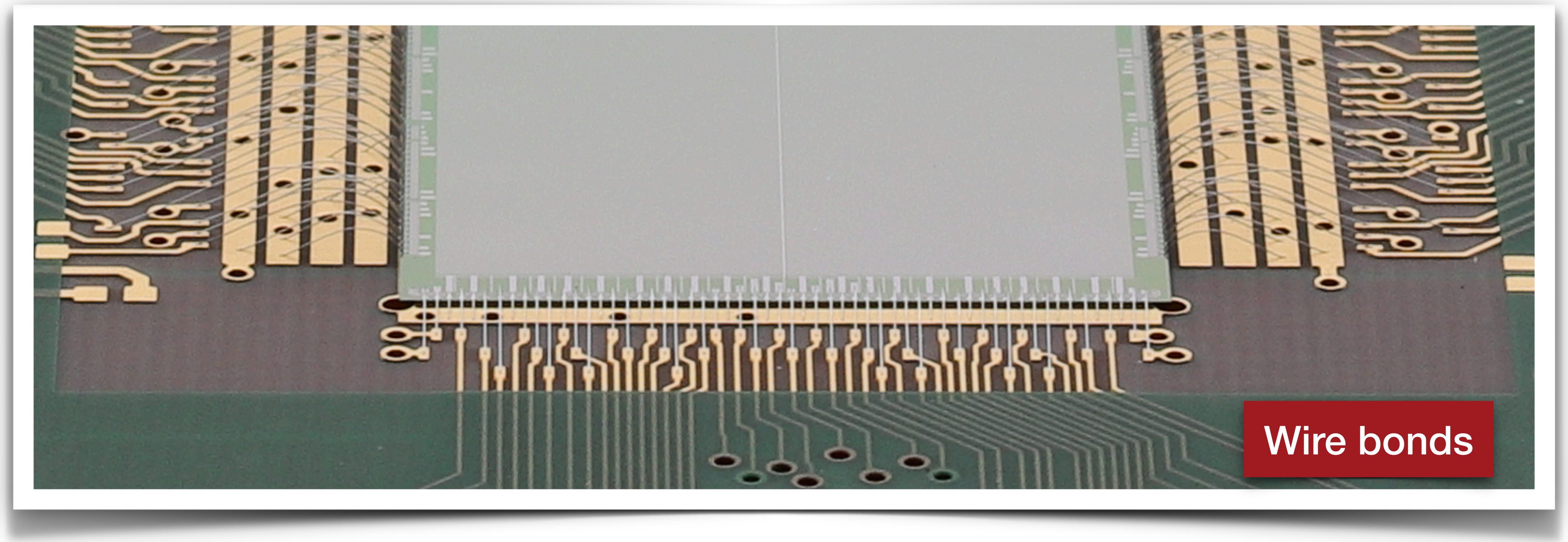
- First MAPS for HEP using stitching
  - one order of magnitude larger than previous chips
- “**MOSS**”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm^2)
  - conservative design, different pitches
- “MOST”: 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm^2)
  - more dense design
- Plenty of small chips (like MLR1)



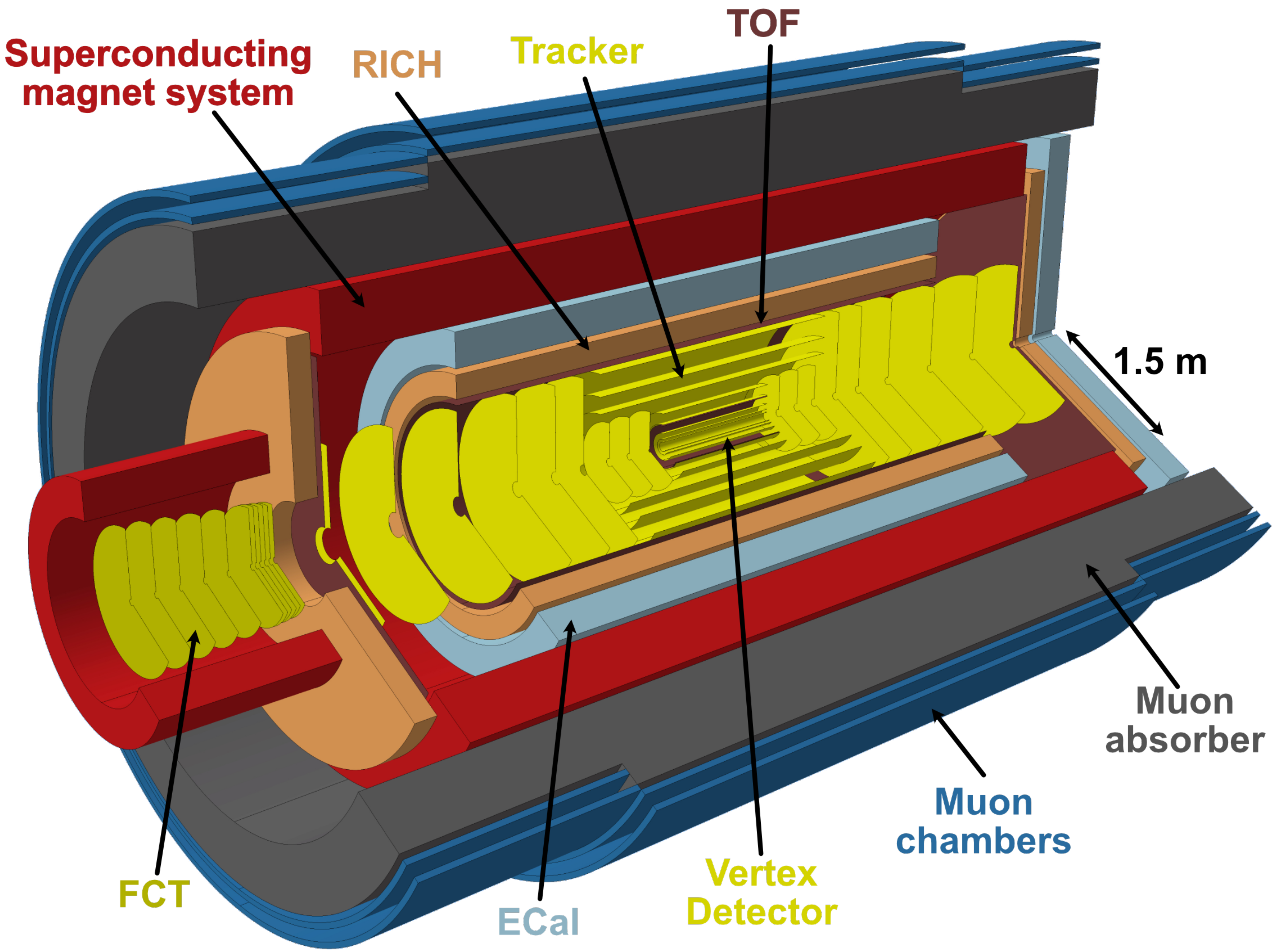
Bonded sensor tests





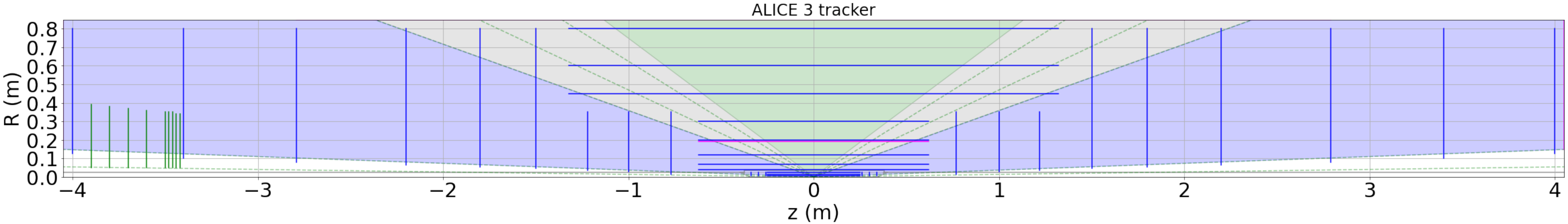


- First MOSS chips bonded
- Functional tests started and promising



ALICE 3 Vertex Detector and Trackers

ALICE 3 — Vertex Detector and Tracker



- **11 barrels, 12 discs**
  - inner-most part within beam pipe
- large active area: **~60 m²**
  - order of magnitude more than ITS2,
  - the currently largest MAPS application
- low material budget: **0.1% X_0** / inner layer
  - less than ITS2, while being larger
- high intrinsic resolution: **2.5 μm**

	Layer	Material thickness (%X_0)	Intrinsic resolution (μm)	Barrel layers Length (±z) (cm)	Barrel layers Radius (r) (cm)	Forward discs Position ($\|z\|$) (cm)	Forward discs R_{in} (cm)	Forward discs R_{out} (cm)
Vertex Detector	0	0.1	2.5	50	0.50	26	0.005	3
	1	0.1	2.5	50	1.20	30	0.005	3
	2	0.1	2.5	50	2.50	34	0.005	3
Outer Tracker	3	1	10	124	3.75	77	0.05	35
	4	1	10	124	7	100	0.05	35
	5	1	10	124	12	122	0.05	35
	6	1	10	124	20	150	0.05	80
	7	1	10	124	30	180	0.05	80
	8	1	10	264	45	220	0.05	80
	9	1	10	264	60	279	0.05	80
	10	1	10	264	80	340	0.05	80
	11	1				400	0.05	80

ALICE 3 — Silicon Tracker — Specifications

Vertex Detector (VD)

- **Pointing resolution** $\propto r_0 \cdot \sqrt{x/X_0}$
  (multiple scattering regime)
  - Radius and material of first layer crucial
  - Minimal radius given by required aperture:
    R ≈ 5 mm at top energy,
    R ≈ 15 mm at injection energy
    → **retractable vertex detector**

Tracking Detectors (Middle Layers + Outer Tracker)

- **Relative pT resolution** $\propto \frac{\sqrt{x/X_0}}{B \cdot L}$
  (limited by multiple scattering)
  - Integrated magnetic field crucial
  - Overall material budget critical

Component	Observables	|η| < 1.75 (barrel)	1.75 < |η| < 4 (forward)	Detectors
Vertexing	Multi-charm baryons, dielectrons	**Best possible DCA resolution,** **$\sigma_{DCA} \approx$ 10 µm at 200 MeV/*c***	**Best possible DCA resolution,** **$\sigma_{DCA} \approx$ 30 µm at 200 MeV/*c***	Retractable silicon pixel tracker: $\sigma_{pos} \approx$ 2.5 µm, $R_{in} \approx$ 5 mm, $X/X_0 \approx$ 0.1 % for first layer
Tracking	Multi-charm baryons, dielectrons	**σ_{p_T} / p_T ~1-2 %**		Silicon pixel tracker: $\sigma_{pos} \approx$ 10 µm, $R_{out} \approx$ 80 cm, $X/X_0 \approx$ 1 % / layer

ALICE 3 Vertex Detector and Tracker — in numbers

	Vertex Detector	Middle Layers	Outer Tracker	ITS3	ITS2
Pixel size (µm^2)	÷ 9 *O*(10 x 10)	• 2.8 *O*(50 x 50)	• 2.8 *O*(50 x 50)	*O*(20 x 20)	*O*(30 x 30)
Position resolution (µm)	÷ 2 2.5	• 2 10	• 2 10	5	5
Time resolution (ns RMS)	÷ 10 100	÷ 10 100	÷ 10 100	100* / O(1000)	O(1000)
Shaping time (ns RMS)	÷ 25 200	÷ 25 200	÷ 25 200	200* / O(5000)	O(5000)
Fake-hit rate (/ pixel / event)	≈ $< 10^{-8}$	≈ $< 10^{-8}$	≈ $< 10^{-8}$	$<10^{-7}$	$<< 10^{-6}$
Power consumption (mW / cm^2)	+ 75% 70	20	20	20**	47 / 35***
Particle hit density (MHz / cm^2)	• 20 94	1.7	67% 0.06	8.5	5
Non-Ionising Energy Loss (1 MeV n$_{eq}$ / cm^2)	• 3000 1 x 10^{16}	• 100 2 x 10^{14}	≈ 5.6 x 10^{12}	3 x 10^{12}	3 x 10^{12}
Total Ionising Dose (Mrad)	• 1000 300	• 10 5	≈ 0.2	0.3	0.3
Surface (m^2)	• 2.5 0.15	÷ 2 5	• 6 57	0.06	10
Material budget (% X_0)	0.1	1	1	0.05	0.36 / 1.1 ***

* goal, not crucial, like not possible due to power budget

** pixel matrix

*** innermost layers / outer layers

• X Change compared to ITS2

Improving performance concerning all aspects

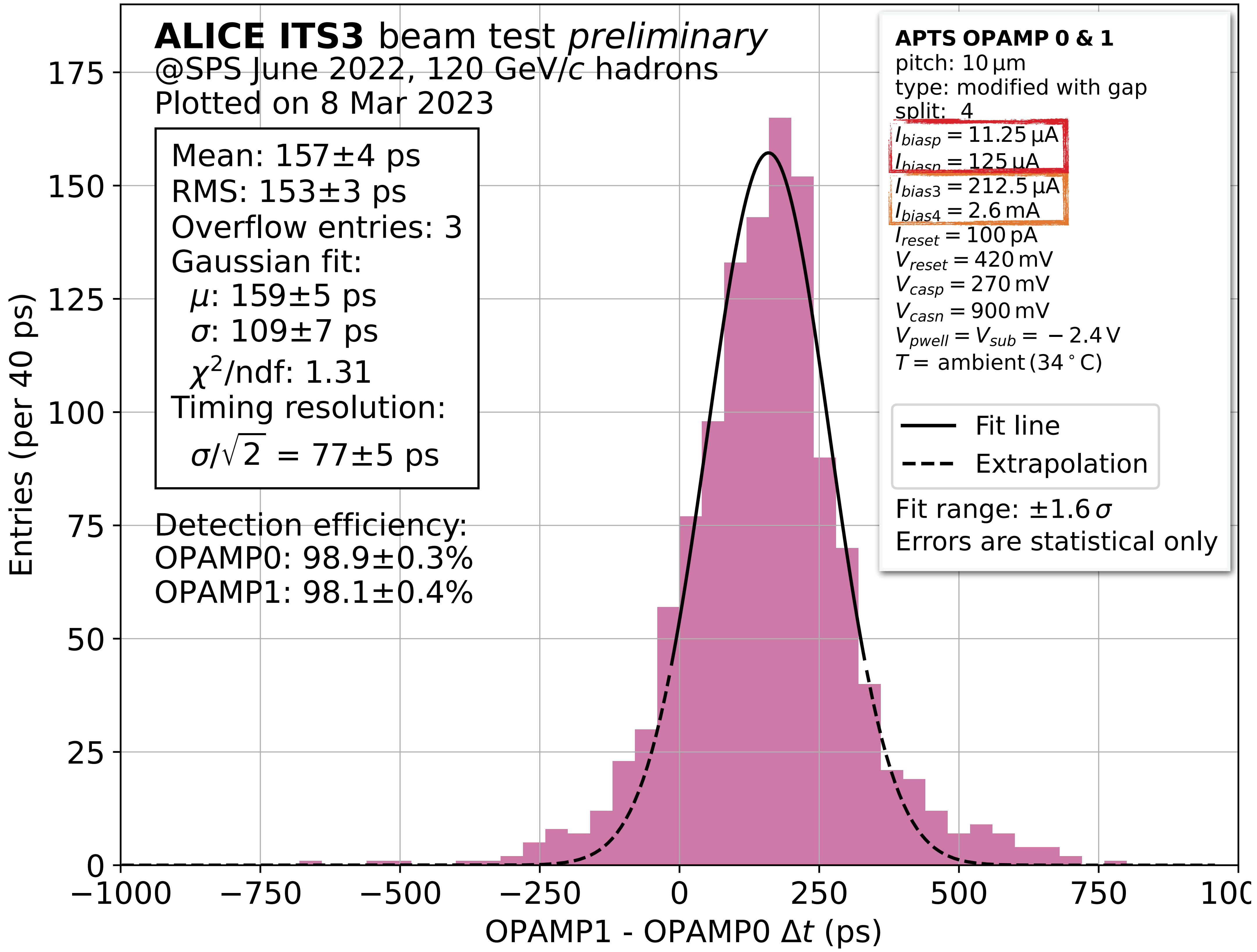
Different optimisations needed for the different ALICE 3 Vertex Detector and tracking layers

ITS3 — Radiation hardness - detection efficiency & FHR

Performance at sub-zero temperatures?

ITS3 — Timing resolution

Sensor only

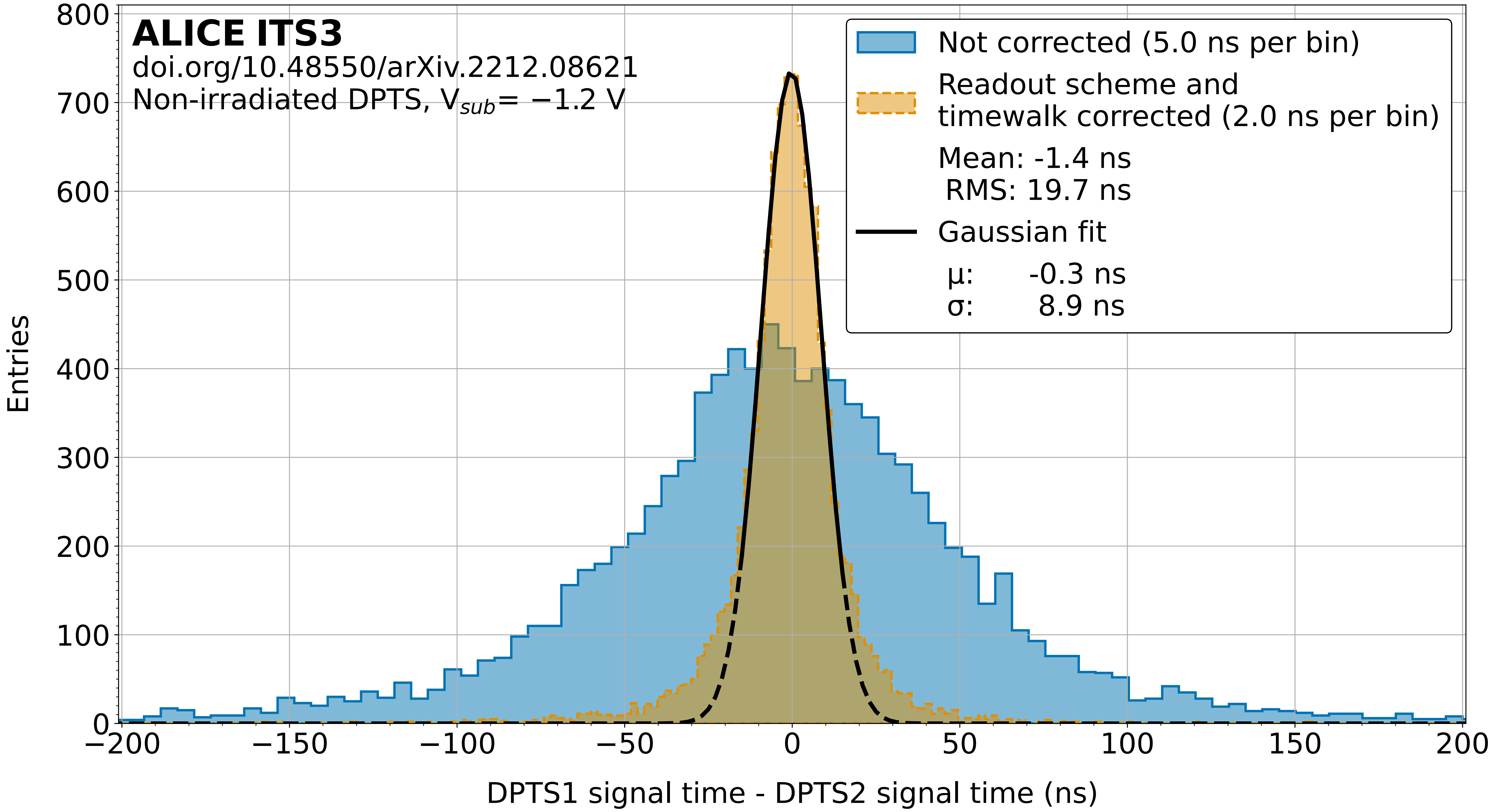


~80 ps timing resolution

~3 μW in-pixel

~3 mW in-chip

With front-end



~6 ns timing resolution

(~30 ns not corrected)

~120 nW in-pixel

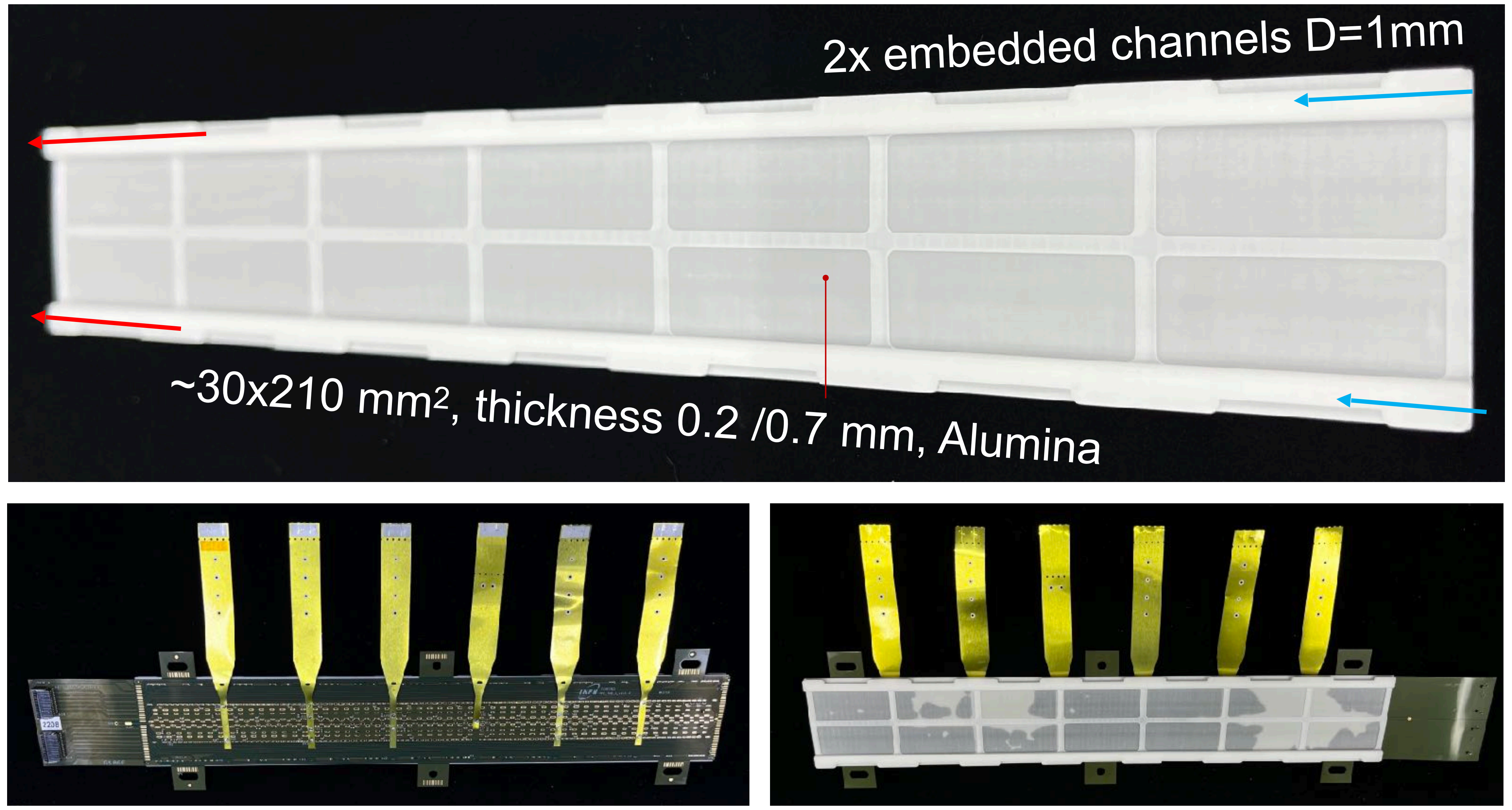
Vertex Detector (IRIS) Mechanics

Petal inside design

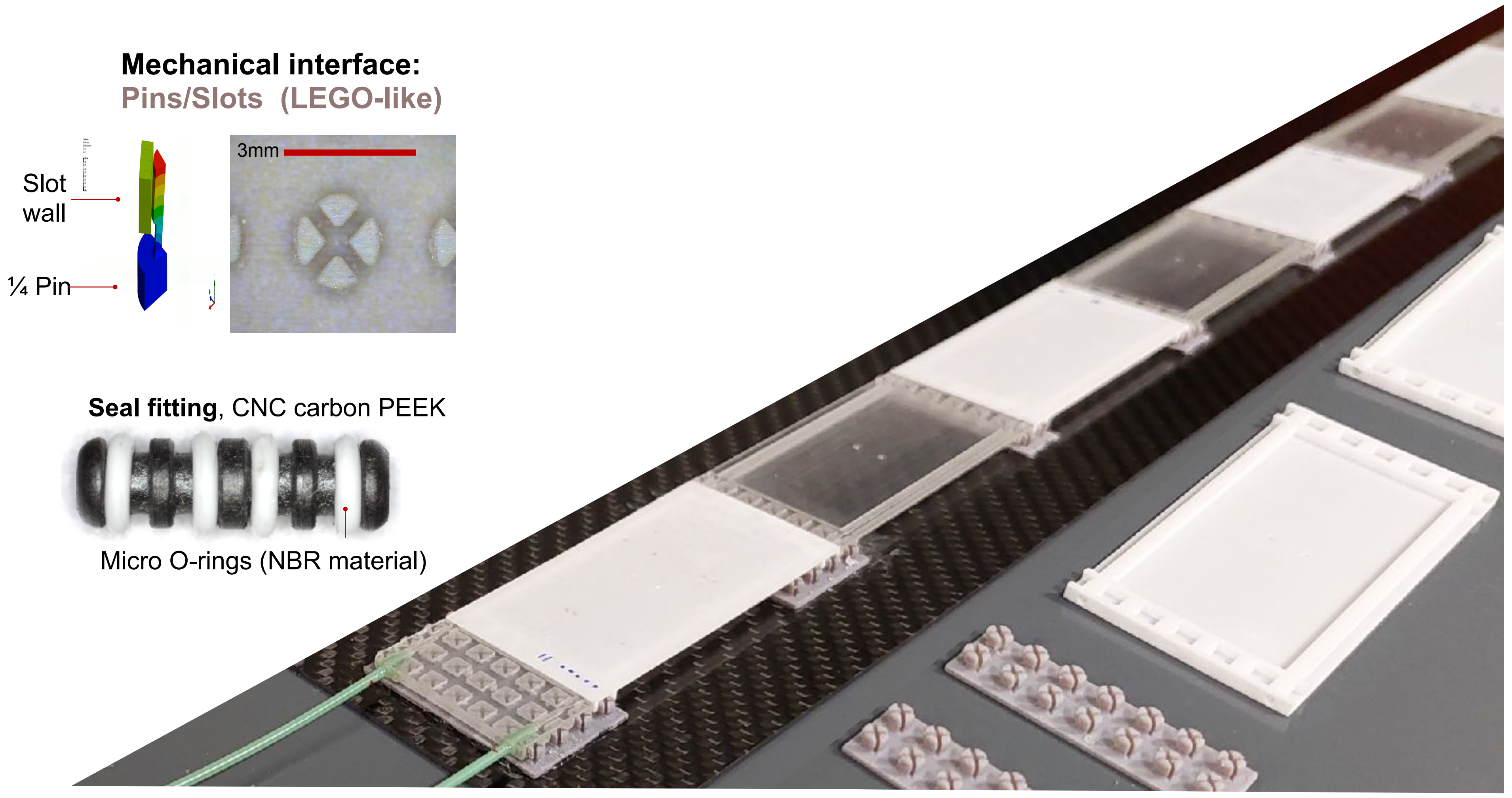
- Active cooling to -25ºC inside the petal to remove heat generated by the sensors
- A cold plate is in thermal contact through carbon paper / foam to the sensors

Material adopted from Corrado Gargiulo’s presentation during the ALICE upgrade week

Tracker Module R&D

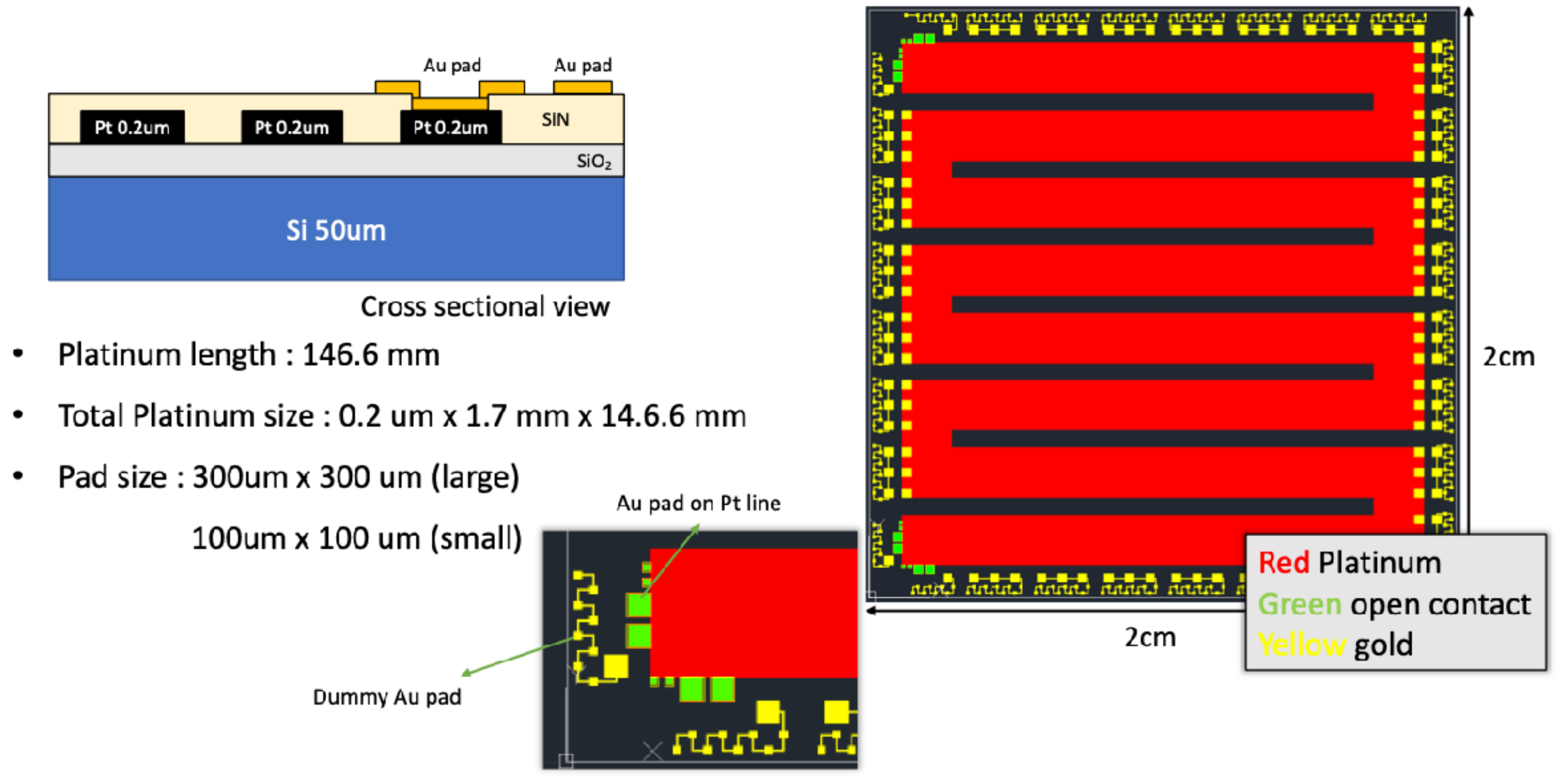


ALICE ITS2 OB module on large-scale 3D printed ceramic cold plate developed in the CERN EP R&D context



LEGO-like modules developed in the CERN EP R&D context

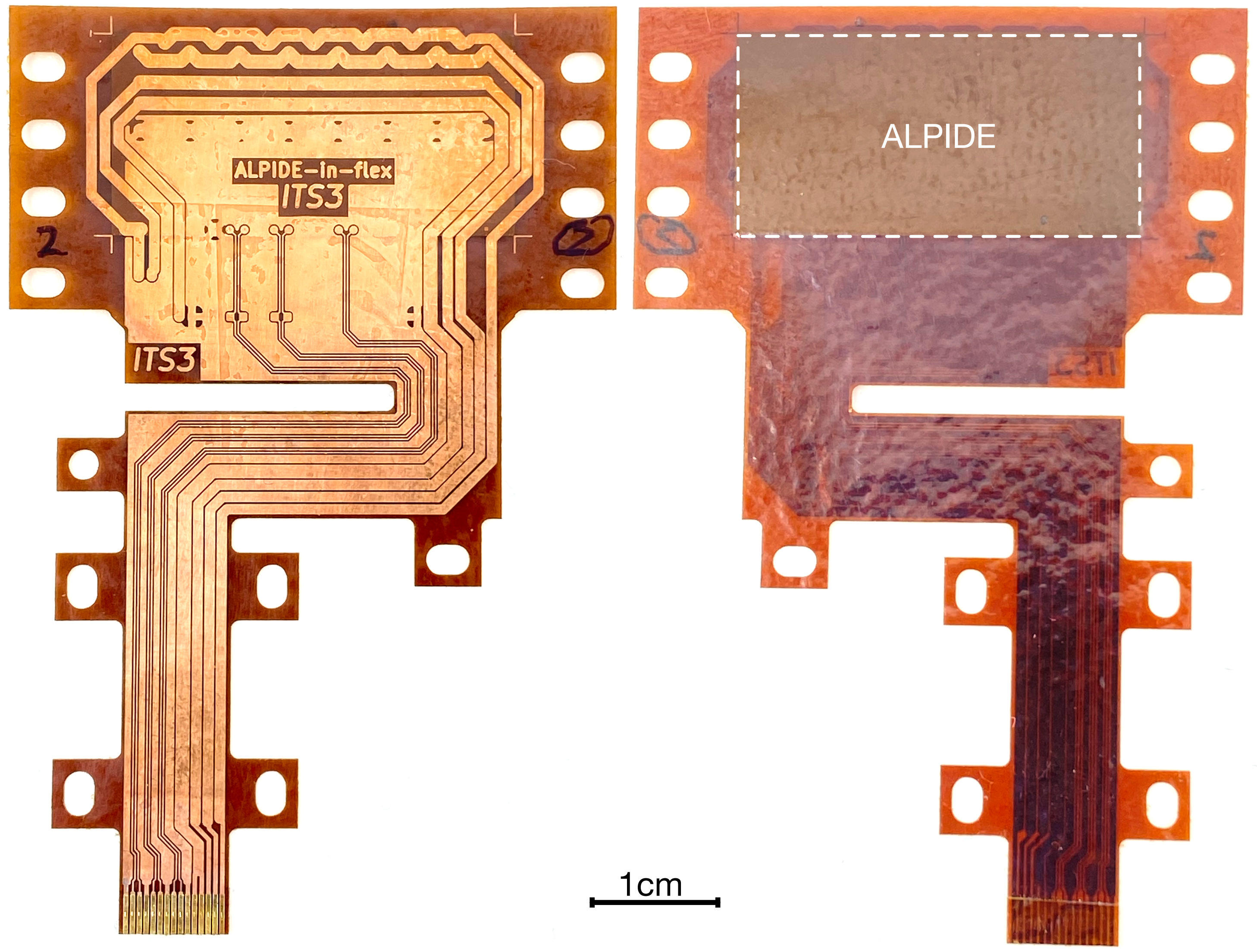
- Targeting easy replacement while maintaining low material budget
  → simplify detector construction
  → important to achieve a high yield
- Using silicon heater chips to optimise module and chip layout



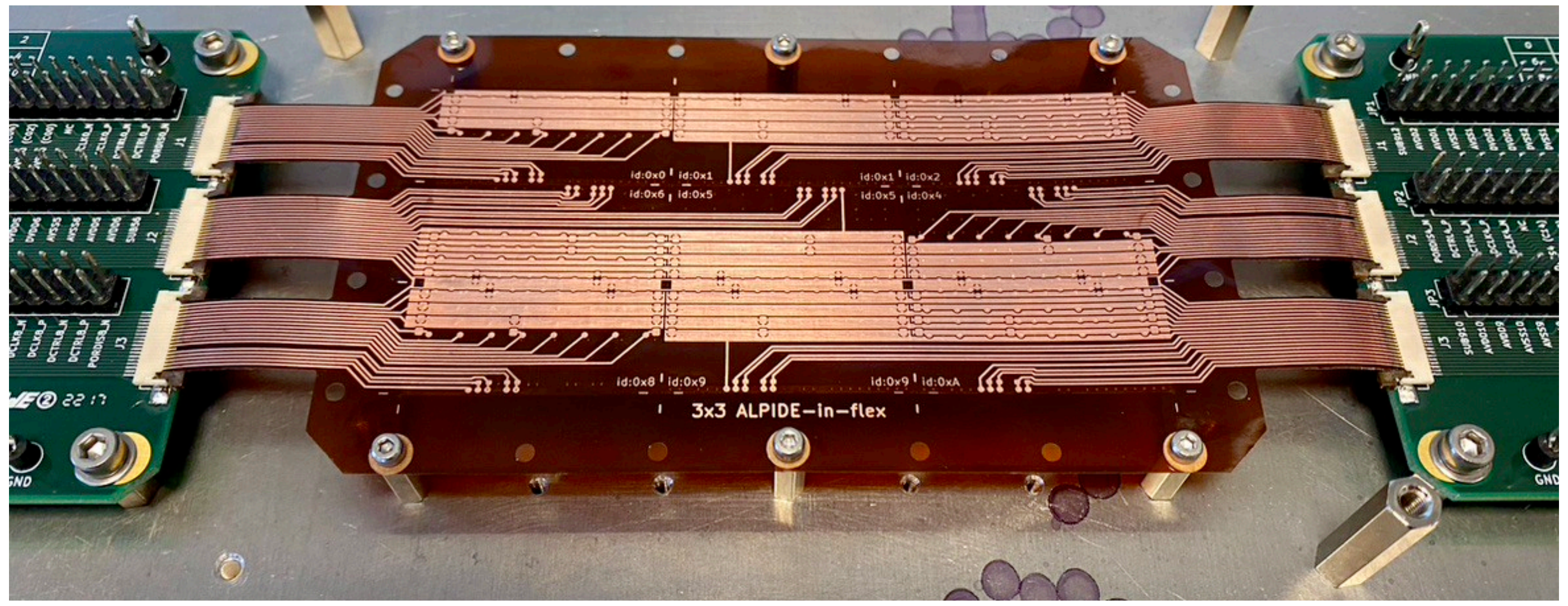
Silicon heater of 2 cm by 2 cm for module integration studies

For information on the CERN EP R&D developments here

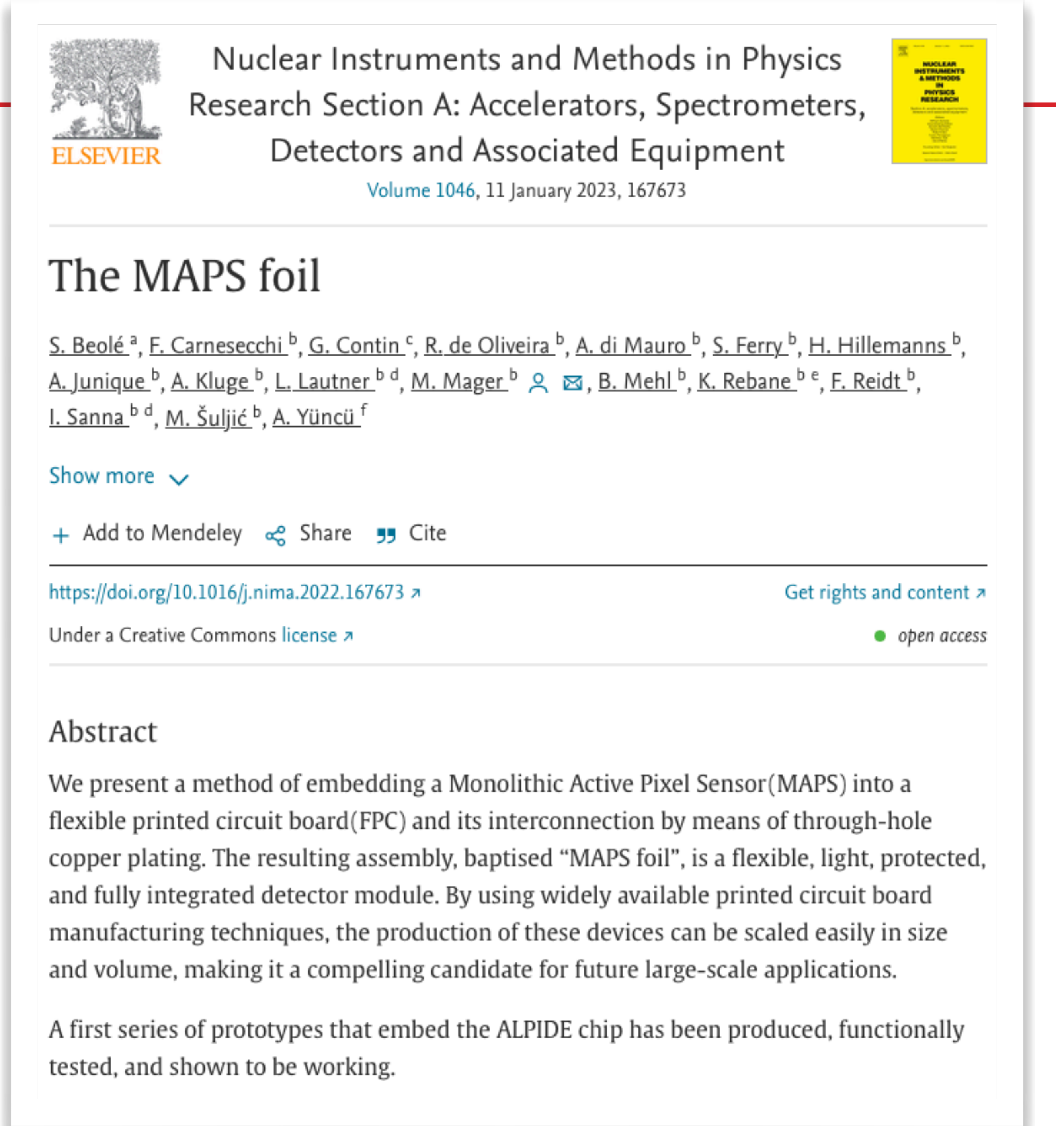
Tracker Module R&D — MAPS foil



Single ALPIDE sensor embedded into Kapton



Next generation: 3 x 3 ALPIDE sensors embedded in to Kapton



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The MAPS foil

S. Beolé [a], F. Carnesecchi [b], G. Contin [c], R. de Oliveira [b], A. di Mauro [b], S. Ferry [b], H. Hillemanns [b], A. Junique [b], A. Kluge [b], L. Lautner [b d], M. Mager [b], B. Mehl [b], K. Rebane [b e], F. Reidt [b], I. Sanna [b d], M. Šuljić [b], A. Yüncü [f]

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Abstract

We present a method of embedding a Monolithic Active Pixel Sensor(MAPS) into a flexible printed circuit board(FPC) and its interconnection by means of through-hole copper plating. The resulting assembly, baptised "MAPS foil", is a flexible, light, protected, and fully integrated detector module. By using widely available printed circuit board manufacturing techniques, the production of these devices can be scaled easily in size and volume, making it a compelling candidate for future large-scale applications.

A first series of prototypes that embed the ALPIDE chip has been produced, functionally tested, and shown to be working.

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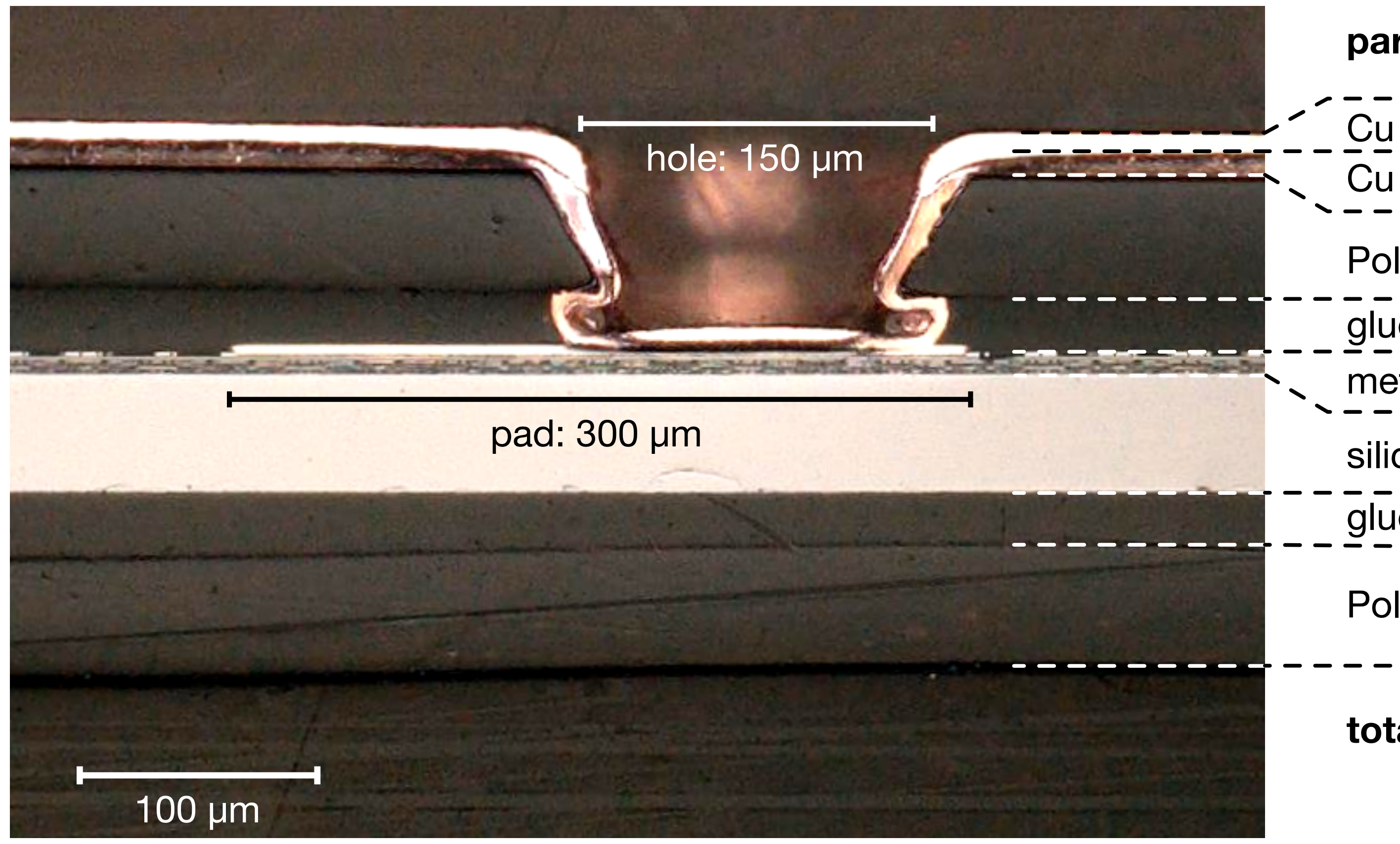

part	thickness	radiation length
Cu plating	13 µm	(0.09%)
Cu cladding	5 µm	(0.03%)
Polyimide	45 µm	0.02%
glue	25 µm	0.01%
metal stack	10 µm	0.01%
silicon	45 µm	0.05%
glue	25 µm	0.01%
Polyimide	45 µm	0.02%
total:	**213 µm**	**0.10%** (+ 0.13% Cu)

Cross section of the MAPS foil

- Novel module concept leading to flexible modules
- Kapton serves as mechanical support and protection
- Potential alternative for wafer-scale chips
- Production process similar to the one of Printed-Circuit Boards (PCBs)

Summary

- ALICE silicon detectors are at frontier of technology
- ITS2
  - largest and most granular pixel detector in high-energy physics
- ITS3
  - first wafer-scale bent silicon pixel detector
- ALICE3
  - retractable vertex detector
  - targeting unprecedented detector performance
  - largest pixel detector to be built (~60 m²)

Thanks a lot for your attention

ITS Outer Barrel during insertion tests