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OPTIMISATION STRATEGY FOR THE SENSOR BASED ON THE MPW3 MONOLITHIC DETECTOR

Preliminary and Conceptional Ideas

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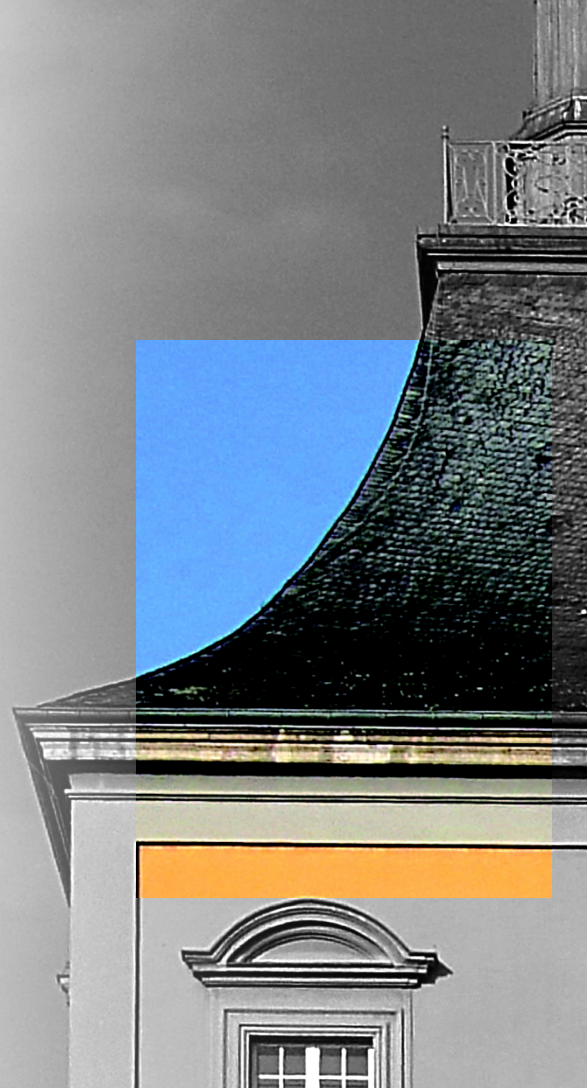
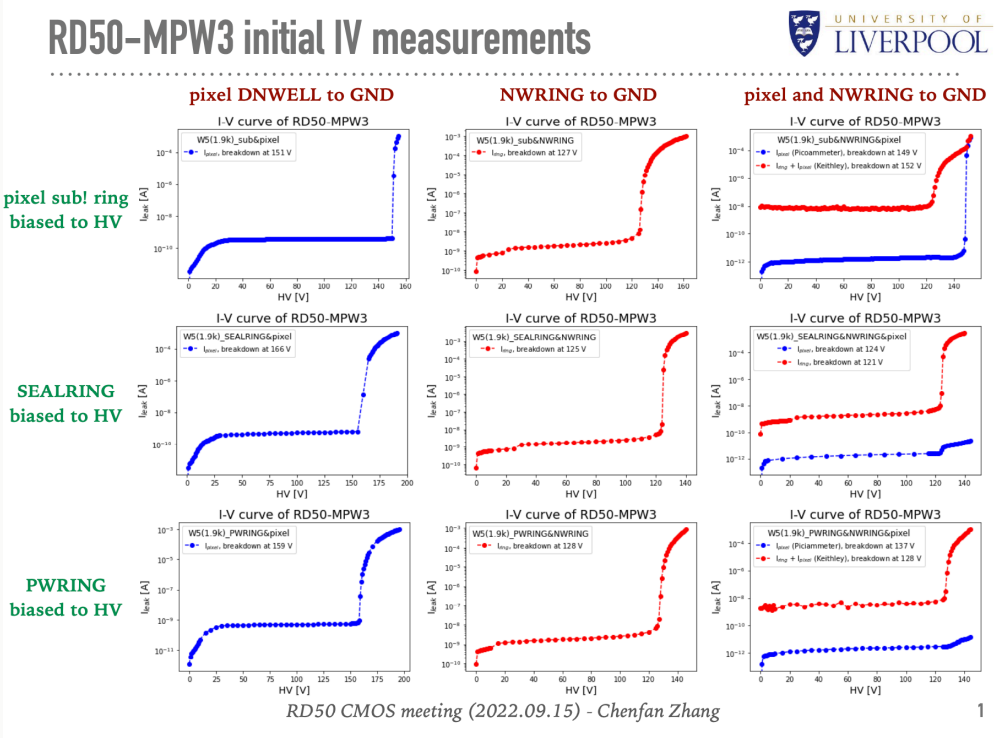
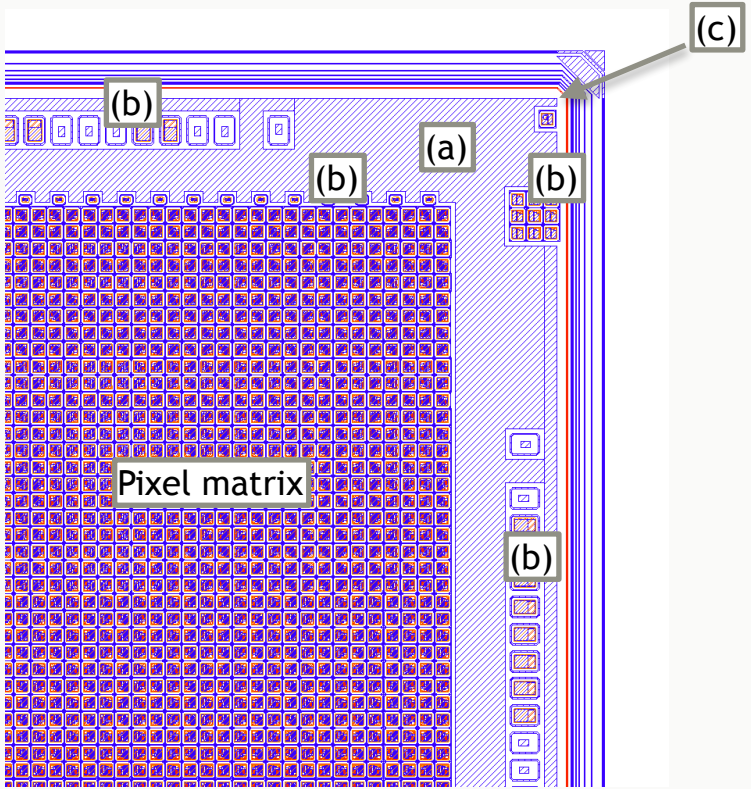


MEASUREMENTS OF THE BREAKDOWN VOLTAGE IN LIVERPOOL



- Measurements of almost all scenarios showing:
  - Large current increase at bias voltage between 120 V and 150V
- Breakdown possibly takes place between the p-stop and pixel (distance of 8um)
- Nevertheless, still hard to locate where the breakdown actually takes place
  - May locate at the implants with similar spacing of 8um

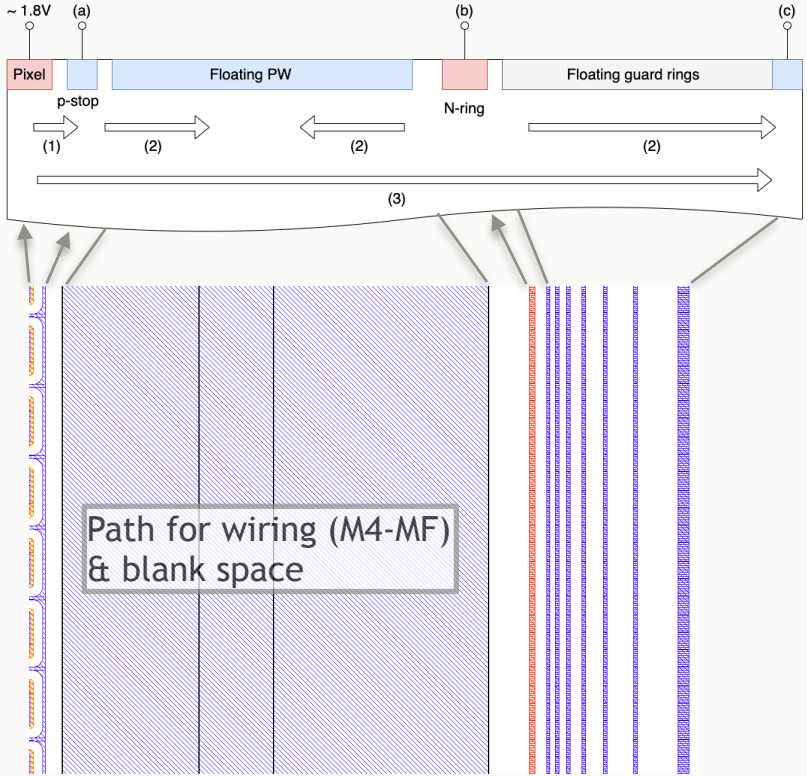
OBSERVATIONS FROM THE LAYOUT



- (a): large floating PW between pixel matrix and GR
  - Directly encloses the pixel matrix
  - Width is not uniform
- (b): isolated structures
  - Physically isolated from the pixel matrix
  - P-stop/ring connected together
  - Locations do not follow a pattern
  - Individual size and structure
- (c): sharp corners
  - Appears at various locations
- Etc. similar cases in the rest part of the chip

- If bias through p-stop -> potential drop more or less predictable
- If bias through edge/back (floating p-stop)
  -> hard to predict the potential distribution among implants

POTENTIAL FROM MATRIX TO THE EDGE



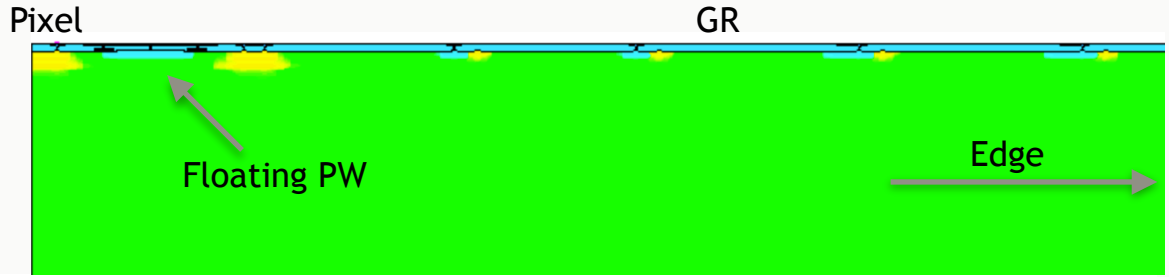
(I) Current biasing method: - HV at (a)
- Potential drop (1), the rest not really relevant

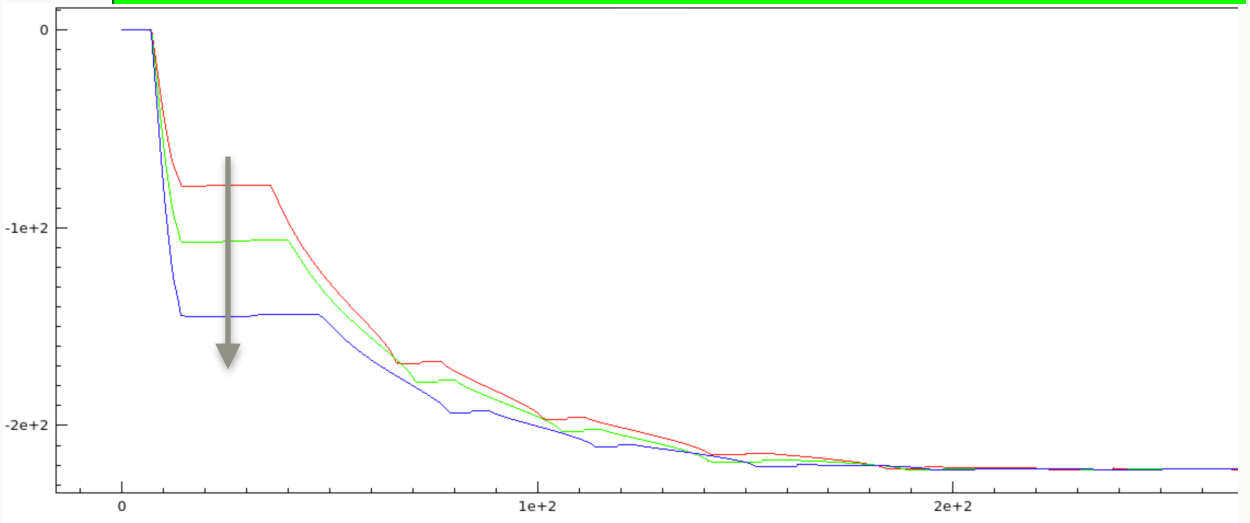
(II) Edge bias (-HV at (c)) with floating p-stop:
- Potential drop (3), across the entire periphery
- Large floating PW suppresses the potential
- Potential drop (1) dominates

(III) Edge bias (-HV at (c)) with floating p-stop and biased N-ring (0V or ~1.8V at (b))
- Potential drop (2), potential drop consists of two parts
- Guard ring region determined by the geometry
- Large floating PW + p-stop can cause large potential drop, although it should be less significant as the previous case

(II) EDGE BIAS (-HV AT (C)) WITH FLOATING P-STOP

- Not exactly the same structure for simulation, but the idea is the same
- Larger floating PW close to the pixel implant leads to lower potential
- Therefore smaller breakdown voltage





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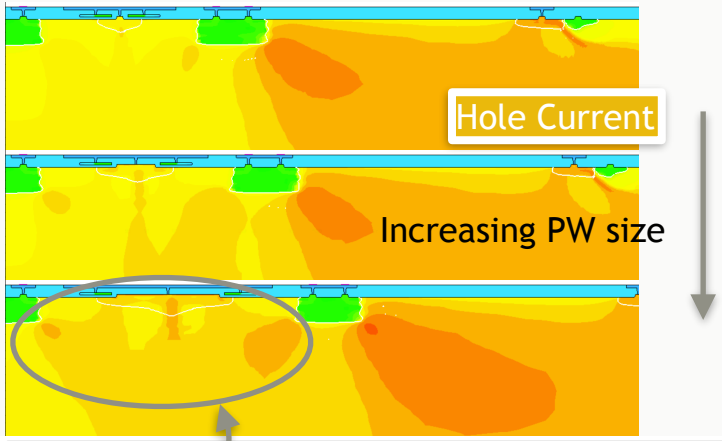
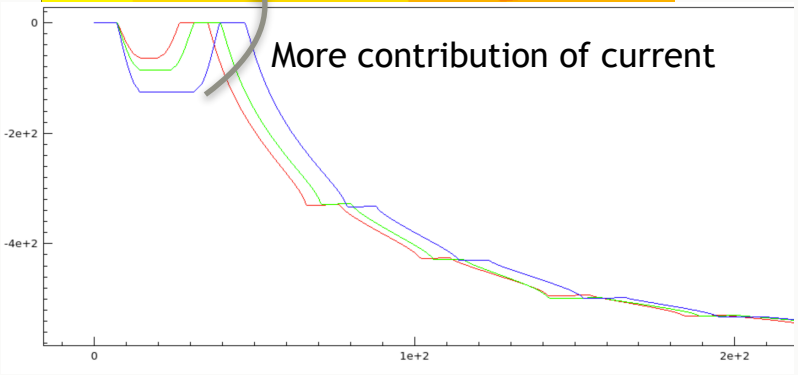
(II) EDGE BIAS (-HV AT (C)) WITH FLOATING P-STOP AND BIASED N-RING (0V OR ~1.8V AT (B))

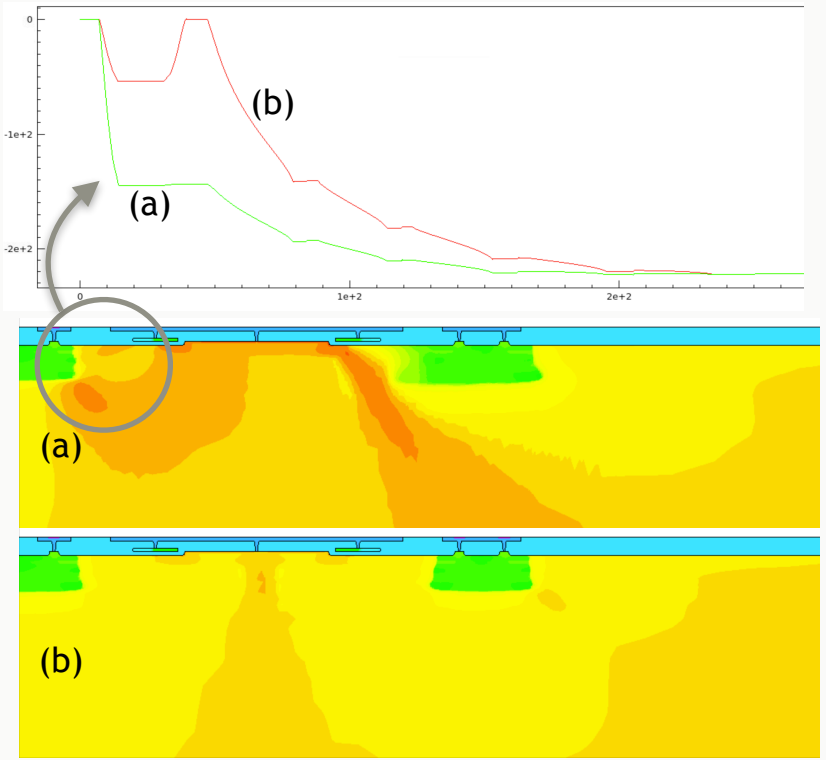




- The biased n-ring (at the same voltage as the pixel) holds the potential of the floating PW at a higher level
- Potential drop at the PW increases with larger width

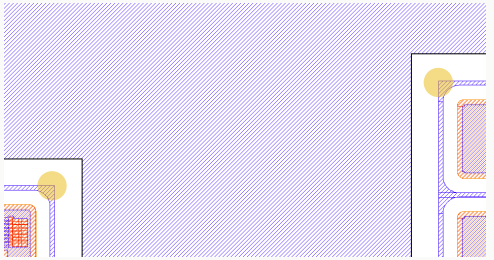
COMPARE BOTH CASES (II) & (III)

- Set the n-ring to a fixed voltage will significantly reduce the voltage drop at the same bias voltage
- Current contribution (from impact ionisation) is reduced



SUMMARY OF THOUGHTS

1. **If we use edge bias, the guard ring structure may not be the only part requires optimisation**
2. The large floating PW can cause a dominating potential drop
3. The structure like an n-ring can be very helpful to regulate the potential distribution

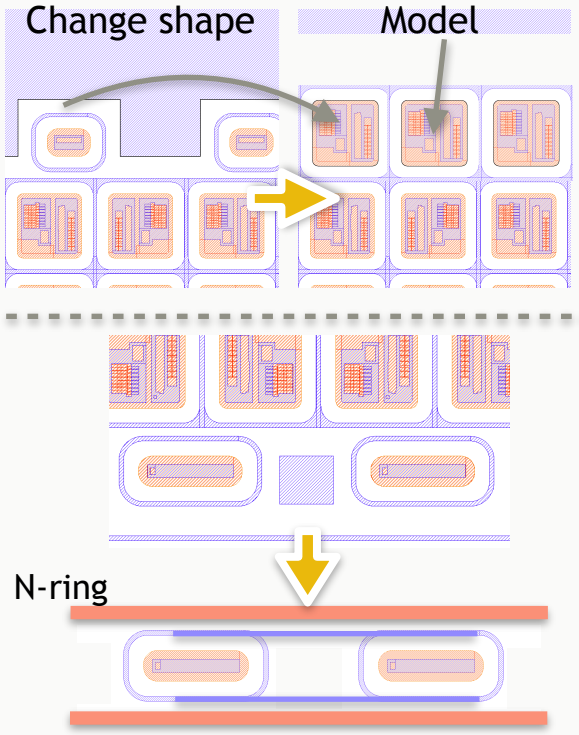


Measures

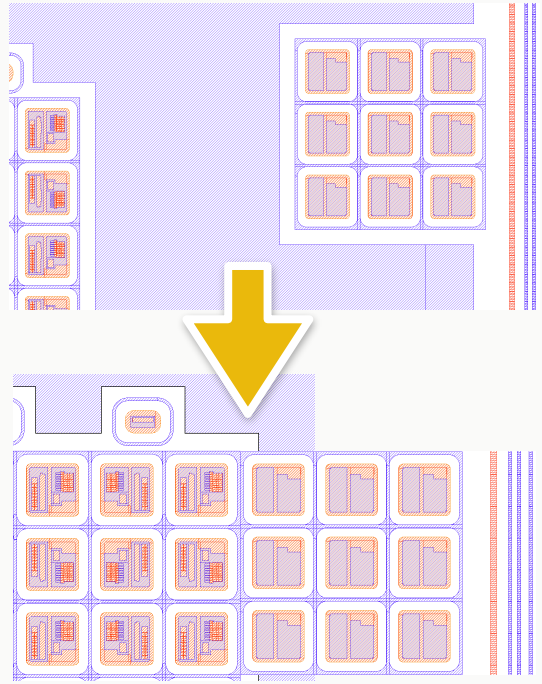
1. Round sharp corners ✅
   - ➡ Less possibility to have high field
2. Re-organise the isolated structures in the periphery
   - ➡ More ordered implant geometry
   - ➡ Easier to predict and debug (if necessary)
3. Reduce the size of the floating PW
   - ➡ Reduce potential drop
4. Implement N-ring/DNW
   - ➡ Regulate potential & field, provide shielding
5. Optimise guard ring

NAIVE EXAMPLES: RE-ORGANISE

- For the structures having a “p-stop” with the same voltage as the matrix, we can merge the p-stop and integrate them into the matrix
- Can change the shape of certain structures besides the matrix and merge into the matrix. Can also use models which acts merely as a passive pixel
- For the structures hard to change, we can eliminate the floating PW and put in n-ring. Would be nice if they can be in a common DNW and be a part of the n-ring



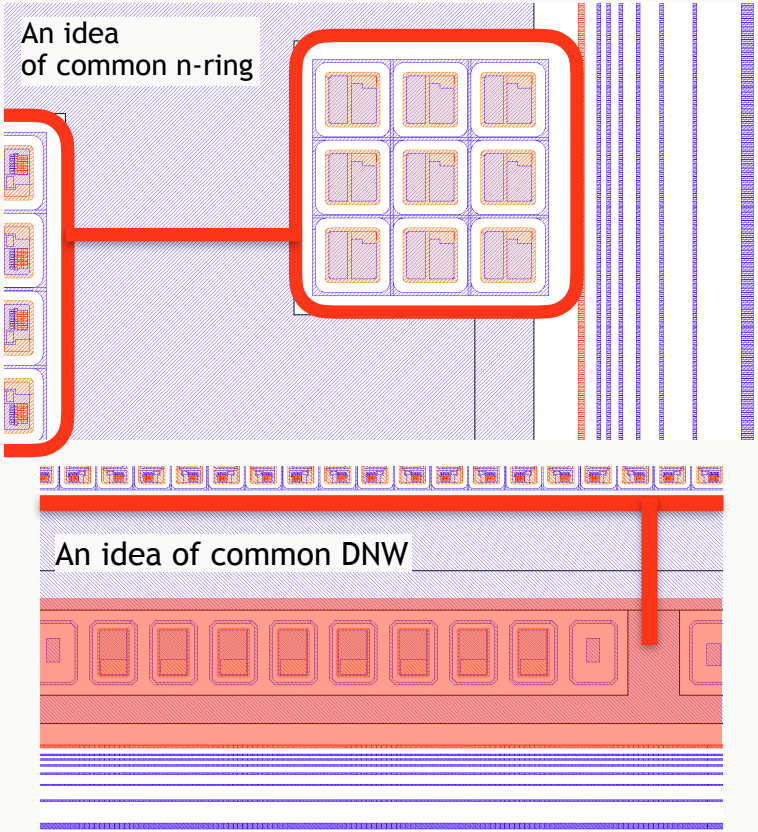
Possible to put these in a common DNW ?



A column of passive structures/models …

IMPLEMENT N-RING/DNW & REDUCE PW

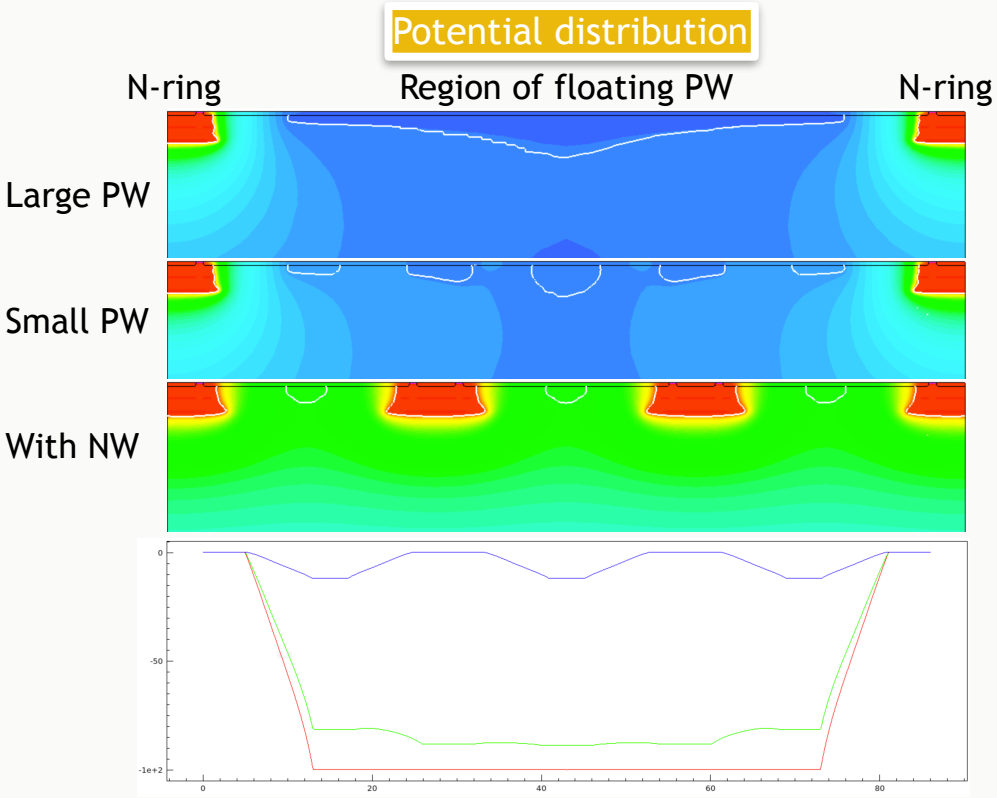
- Both approaches are related
  - Use n-ring (with a fixed potential) to occupy the space of PW (floating potential)
- N-ring:
  - Encloses the pixel matrix -> shape the field of edge pixels & collect the leakage outside the matrix
  - Encloses isolated structures which requires a similar potential at the p-stop/ring (like the test structures)
  - Connect all the n-ring to the n-ring at the guard-ring -> build a common potential
- DNW:
  - If structures can be put into a common DNW (connected to the N-ring), the potential distribution will be more ordered
  - e.g. with low voltage, for signals, etc.
  - HV related parts requires different approaches



REDUCE PW & IMPLEMENT N-RING/DNW

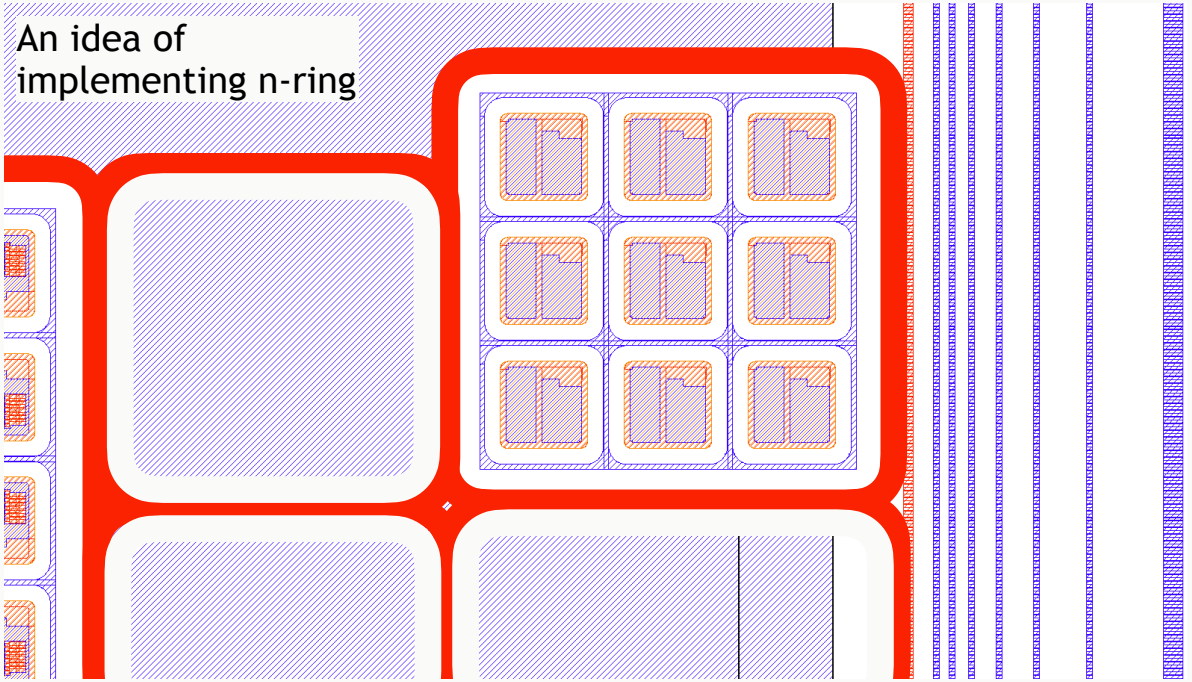
- Enclosing the floating PW with n-ring is maybe still not enough
- Too low potential may still occur at the large PW, and can cause high E-field (triggers breakdown) or punch-through
- Very extreme case:
  The PW is so large that the region beneath cannot be easily depleted
  -> the PW will have the same potential as the backside
  -> breakdown is merely determined by the spacing between PW and the surrounding n-ring

- Possible approaches (require more discussions):
  - Divide the PW into small parts
  - Add N-ring between small PW parts
  - Simply reduce the PW size, create large spacing
  - Add contact to PW to add voltage
  - Use DNW to hold the PW, merge DNW to N-ring



REDUCE PW & IMPLEMENT N-RING/DNW

Very preliminary and conceptional



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SUMMARY

- From the inspection of the design layout, several features might affect the performance of the sensor part of the detector, if the edge biasing and floating p-stop would be adopted:
  - Sharp corners —> unexpected high E-field
  - Large floating PW with an irregular shape, and the structures isolated from the pixel matrix —> potential distribution hard to predict
  - Guard ring geometry still has the room for optimisation

- The effect from floating PW has been visualised using TCAD simulation
  - A large floating PW can lead to large potential drop (high field), or punch-through
  - Using n-ring with fixed potential to divide the PW can provide a better potential distribution

- Possible measures:
  - Round sharp corners
  - Re-organise isolated structures —> build a more ordered layout
  - Use n-ring with a fixed voltage to enclose structures and divide the PW —> may help to reduce the effect of large PW
  - Use common DNW to contain some of the structures can also help to regulate the potential distribution
  - Implement a guard ring structure based on the previous knowledge