Design strategies towards a small pixel size in a large DMAPS prototype in a 150 nm CMOS process

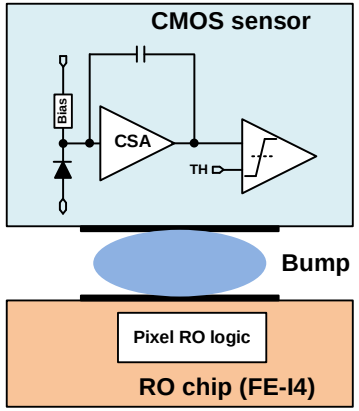
Tianyang Wang

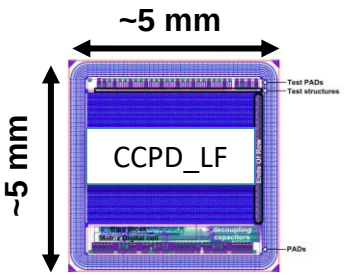
On behalf of Bonn/CPPM/IRFU LFoudry DMAPS development team

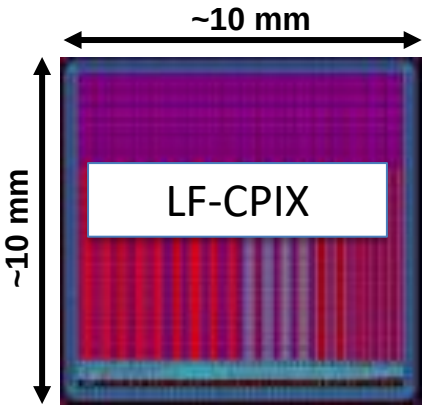
- Review of LF chips and their design strategy
- LF-Monopix1 pixel design
- LF-Monopix2 pixel design
- Outlook for smaller pixel size
- Conclusion

LFoundry DMAPS development line

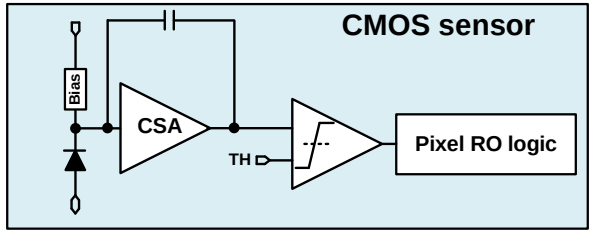
Hybridized concept (“smart pixel”)

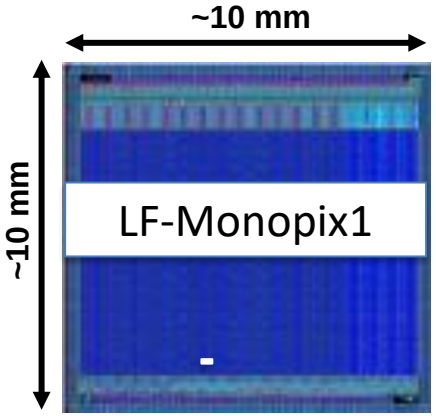


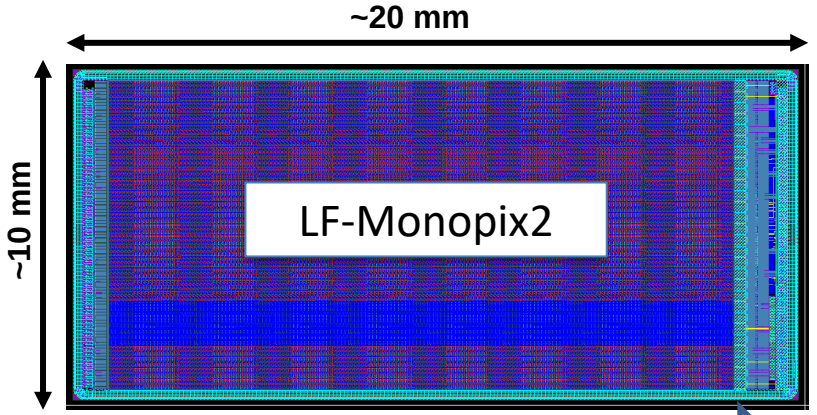




Fully monolithic concept



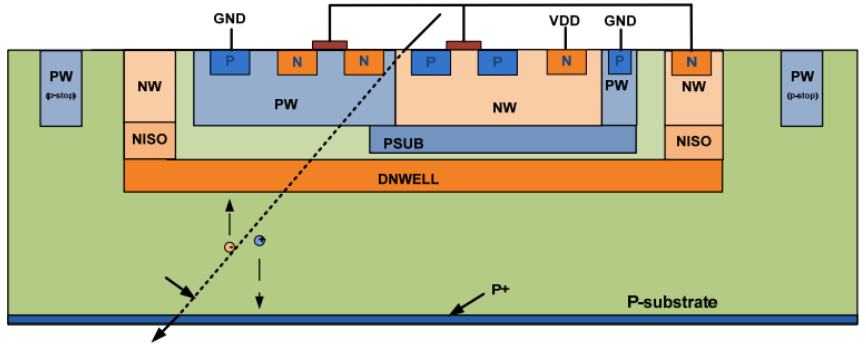




2014 2016 2020

The overall design strategy of LF-Monopix chips

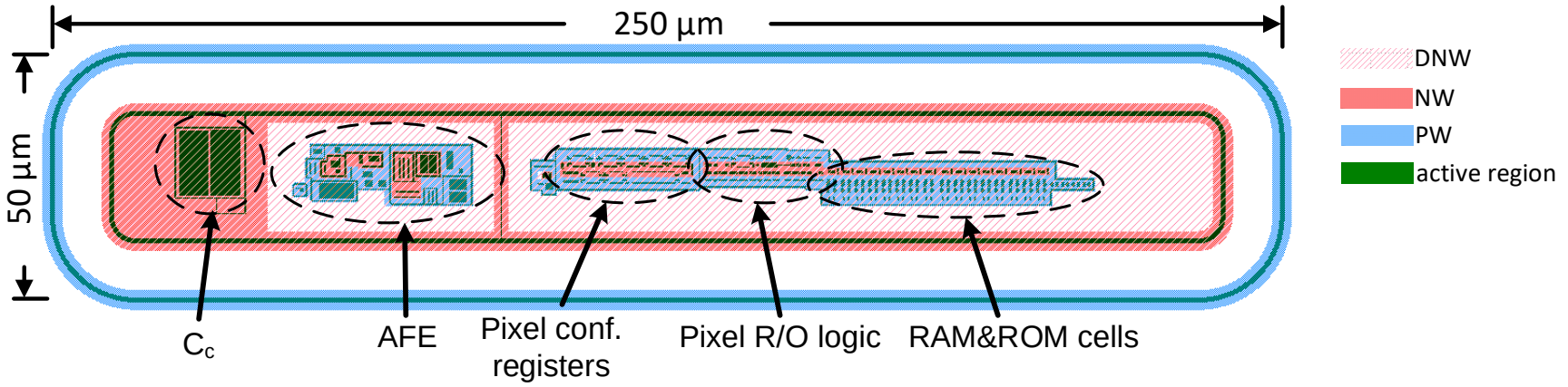
- Inherit the **know-how** from CCPD_LF & LF-CPIX
  - Sensor layout mimicking the standard planar sensor
  - Verified pixel AFE and configuration circuit
- Very **conservative** on circuit design
  - Use well-know and robust circuit structures
  - Very careful shielding scheme
  - Post layout verification is very important
- As a result, robust design has priority over small pixel pitch
  - LF-Monopix1: pixel size is the same as FE-I4 for historical reasons
    - 50 μm × 250 μm gives us margin to make some “paranoid” efforts on the pixel design
  - LF-Monopix2: pushing the pixel size to the limit would need too many (new) design changes
    - A conservative choice was made: 50 μm × 150 μm



LF-Monopix1 pixel design

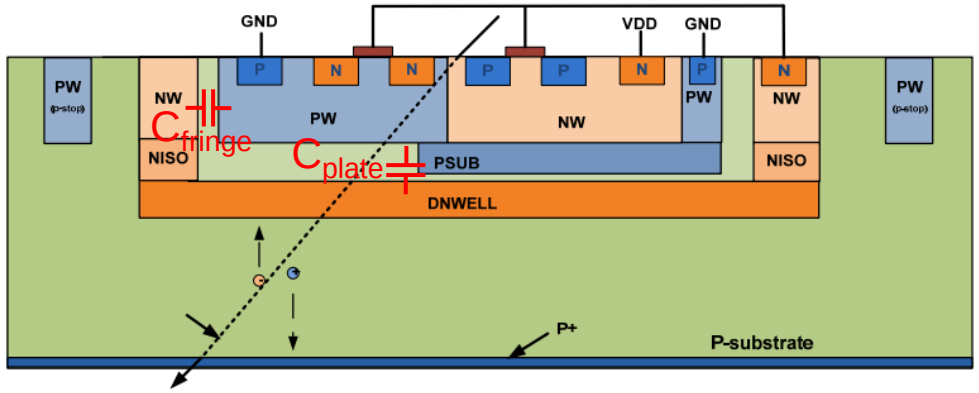
Design considerations: sensor geometry

- Key sensor layout dimensions inherited from previous active and passive pixel chips to avoid surprises on sensor performance (breakdown, charge collection, capacitance, etc.)
  - Width of P-stop (implemented with PWELL)
  - Distance between P-stop and charge collection electrode
  - Over-hang structures above P-stop (not shown in the figure)
- Charge collection electrode is 30 µm × 230 µm
  - only ~50% of the total pixel area is available for circuit implementation

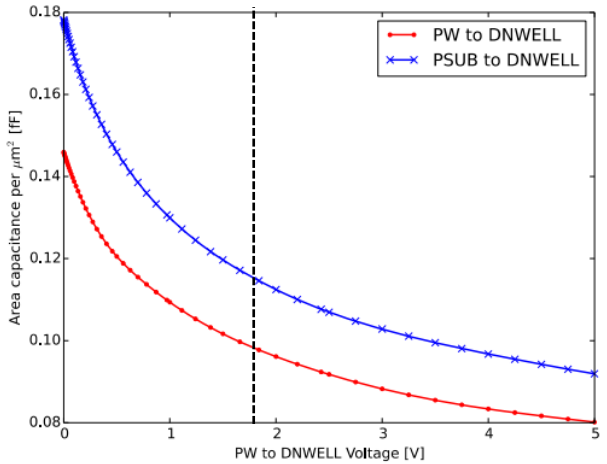


Design considerations: sensor capacitance

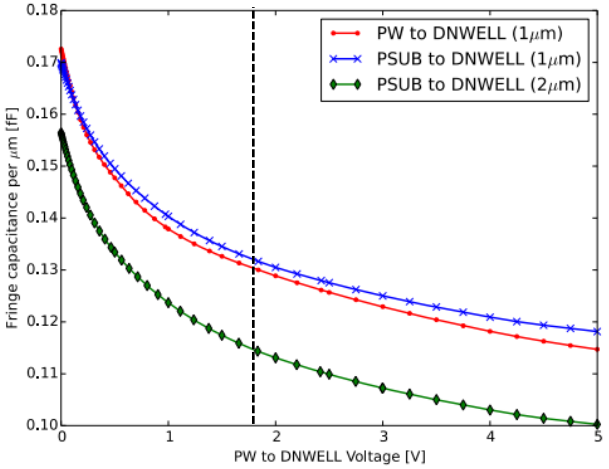
- Capacitance between circuit P-well to the inner wall of charge collection node is not small
  - In-pixel circuit is placed “far away” from vertical N wall
  - Even smaller area “reserved” for circuit if one wants to avoid this fringe capacitance



“Plate” capacitance



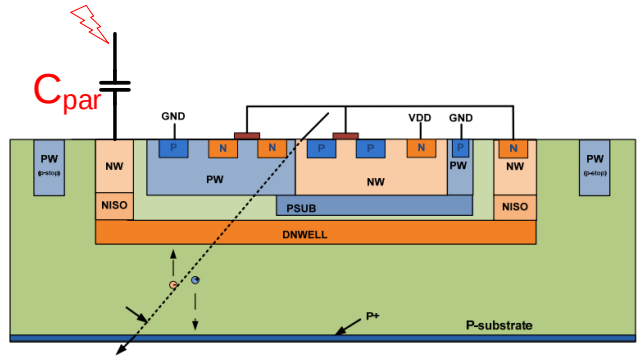
Fringe capacitance

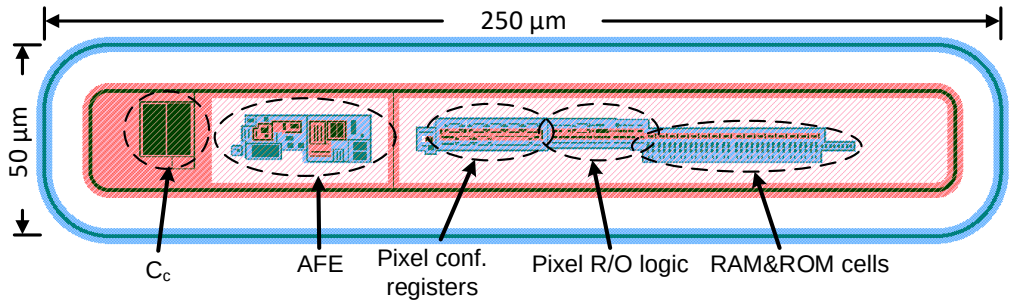


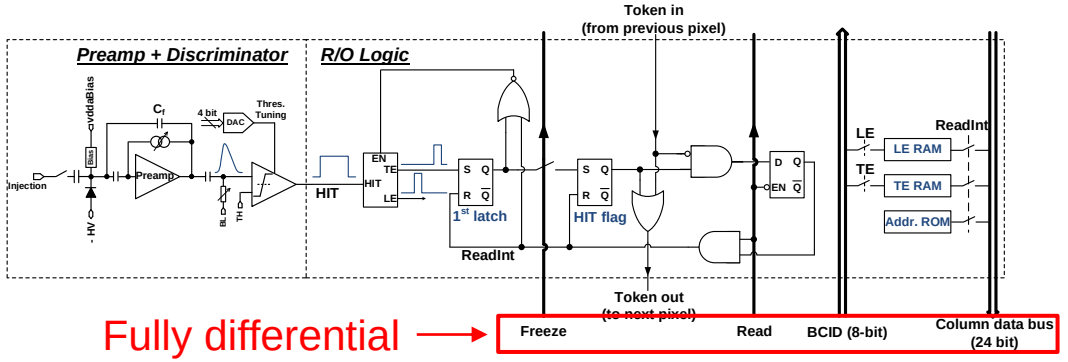
Tomasz Hemperek

Design considerations: xtalk

- Example: for C_{par} = 100 fF, dV = 1 mV => $Q_{crosstalk}$ = 625 e^-
  - Junction between DNWELL and PWELL/PSUB
    - Minimized circuit area => custom made digital logic
    - Stable gndd => minimize transient current due to digital switching
  - Parasitic from metal routing
    - Good shielding + fully differential signals for data and control lines

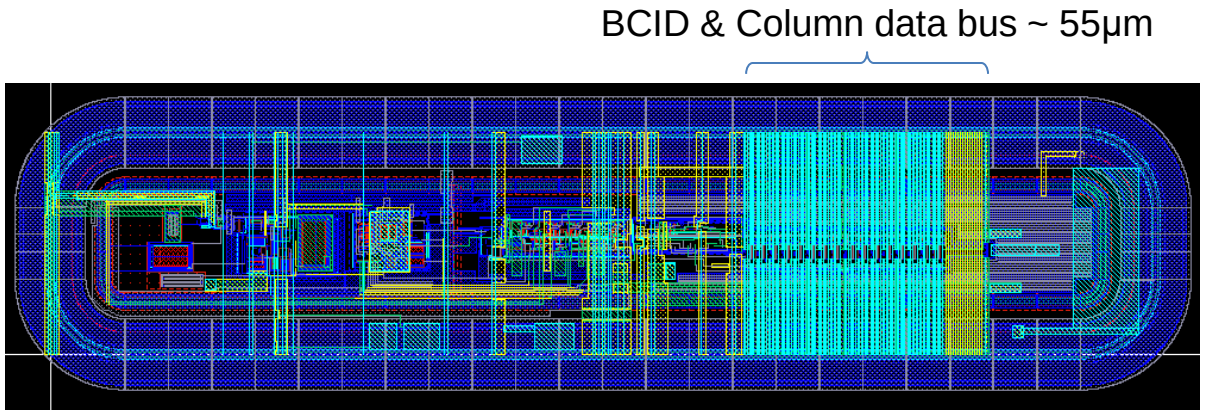






Design considerations: metal system

- Extensive shielding especially for digital column signals
  - Shielding layer under signal lines
  - Shielding between two close parallel column signal lines
- Column signal routing takes quite some space

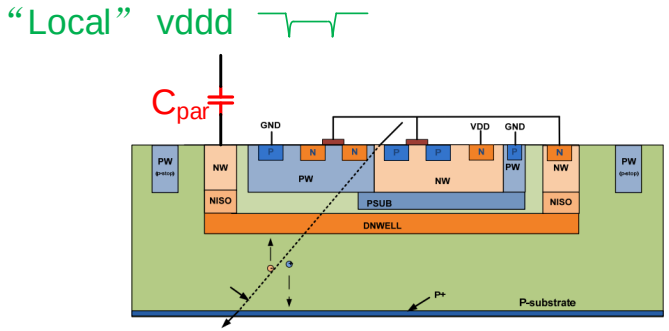


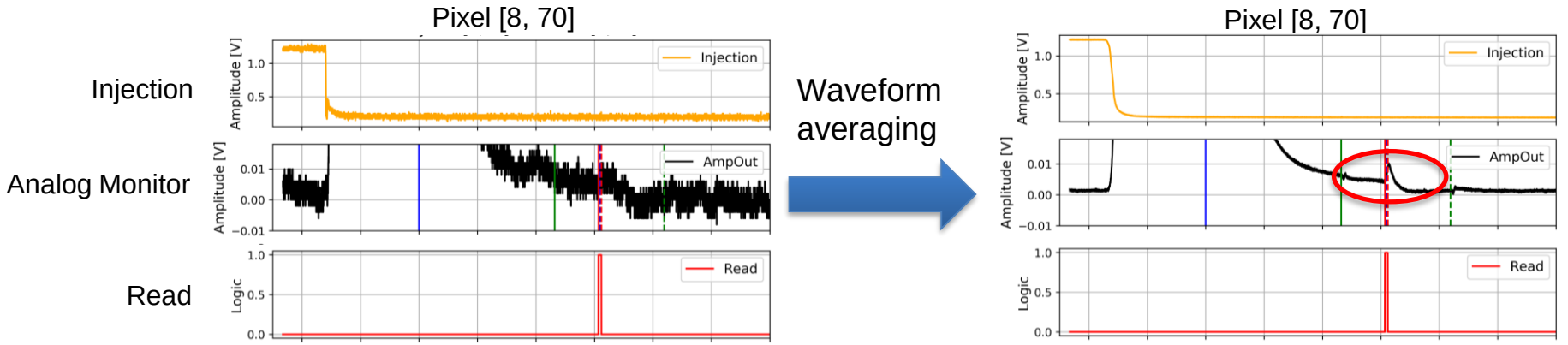
- Local routing: M1 & 2
- Shielding layer: M3 & 4
- Column signal
  - Single-ended: M5
  - Differential: M4 & 5
- PG: MF & MT
  - As wide as possible

Extensive post layout simulation for both pixel and whole column to identify coupling sources
- Column post layout simulation is time consuming and needs proper tool usage
- One can never be too careful

Xtalk measured in LF-Monopix1

- CSA output disturbance in correlation with “Read”
  - “hidden” in the noise floor => visible after “averaging”
  - Due to a flaw in the shielding scheme using vddd



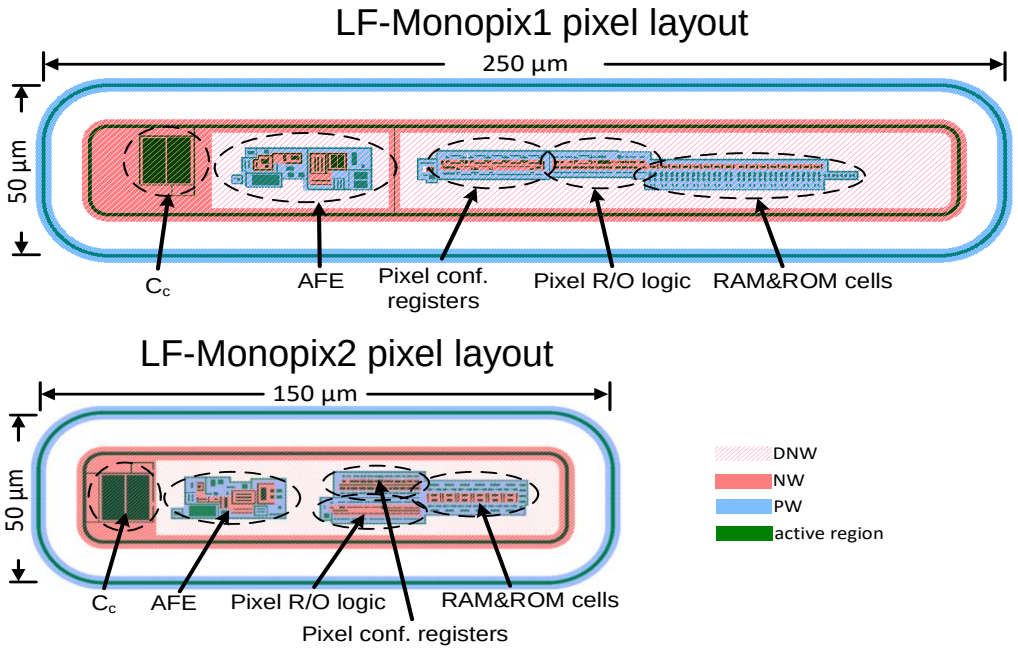


Doubts existed even among ourselves for such a large electrode DMAPS design, but the chip ended up nicely => Prove a good performing large electrode DMAPS chip with complicated pixel circuit for **the first time**

LF-Monopix2 pixel design

LF-Monopix2: towards a smaller pixel

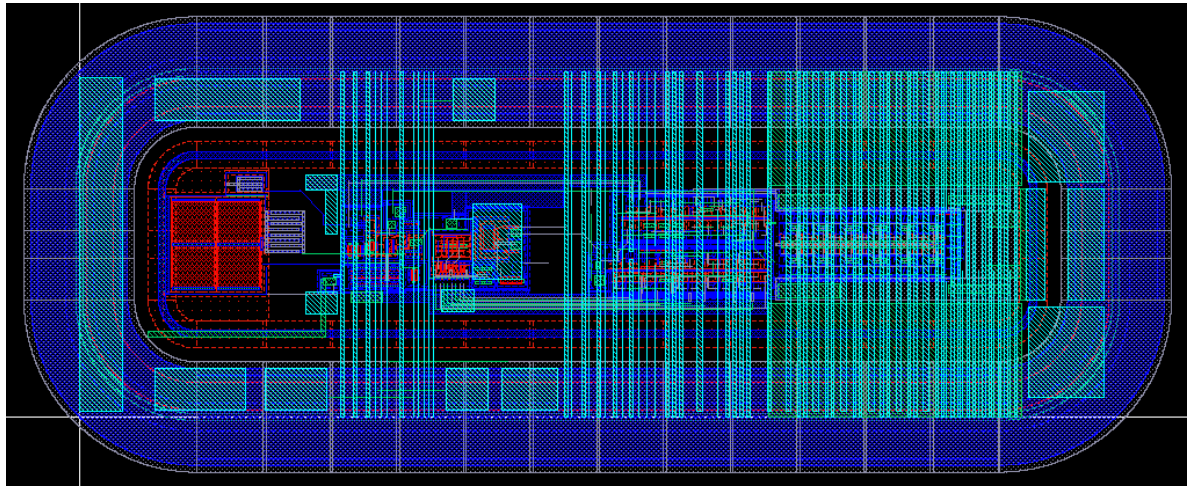
- Key sensor geometries kept the same
  - We did not want to take risks before new possibilities being carefully studied
  - Max. ~50% pixel area for circuit
- Time stamp reduced from 8-bit to 6-bit
  - Should be careful about data loss @ high rate
- Digital logic further optimized for smaller area
  - But only limited improvement could be made



The total circuit area adds up to ~ 1500µm^2 which defines the ultimate pixel area with the existing circuit design

LF-Monopix2: towards a smaller pixel

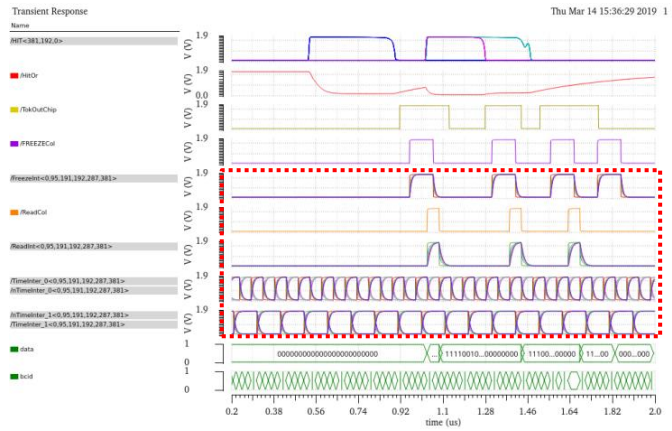
- Remove some overdoing in LF-Monopix1
  - Single-ended signaling used for “Read” & “Freeze” => good shielding suffices
  - No shielding between lines of column data bus => need careful simulation
- Fix the “Read” xtalk in LF-Monopix1
  - Fix was proven effective by measurements



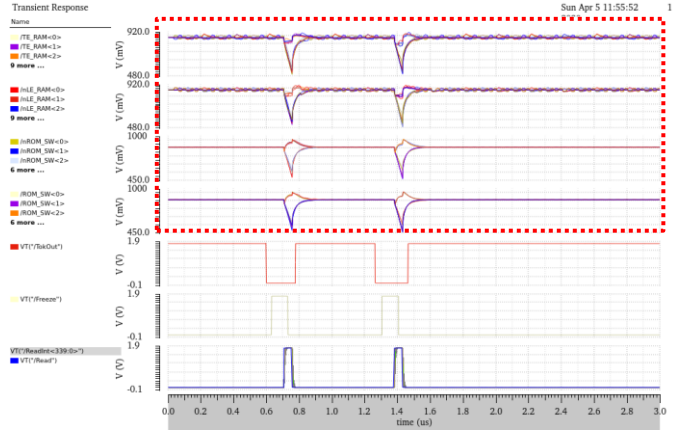
- Local routing: M1 & 2
- Shielding layer: M3 & 4
- Column signal
  - Single-ended: M5
  - Differential: M4 & 5
- PG: MF & MT
  - As wide as possible

LF-Monopix2: towards a smaller pixel

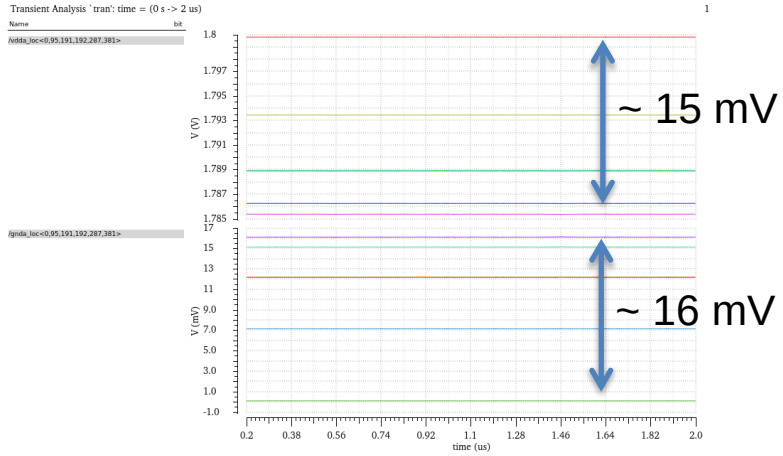
- Many tedious full column post layout simulation to ensure signal integrity



Signal slew & skew along the column



Xtalk and operation speed of column data bus



IR of PG along the column

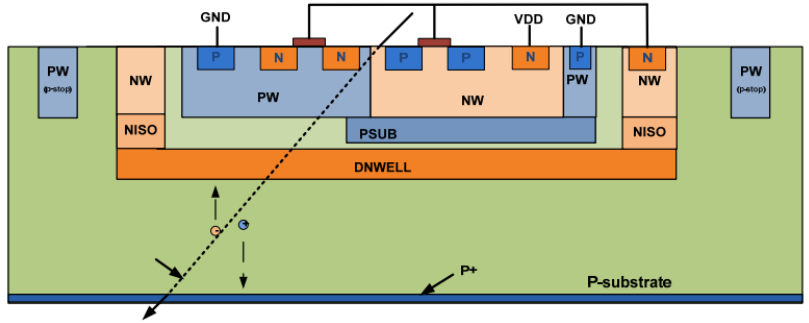
Line width, spacing & shielding

Metal width and layers used for PG

Influence minimum pixel pitch

Outlook to a smaller pixel size

- Squeeze the sensor structure
  - Slimmer P-stop => limited to 1.5μm from foundry design rules
  - Smaller gap between charge collection node & P-stop
    - Capacitance to P-stop? H. Krueger, doi: 10.1088/1748-0221/16/01/P01029
    - Breakdown behavior?
- Smaller gap between N "wall" and circuit P well
  - "Fringe" capacitance
- Column line routing
  - Share lines between two neighboring pixel columns
    - More complex routing within the pixel
    - Larger line load => signal skewing
- Narrower PG metal => IR drop



Conclusions

- LF-Monopix chip series is a nicely performing large electrode DMAPS design
  - Demonstrate large electrode DMAPS with complicated in-pixel circuitry
  - Chip performance verified in large scale matrix
- A smaller pixel (50 μm × 150 μm) achieved in LF-Monopix2
  - Not an ultimate small pixel, but a robust pixel with conservative design strategy
  - Performance improvement over LF-Monopix1 verified in measurement
- The ultimate pixel size calls for very careful studies on different aspects
  - May require trade off breakdown, pixel capacitance, xtalk, circuit robustness, etc.