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Design strategies towards a small pixel size in a large DMAPS prototype in a 150 nm CMOS process

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LF-Monopix2 is the latest prototype in a decade-long R&D effort to develop a large DMAPS device in a 150 nm CMOS process. All pixels in this chip contain both digital and analog electronics within their collection node and they are read-out through a fast column-based synchronous architecture. The design follows the so-called "large electrode" approach, where a careful layout of each pixel's wells and circuitry is necessary in order to avoid low breakdown voltage or spurious signals coupled to the collection node due to digital activity.

This contribution will outline the design strategy of the LF-Monopix chip series, with an emphasis on the pixel layout design for small pixel size and cross-talk mitigation. In addition, it will present an outlook of the challenges and possible approaches to reduce it even further in a future device.

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